ETM32E-01

EPSON TOYOCOM

Application Manual

Real Time Clock Module

RX-5412SF

EPSON TOYOCOM CORPORATION

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CONTENTS

Serial Interface RTC Module

RX - 5412 SF

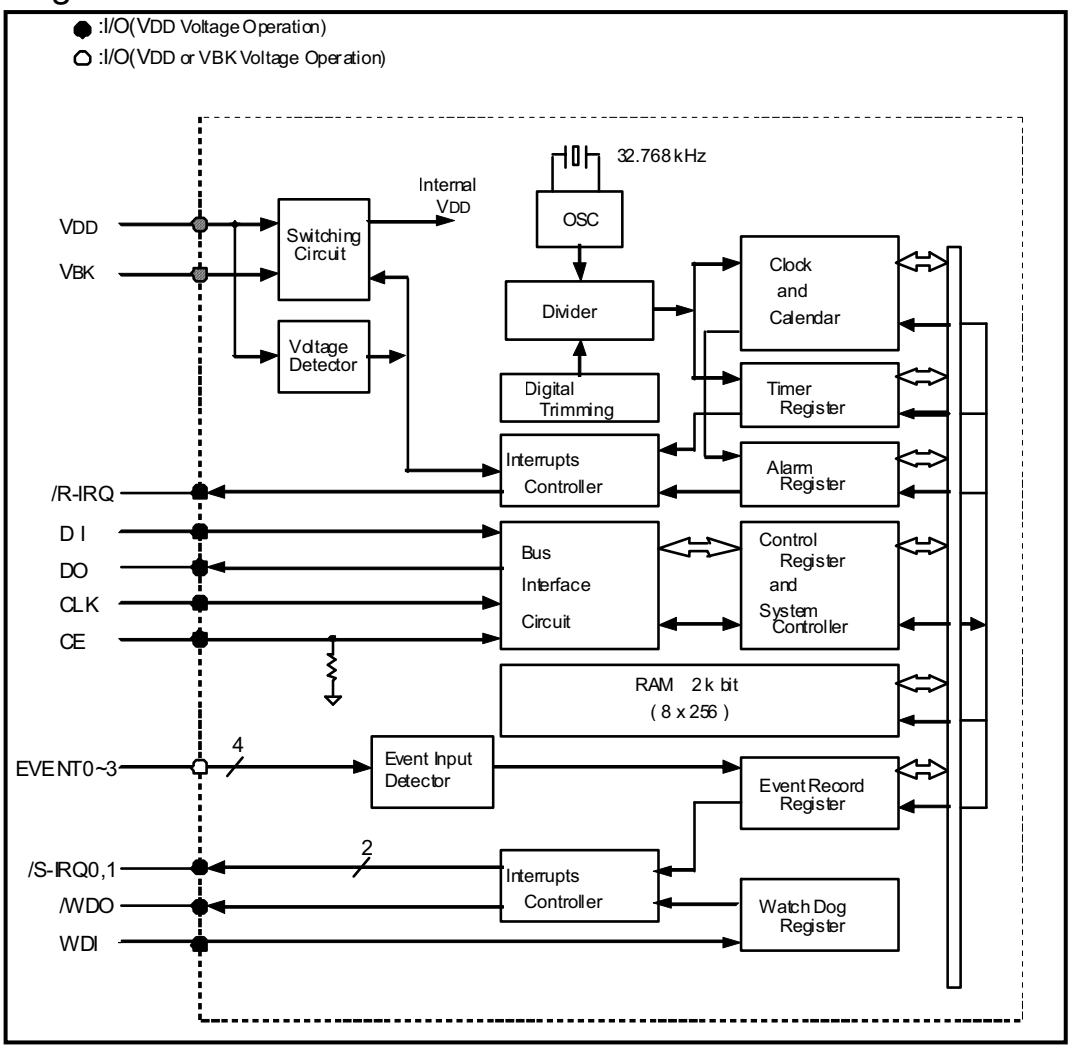
- Built-in 32.768 kHz crystal oscillator with frequency adjusted
- Serial interface in 4 lines form
  (possible to make it to 3 lines by wired-OR connecting DI and DO pins)
- Alarm interrupt function for day of the week, day, hour, and minute (/IRQ pin)
- Automatic adjustment for leap year (supports from year 2000 to 2099)
- Time update interrupt function (second·minute, /IRQ pin)
- Event record function can record separate time data in each of event input terminal.
- Wide range of interface voltage between 2.5 V and 5.5 V
- Wide range of clock (retained) voltage between 1.4 V and 5.5 V
- Low current consumption at 0.5 μA / 3 V (Typ.)

1. Overview

This module is a real-time clock with serial interface in 4 lines form (or 3 lines form). It has a built-in crystal oscillator. The module offers many functions such as Clock & Calendar circuitry with automatic leap year adjustment, interval timer, time update interrupt.

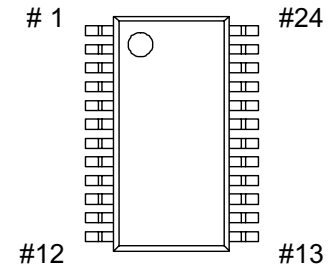
And, this module has many function such as a event detection, time stamp record, a watch dog timer and a power supply monitor .

2. Block diagram



3. Terminal description

3.1. Terminal connections



3.2. Pin functions

Signal name	Pin No.	I / O	Function	terminal name	Pin No.	I / O	Function
VSS	1	-	GND	(VSS)	24	-	
EVENT0	2	Input	Event input	(VSS)	23	-	
EVENT1	3	Input	Event input	(VSS)	22	-	
VBK	4	-	Backup power supply	(VSS)	21	-	
EVENT2	5	Input	Event input	(VSS)	20	-	
(VSS)	6	-		(VSS)	19	-	
EVENT3	7	Input	Event input	/S-IRQ1	18	Output	Event record interrupt output (open drain)
CE	8	Input	Chip enabled input	/S-IRQ0	17	Output	Event record interrupt output (open drain)
CLK	9	Input	Clock input pin for serial data transmission	WDI	16	Input	Watch dog input (open drain)
DO	10	Output	Data output pin for serial data transmission	/WDO	15	Output	Watch dog output (open drain)
DI	11	Input	Data input pin for serial data transmission	N.C.	14	-	-
/R-IRQ	12	Output	RTC function interrupt output (open drain)	VDD	13	-	Power supply

4. Absolute maximum ratings

GND=0 V

Item	Symbol	Condition	Rating	Unit
Power voltage	V_{DD}	Between V_{DD}, V_{BK} and GND	−0.3 to +6.5	V
Input voltage	V_{IN}	Input pin	GND−0.3 to +6.5	V
Output voltage (1)	V_{OUT1}	DO pin	GND−0.3 to V_{DD} +0.3	V
Output voltage (2)	V_{OUT2}	Output pin(other than DO)	GND−0.3 to +6.5	V
Storage temperature	T_{STG}	Stored bare product after unpacking	−55 to +125	°C

5. Recommended operating functions

GND=0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating power voltage	V_{DD}	V_{DD} pin	V_{DET}	3.0	5.5	V
Time Stamp function operation voltage	V_{CH}	V_{DD} or V_{BK} pin	1.4	3.0	5.5	V
Clock power voltage	V_{CLK}	V_{DD} or V_{BK} pin	V_{LOW}	3.0	5.5	V
Input voltage	V_{IN}	Input pin	0	-	5.5	V
Output voltage (1)	V_{OUT1}	DO pin	GND	-	V_{DD}	V
Output voltage (2)	V_{OUT2}	Output pin(other than DO)	0	-	5.5	V
Operating temperature	T_{OPR}	No condensation	−40	+25	+85	°C

6. Frequency characteristics

GND=0 V

Item	Symbol	Condition	Rating	Unit
Frequency precision	$\Delta f / f$	Ta= +25 °C, V_{DD}=3.0 V	5 ± 23 (*1)	$\times 10^{-6}$
Frequency voltage characteristics	f / V	Ta= +25 °C, V_{DD}=2.0 V to 5.0 V	± 2 Max.	$\times 10^{-6}$ / V
Frequency temperature characteristics	Top	Ta= −20 °C to +70 °C, V_{DD}= 3.0 V ; reference at +25 °C	+10 / −120	$\times 10^{-6}$
Oscillation start up time	tSTA	Ta= +25 °C, V_{DD}=3.0 V	3 Max.	s
Aging	fa	Ta= +25 °C, V_{DD}=3.0 V ; first year	± 5 Max.	$\times 10^{-6}$ / year

*1) This difference is 1 minute by 1 month. (excluding offset)

7. Electrical characteristics

*If not specifically indicated, GND=0 V, V_{DD}=2.5 V to 5.5 V, Ta= −40 °C to +85 °C

7.1. DC electrical characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{BK1}	CE = GND, VDD =0V Output pin = OPEN A current to supply from VBK.	V_{BK}=5 V		0.5	1.0	μA
Current consumption (2)	I_{BK2}		V_{BK}=3 V		0.5	1.0	
Current consumption (3)	I_{DD1}	VDD =3V ,VDET<VDD Output pin = OPEN A current to supply from VDD.	CE=GND		12	50	
Current consumption (4)	I_{DD2}		During access (FCLK=2MHz)		80	160	
Current consumption (5)	I_{DD3}	VDD =5V ,VDET<VDD Output pin = OPEN A current to supply from VDD.	CE=GND		18	180	
Current consumption (6)	I_{DD4}		During access (FCLK=2MHz)		120	240	
"H" input voltage(1)	V_{IH1}	Input pin(other than Event0-3)		0.7 × V_{DD}		5.5	V
"H" input voltage(2)	V_{IH2}	Input pin(Event0-3)		0.7 × V_{CH}		5.5	
" L " input voltage(1)	V_{IL1}	Input pin(other than Event0-3)		0		0.3 × V_{DD}	
" L " input voltage(2)	V_{IL2}	Input pin(Event0-3)		0		0.3 × V_{CH}	
"H" Output voltage	V_{OH1}	DO pin	V_{DD} = 5 V, I_{OH} = −1 mA	4.5		5.0	V
	V_{OH2}		V_{DD} = 3 V, I_{OH} = −1 mA	2.2		3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = −100 μA	2.9		3.0	
"L" Output voltage	V_{OL1}	DO pin	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 μA	GND		GND+0.1	
	V_{OL4}	Open drain output pin.	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.25	
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.4	

Input resistance (1)	R_{DWN1}	CE pin V_{IN} = V_{DD}	V_{DD}=5 V	75	150	300	kΩ
Input resistance (2)	R_{DWN2}		V_{DD}=3 V	150	300	600	kΩ
Input leakage current	I_{LK}	Input pin other than CE V_{IN} = V_{DD} or GND		−0.5		0.5	μA
Output leakage current	I_{OZ}	Output pin, V_{OUT} = V_{DD} or GND		−0.5		0.5	μA
Power supply detection voltage	V_{DET}	V_{DD} pin		2.45	2.5	2.55	V
	V_{LOW}	V_{DD} pin		1.0	1.2	1.4	

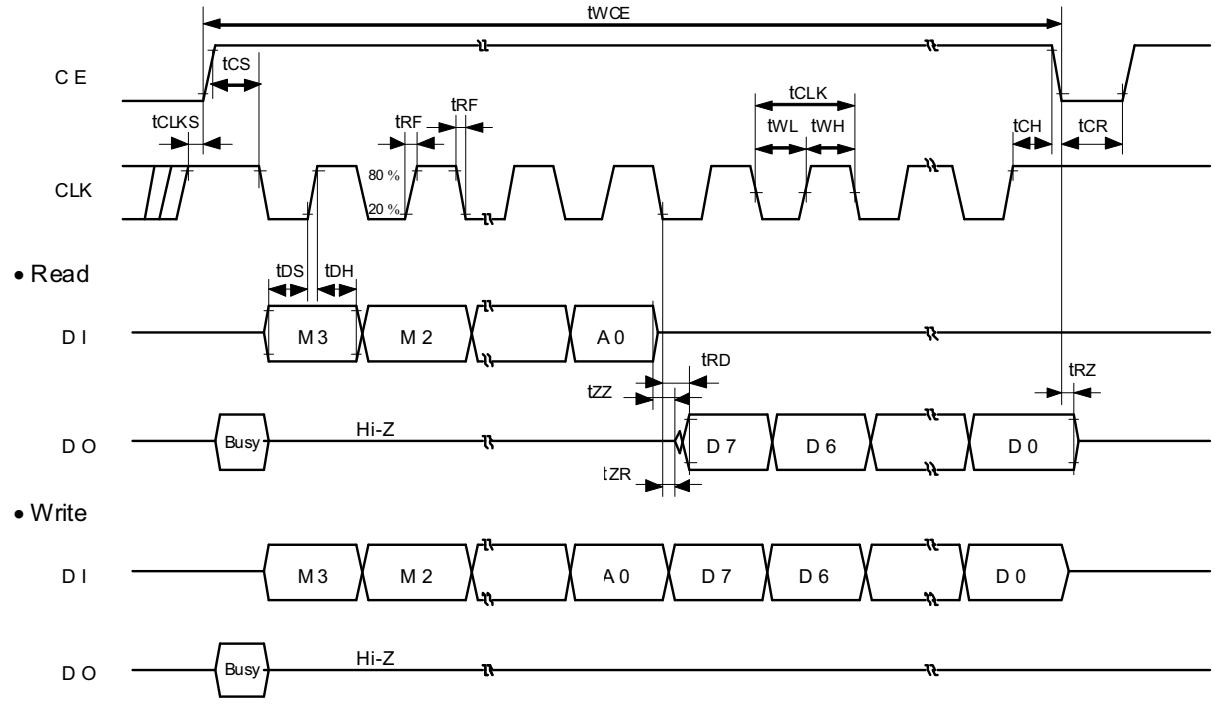
7.2. AC electrical characteristics

∗If not specifically indicated, GND=0 V, Ta= −40 °C to +85 °C

Item	Symbol	Condition	V_{DD} = 3 V ±10%		V_{DD} = 5 V ±10%		Unit
			Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		500	10000	350	10000	ns
CLK H pulse width	t_{WH}		250		175		ns
CLK L pulse width	t_{WL}		250		175		ns
CLK rise and fall time	t_{RF}			100		50	ns
CLK setup time	t_{CLKS}		50		25		ns
CE setup time	t_{CS}		200		150		ns
CE hold time	t_{CH}		200		100		ns
CE recovery time	t_{CR}		300		200		ns
CE enable time	t_{WCE}			0.95		0.95	s
Write data setup time	t_{DS}		100		50		ns
Write data hold time	t_{DH}		100		50		ns
Read data delay time	t_{RD}	C_L=50 pF		200		150	ns
DO output switching time	t_{ZR}			50		25	ns
DO output disable time	t_{RZ}	C_L=50 pF R_L=10 kΩ		200		100	ns
DI/DO conflict avoiding time	t_{ZZ}		0		0		ns
WDI H pulse width	t_{WWH}		250		175		ns
WDI L pulse width	t_{WWL}		250		175		ns

*When you use a time stamp function, tWCE1 is applied, and tWCE2 is applied when you do not use a this function.

Timing chart



∗ If DI and DO pins are wired-OR connected to make it to 3 lines form, secure tzz to avoid bus conflict.

8. How to use

8.1. Real-time clock function summary

1) Clock functions
This function is used to set and read out month, day, hour, date, minute, second, and year (last two digits) data.
Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

2) Timer function
Timer function which can be set up between 1/4096 second and 4095 minutes.

3) Alarm function
Alarm function can be set to free combination of day, day of week, hour, or minute.

4) Automatic power switching function

When it monitor the main power supply and detect a voltage drop, switch it to a backup power supply automatically.

8.2. Extension function summary

1) Detection of an external event and a time stamp function
4 event port, can detect an event input with selectable detection cycle and record time stamp data to a memory.

2) Watchdog function

When detect halt of input signal on WDI terminal, this function can output an interrupt signal.

3) S-RAM function

S-RAM (256 words x 8 bits (2048 bits)) useful for event recording and general purpose memory.

8.3. Register table

[Bank 0]

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
00	SEC	○	40	20	10	8	4	2	1	∗3
01	MIN	○	40	20	10	8	4	2	1	∗3
02	HOUR	○	○	20	10	8	4	2	1	∗3
03	WEEK	○	6	5	4	3	2	1	0	∗3
04	DAY	○	○	20	10	8	4	2	1	∗3
05	MONTH	○	○	○	10	8	4	2	1	∗3
06	YEAR	80	40	20	10	8	4	2	1	
07	RAM	●	●	●	●	●	●	●	●	∗4
08	MIN Alarm	AE	40	20	10	8	4	2	1	
09	HOUR Alarm	AE	●	20	10	8	4	2	1	∗4
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	∗4
	DAY Alarm		●	20	10	8	4	2	1	
0B	Timer Counter 0	128	64	32	16	8	4	2	1	
0C	Timer Counter 1	●	●	●	●	2048	1024	512	256	∗4
0D	Control Register 0	TEST1	WADA	USEL	TE	○	○	TSEL1	TSEL0	∗2, ∗3
0E	Control Register 1	VDET	VLOW	UF	TF	AF	○	VLF	PON	∗1, ∗7
0F	Control Register 2	TEST2	○	UIE	TIE	AIE	○	STOP	RESET	∗2, ∗7
20	Event Input 0	PE0	ME0	HL0	○	○	○	E0S1	E0S0	
21	Event Input 1	PE1	ME1	HL1	○	○	○	E1S1	E1S0	
22	Event Input 2	PE2	ME2	HL2	○	○	○	E2S1	E2S0	
23	Event Input 3	PE3	ME3	HL3	○	○	○	E3S1	E3S0	
24	Event Control	C1	C0	T1	T0	○	MP	MS1	MS0	
25	Memory Data Select	PN	Year	Month	Day	Week	Hour	Min.	Sec.	
26	Memory Address	128	64	32	16	8	4	2	1	
27	Memory Alarm	128	64	32	16	8	4	2	1	
28	Voltage Detection	○	○	DT1	DT0	○	○	○	○	
29	Watch Dog Register	WD3	WD2	WD1	WD0	WDP	○	○	WDE	
2A	Flag Register	EF3	EF2	EF1	EF0	○	WDF	BF	MF	
2B ⏐ FF	Reserved	Reserved								∗5

[Bank 1]

Address([h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
00	RAM 00	●	●	●	●	●	●	●	●	∗4
01	RAM 01	●	●	●	●	●	●	●	●	∗4
⋮	⋮	⋮				⋮				⋮
FE	RAM FE	●	●	●	●	●	●	●	●	∗4
FF	RAM FF	●	●	●	●	●	●	●	●	∗4

Note When after the initial power-up or when the result of read out the VLF bit is "1" , initialize all registers, before using the module.

∗1) Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

∗2) TEST1, TEST2 bit are bit for our test. Be sure to set zero "0" when write.

∗3) The '○' mark indicates a write-prohibited bit, which returns a "0" when read.

∗4) The '●' mark indicates a read/write-accessible RAM bit for any data.

∗5) Address 10h-1Fh of Bank 0 is a register for our inspection, so please do not access there. In such case, the time keeping operation cannot be guaranteed. Further, 2B h - FF h (Reserved register) is a register for our setting. It is inability to write and is not nfixed when read.

∗6) Address 00 h ~ FF h of Bank 1 is a register for event record.
And it is also possible to use as RAM bit that is able to R/W of optional data.

∗7) Address 0E h of Bank 0 is a flag register of an RTC function.
Be sure not to set "1" when write.

9. Real-time clock function summary

9.1. Register description

9.1.1. Clock and calendar registers (Reg-0 to Reg-6/Bank0)

- Data format

  Data is in the BCD format. For example, if the SEC register is set to "0101 1001", this means 59 seconds. The time measurement is in 24-hour format (fixed).

- YEAR register and leap year

  The YEAR register becomes year 00 after year 99.

  Divide the YEAR register's 2-digit BCD by four, and if the remainder is 0, then this year is determined as the leap year. (Year 00 is processed as a leap year. This calendar expires in year 2099.)

- Day of the WEEK register

  The day of the WEEK register is made of 7 bits from 0 to 6. The bits are assigned as shown in the following table.

  Be sure not to set multiple days of week to "1".

bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day of the week
0	0	0	0	0	0	**1**	Sunday
0	0	0	0	0	**1**	0	Monday
0	0	0	0	**1**	0	0	Tuesday
0	0	0	**1**	0	0	0	Wednesday
0	0	**1**	0	0	0	0	Thursday
0	**1**	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

9.1.2. Alarm registers (Reg-8 to Reg-A / Bank0)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN alarm	AE	40	20	10	8	4	2	1
9	HOUR alarm	AE	•	20	10	8	4	2	1
A	WEEK alarm	AE	6	5	4	3	2	1	0
	DAY alarm		•	20	10	8	4	2	1

You can set the day of the week, day, hour and minute for alarm. The WADA bit specifies which alarm of the WEEK alarm or the DAY alarm assign to the register A.

Bit 7 is the AE (Alarm Enable) bit for all the alarm registers. By using this bit, you can easily set the hourly alarm and the daily alarm. The day of the week alarm can be set to any multiple days of week.

When the AE bit is set to "0", the appropriate register and the clock register are compared; when the AE bit is set to "1" ("don't care"), the two registers are not compared because they are considered to have the same value.

When the alarm goes off, the AF (Alarm Flag) bit of Reg-E is set to "1"; if at this moment the AIE (Alarm Interrupt Enable) bit of Reg-F has been set to "1", the /IRQ pin is set to the low level and the interrupt signal occurs. If the AIE bit has been set to "0", the alarm interrupt output from the /IRQ pin is prohibited.

If alarm interrupt is not used, then addresses 8 to A can be used as memory registers. In this case, set the AIE bit to "0" to prohibit usage of the alarm and alarm interrupt.

- The relationship between the day of the week alarm bit and each day of the week

bit	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0
Day of the week	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

9.1.3. Timer counter (Reg-B and Reg-C / Bank0)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer counter 0	128	64	32	16	8	4	2	1
C	Timer counter 1	•	•	•	•	2048	1024	512	256

This register controls 12 bits of internal preset-able down counter used for timer interrupt.
TSEL0 and TSEL1 of Reg-D specify the count cycle of the down counter (source clock). Timer counter 0 and timer counter 1 specify the preset value of the down counter.

When the TE bit of Reg-D is set to "0, The presetable counter loads the written data to the timer counter (It is initial value.), and then stops the count down. Afterwards, when the TE bit set to 1, count down starts.

Using a source clock cycle, the down counter continues the countdown. When the data becomes zero, the TF (Timer Flag) of Reg-E is set to "1". At this moment, if the TIE bit (Timer Interrupt Enable) of Reg-F was set to 1 beforehand, the /IRQ pin is asserted low for generate the interrupt signal.
When the TIE bit is set to "0", output from the /IRQ pin is prohibited.

Next, it reloads the data of timer counter register and restarts the countdown (repeat operation).
But, even if write 1 to the TE bit, and write 0 to the timer counter, timer interrupt from the /TIRQ pin is not generated. In order to operate timer expectedly, you should set the TE bit and the TIE bit adequately.

If timer interrupt is not used, then addresses B and C may be used as memory registers. In this case, set TE bit and TIE bit to "0", to prohibit timer operation and timer interrupts.

• Timer interrupt and source clock selection

TSEL1	TSEL0	Source clock
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	Update in minutes

• Timer interrupt interval

Timer counter setting value	Source clock			
	4096 Hz	64 Hz	1 Hz	Update in minutes
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

9.1.4. Control register and flag register (between Reg-D and Reg-F / Bank0)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension register	TEST	WADA	USEL	TE	○	○	TSEL1	TSEL0
E	Flag register	VDET	VLOW	UF	TF	AF	○	VLF	PON
F	Control register	TEST	○	UIE	TIE	AIE	○	STOP	RESET

- TEST bit: This bit is used by manufacture for testing.
  Be sure to set this bit to "0". Be careful not to set this bit to "1" when writing to other bits of Reg-D.
  When CE pin goes to L, TEST is cleared .

- WADA bit (WEEK Alarm / DAY Alarm)
  This bit sets either the WEEK alarm or the DAY alarm. When this bit is 0, the Reg-A is re-assigned to the WEEK alarm register. And when this bit is 1, the Reg-A is re-assigned to the DAY alarm register.

- USEL bit (Update Interrupt Select)
  Specify the occurrence timing of time update interrupt.
  [Selection of timing for time update interrupt]

USEL	Timing	Auto recovery time
0	Update in seconds	7.813 ms
1	Update in minutes	7.813 ms

- TE bit (Timer Enable)
  When the TE bit is 0, The presetable counter loads the written data to the timer counter (It is initial value.), and then stops the count down. And when the TE bit is 1, count down starts.

- VDET (Voltage Detect)
  When power supply is higher than VDET voltage, this bit shows 0. And when power supply is lower than VDETvoltage, this bit shows 1. But in this case, this bit continues keeping 1 till it is cleared by 0.
  This bit is not affected by another bits (STOP, RESET). You cannot write "1" over these bits.

- VLOW (Voltage Low)

  When power supply is higher than VLOW voltage, this bit shows 0. And when power supply is lower than VLOW voltage, this bit shows 1. But in this case, this bit continues keeping 1 till it is cleared by 0.
  This bit is not affected by another bits (STOP, RESET). You cannot write "1" over these bits.

- AF bit, TF bit, and UF bit (Alarm Flag, Timer Flag, Update Flag)
  When the alarm occurs , the AF bit is set to 1. When the data is just zero, the TF (Timer Flag) of Reg-E is set to 1. At the end of time update, the UF bit is set. These data 1 is retained until writing over them with 0. You cannot write "1" over these bits.

- AIE bit, TIE bit, and UIE bit (Alarm, Timer, Update Interrupt Enable)
  These bits control whether or not to generate interrupt signal from IRQpin, when alarm, timer, or time update interrupt event occurs. AIE corresponds to alarm interrupt, TIE corresponds to timer interrupt, and UIE corresponds to time update interrupt.

- VLF (Voltage Low Flag)
  This bit shows the logic sum of each bit (VLOW, ICNT, PON). In this case, this bit continues keeping 1 till it is cleared by 0. This bit is not affected by another bits (STOP, RESET).

- PON bit (Power On Reset)

  When the initial power-up occurs, or device returns from a blackout or such as, this bit shows 1.
  And this case, this bit continues keeping 1 till it is cleared by 0.
  This bit is not affected by another bits (STOP, RESET).

- STOP bit
  When this bit is set to "1", the operation of counting up the seconds in the Clock & Calendar circuitry is stopped, which stops the clock. When this bit is set to "0", the clock resumes its operation.

- RESET bit
  When this bit is set 1, clock update was stop and clock data (digits of less than a second) is reset. This bit continues keeping 1 till it is cleared by 0.but CE terminal turned into L, this bit is cleared automatically.

9.1.5. Event detection setting register (Reg - 20-23 [h] / Bank 0)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20	Event Input 0	PE0	ME0	HL0	○	○	○	E0S1	E0S0
21	Event Input 1	PE1	ME1	HL1	○	○	○	E1S1	E1S0
22	Event Input 2	PE2	ME2	HL2	○	○	○	E2S1	E2S0
23	Event Input 3	PE3	ME3	HL3	○	○	○	E3S1	E3S0

The setting of event detection and record is set by this register.
It is able to set each pin of EVENT 0-3 individually.
Event Input 0 support EVENT0 pin, Event Input 1support EVENT1 pin, Event Input 2 support EVENT2 pin and Event Input 3 support EVENT3 pin.

1) PE0-3 bit (Port Enable)

When each PE bit is 1 , each event detection operation is enabled.
When each PE bit is 0 , each event detection operation is inhibited.
When supply initial power, all pins [”0”] are selected.

2) ME0-3 bit (Memory Enable)

When each ME bit is 1, each memory record functions enabled.
When each ME bit is 0, each memory record functions are inhibited.
Even if memory record is void, it is able to output the interrupt signal when detect event input by means of setting E0S1-E3S1,E0S0-E3S0bit.
When MP bit is 1 and MF bit is 1 ,ME0-3 bit is cleared .
You must set ME0-3 bit to 1 after you set MP bit to 0 or MF bit to 0 to validate a record function

3) HL0-3bit (Rise/Fall select)

Specify detection level of event input.
When each HL bit is 1, it detects event by hold "H"level input that is longer than chattering cancel cycle.
When each HL bit is 0, it detects event by hold "L"level input that is longer than chattering cancel cycle.

4) E0S1-E3S1/E0S0-E3S0 bit

This register controls the output of interrupt signal of event input.
It choose which pin it outputs an interrupt signal to.
It can select either /S-IRQ1 pin or /S-IRQ0 pin.
When each bits are set to "1", interrupt-signal is output from selected terminal pin.
In case of selecting multiple input pins such as E0S1and E1S1 etc., signal is output with OR from interrupt pin.
In case of selecting multiple bit such as E0S1and E0S0 etc., interrupt signal is output both to /S-IRQ1pin and /S-IRQ0 pin.
When initial power-on is occur, these all bits are cleared and inhibits the interrupt-signal output, sure.
Relations concerning control bit and event input pin are shown below.

Operation if set “1” to each bit.

bit	Event Input Pin	Interrupt Output Pin
E0S1	EVENT 0	/S-IRQ1
E1S1	EVENT 1	
E2S1	EVENT 2	
E3S1	EVENT 3	
E0S0	EVENT 0	/S-IRQ0
E1S0	EVENT 1	
E2S0	EVENT 2	
E3S0	EVENT 3	

9.1.6. Event Control Register (Reg - 24 [h] / Bank 0)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
24	Event Control	C1	C0	T1	T0	○	MP	MS1	MS0

1) C1/C0 bit (Cycle 1/0)

C1/C0 bit can set up internal memory transfer cycle of event data.
When event signal is detected, it can record to internal memory by set up cycle.
When multiple events input are detected in one input pin within the same transfer cycle, only the first event is effective. Therefore, it is able to depress resolving power of event detection by setting up long cycle.
When supply initial power,[C1:1,C0:0 cycle 1s]is selected.

This setting up is common to all event input pins.

Memory transfer cycle

C1 (bit 7)	C0 (bit 6)	Cycle
0	0	250ms
0	1	500ms
1	0	1s
1	1	1min.

2) T1/T0 bit

T1/T0 bit can set up chattering cancel function of event input pin.
If event input is held for more than set up cycle, the event becomes effective.
When you set [T1=0, T0=0], Chattering cancel function stops.
When supply initial power,[T1:1,T0:0 cycle 62.5-125ms]is selected.
This setting up is common to all event input pins.
Chattering cancel cycle

T1 (bit 5)	T0 (bit 4)	Cycle
0	0	Function stops
0	1	31.2-62.5ms
1	0	62.5-125ms
1	1	125-250ms

3) MP bit

MP bit is a bit to control if continue event record or stop it.
When MP bit is 1, event record is stopped if address to record event is equal to address that was set up with event memory alarm.
When MP bit is 0, event record does not stop.

4) MS1/MS0 bit

This bit can control output interrupt of event memory alarm that is able to set up address with Address 27[h].
If MS1 bit is“ 1 ", /S-IRQ1 pin can output interrupt signal , and if MS1 bit is " 0 ", /S-IRQ1 pin can’t output interrupt signal .
If MS1 bit is“ 1 ", /S-IRQ0 pin can output interrupt signal , and if MS0 bit is " 0 ", /S-IRQ0 pin can’t output interrupt signal .

When supply initial power, all pins[”0”]are selected.

9.1.7. Memory Data Selection (Reg - 25 [h] / Bank 0)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
25	Memory Data Select	PN	Year	Month	Day	Week	Hour	Min.	Sec.

When an event was detected, can select it which data be recorded.
Set “1” to data to be recorded. This setting up is common to all event input ports.
Selected data is recorded in order of high-ranking data bit.
If many data of record are set up, memory is more consumed.

1) PN bit (Port Number)
If set PN bit, 1 byte record is executed with the following data component.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	1	1	1	VLOW	HL	Port1	Port0

" 1 " is recorded for bit 7-4.
VLOW (bit 3) record electric power condition (condition of VLOW) when event was detected.
HL (bit 2) record voltage level setting (value of HL0-3 bit) when event was detected.
Port1 (bit 1) and Port0 (bit 0) record detected event input pin with Binary. The relation between value of Port1& Port0 event input pin is as follows.

Event Input Pin	Port1 (bit 1)	Port0 (bit 0)
EVENT 0	0	0
EVENT 1	0	1
EVENT 2	1	0
EVENT 3	1	1

In case VLOW (bit 3) is " 1 ", event record data are not guaranteed.

9.1.8. Event Memory Address (Reg - 26 [h] / Bank 0)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
26	Event Memory Address	128	64	32	16	8	4	2	1

In reading mode, it is able to read address to be recorded event in the next time. (Final record address +1 address)
Event data start record from selected address, and run in cycles to Address 00 if over Address FF.
When input initial power,[Address:00]is selected.

9.1.9. Event Memory Alarm (Reg - 27 [h] / Bank 0)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
27	Event Memory Alarm	128	64	32	16	8	4	2	1

It is a register to detect that memory for event record is over prescribed data volume.
If MP bit (bit 2 of Address 24[h]) is " 0 ".
If record data reach address specified by event memory alarm, flag of MF is set up and consequently it is able to give interrupt output.
After that, event record operation is continued if event is detected.
Therefore, event record is continued even if memory alarm is given, and record is overwritten if any data is still remained in address.
If MP bit (bit 2 of Address 24[h]) is " 1 ".
If record data reach address specified by event memory alarm, flag of MF is set up and consequently it is able to give interrupt output.
And if record up to the final time digit specified by memory data selection, event record is stopped and ME0-3 bit become " 0 ".
It is able to start record of event again by writing “1” to ME0-3 bit after writing "0" to MF bit. Event record restart address is next of final address of former record.
Time stamp function is stop when it completed record up to the final time digit specified by memory data selection.
When supply initial power,[Address:7F]is selected.

9.1.10 Watchdog Timer (Reg - 29 [h] / Bank 0)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
29	Watch Dog Resister	WD3	WD2	WD1	WD0	WDP	○	○	WDE

Watchdog timer function has a 4 bit preset-down counter.
When WDE is set to " 1 ", this function becomes effective.
If counting value is “0” without input to WDI pin, WDF flag is set " 1 " and WDE bit is set” 0 ”.
In this case, /WDO pin can output interrupt signal.
Interrupt signal is automatically returned with clock cycle, which is specified by WDP bit.
It is able to start record of event again by writing “1” to WDE bit after writing "0" to WDF bit.
Set up clock cycle of countdown with WDP.
Set up presetting value of countdown within WD 0 - 3. When supply initial power,[WDE:0]is selected.

	WD3 (bit 7)	WD2 (bit 6)	WD1 (bit 5)	WD0 (bit 4)	Count down Presetting value
W / R	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

	WDP (bit 3)	Watchdog setting range	
		Min. Time [Presetting value =1] (Clock cycle)	Max. Time [Presetting value =15]
W / R	0	1.95ms	29.30ms
	1	31.25ms	468.75ms

An error with max.±1ms is caused.

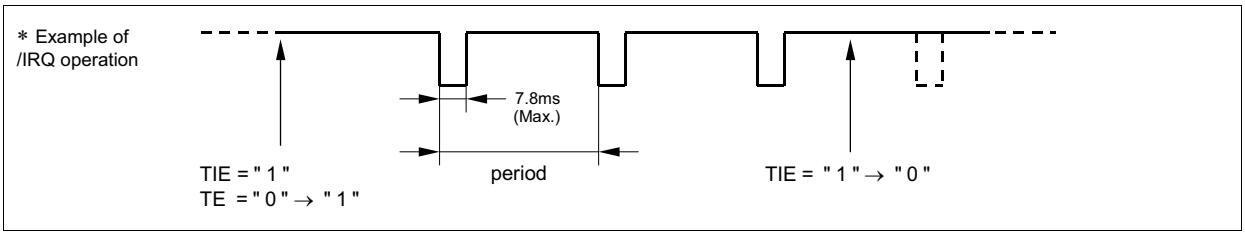
9.1.11. Interrupt flag register (Reg - 2A [h] / Bank 0)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
2A	Flag Register	EF3	EF2	EF1	EF0	○	WDF	BF	MF

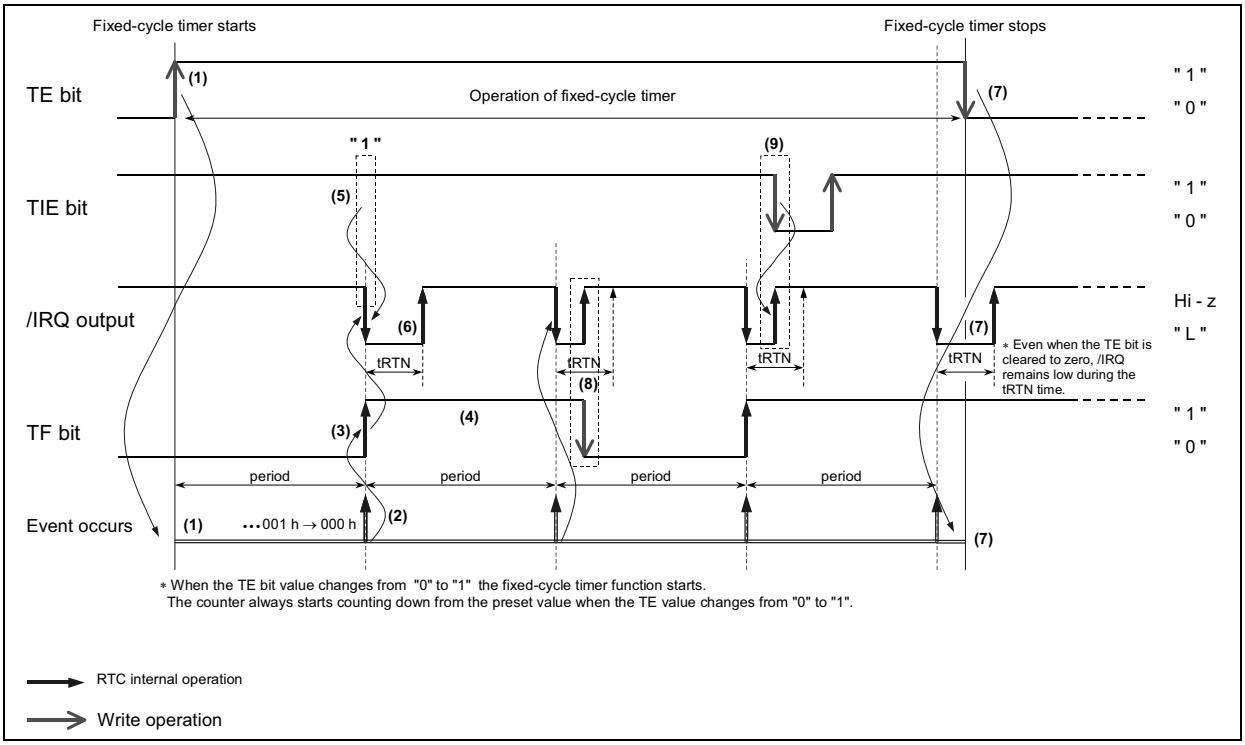
.

9.2. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, the /IRQ pin goes to low level and "1" is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /IRQ pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low-level to Hi-Z).



9.2.1. Diagram of fixed-cycle timer interrupt function



(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event that occurs when the count value changes from 001h to 000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleared to zero.

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /IRQ pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /IRQ pin output remains Hi-Z.

(6) Output from the /IRQ pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /IRQ is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /IRQ pin is set to Hi-Z status.
∗ When /IRQ = low, the fixed-cycle timer function is stopped. The tRTN period is the maximum amount of time before the /IRQ pin status changes from low to Hi-Z.

(8) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the TF bit value changes from "1" to "0".

(9) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

9.2.2. Related registers for function of fixed-cycle timer interrupt function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C	Timer Counter 1	•	•	•	•	**2048**	**1024**	**512**	**256**
0D	Control Register0	TEST1	WADA	USEL	**TE**	○	○	**TSEL1**	**TSEL0**
0E	Control Register1	VDET	VLOW	UF	**TF**	AF	○	VLF	PON
0F	Control Register2	TEST2	○	UIE	**TIE**	AIE	○	STOP	RESET

∗ Before entering operation settings, we recommend first clearing the TE bit to "0" and then clearing the TF and TIE bits to "0" in that order, so that all control-related bits are zero-cleared (= set to operation stop mode) to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – 0B to 0C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) TSEL1, TESL0 bits (Timer Select 1, 0)

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL1, 0	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN	Effects of STOP and RESET bits
W / R	0	0	4096 Hz /Once per 244.14 μs	122 μs	–
	0	1	64 Hz /Once per 15.625 ms	7.813 ms	
	1	0	1 Hz /Once per second	7.813 ms	
	1	1	1/60 Hz /Once per minute	7.325 ms	∗ Does not operate when the STOP bit value is "1".

∗1) The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

∗2) An interrupt that occurs when the source clock is in 1/60 Hz mode is linked to the internal clock's "minute" update operation.

2) Down counter for fixed-cycle timer (Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set. The counter counts down based on the source clock's period, and when the count value changes from 001h to 000h, the TF bit value becomes "1".
The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value. Be sure to write "0" to the TE bit before writing the preset value. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

Address 0C Timer Counter 1								Address 0B Timer Counter 0							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
•	•	•	•	2048	1024	512	256	128	64	32	16	8	4	2	1

∗ By the status of TE-bit, contents changes when reads these register.

TE bit	Description
" 0 " ∗ Stops fixed-cycle timer interrupt function.	The default (preset) value can be checked by reading this register.
" 1 " ∗ Starts fixed-cycle timer interrupt function.	The status during a countdown can be checked by reading this register. ∗ However, since the read data is not held (the data may be changing), to obtain accurate data the countdown status should be read twice and then compared.

∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – 0B to 0C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

3) TE bit (Timer Enable)

When TE bit is "0", the default (preset) can be checked by reading this register.

TE	Data	Description
Write / Read	0	Stops fixed-cycle timer interrupt function. * Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-Z).
	1	Starts fixed-cycle timer interrupt function. * The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

If it was already cleared to zero, this value changes from "0" to "1" when an event occurs, and the new value is retained.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-Z).
	1	This bit is invalid after a "1" has been written to it.
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when a fixed-cycle timer interrupt event has occurred.

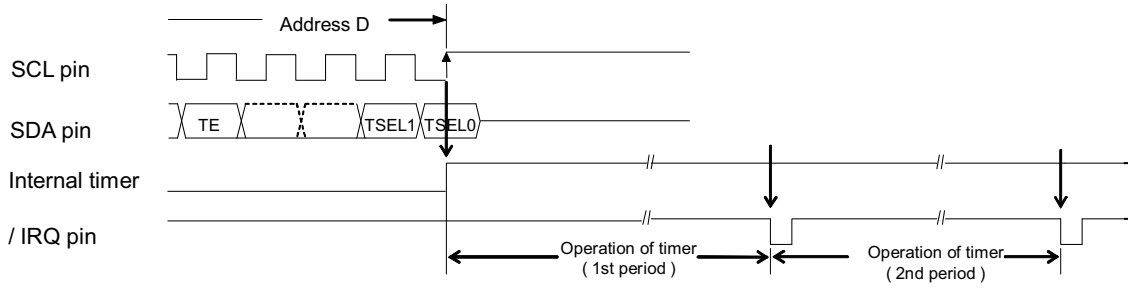
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.

When a "0" is written to this bit, output from the /IRQ pin is prohibited (disabled).

TIE	Data	Description
Write / Read	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-Z). * Even when the TIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low).

9.2.3. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the falling edge of the CLK signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).



9.2.4. Fixed-cycle timer interrupt interval (example)

The combination of the source clock settings (settings in TSEL1 and TSEL0) and fixed-cycle timer countdown setting (Reg−0B to Reg-0C setting) sets the fixed-cycle timer interrupt interval, as shown in the following examples.

Timer Counter setting	Source clock			
	4096 Hz TSEL1,0 0 , 0	64 Hz TSEL1,0 0 , 1	1 Hz TSEL1,0 1 , 0	1/60 Hz TSEL1,0 1 , 1
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

- Fixed-cycle timer interrupt time error and fixed-cycle timer interrupt interval time

A fixed-cycle timer interrupt time error is an error in the selected source clock's $^{+0}/_{-1}$ interval time. Accordingly, the fixed-cycle timer interrupt's interval (one cycle) falls within the following range in relation to the set time.

Fixed-cycle timer interrupt's interval

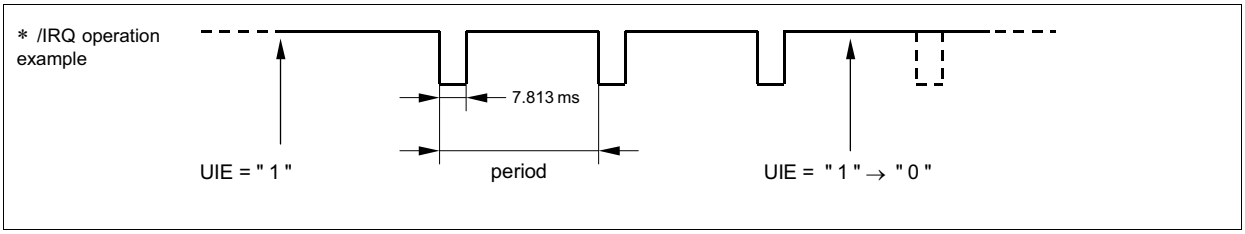
(Fixed-cycle timer interrupt's set time(∗) − source clock interval) to (fixed-cycle timer interrupt set time)

∗) Fixed-cycle timer interrupt's set time = Source clock setting × Countdown timer setting for fixed-cycle timer

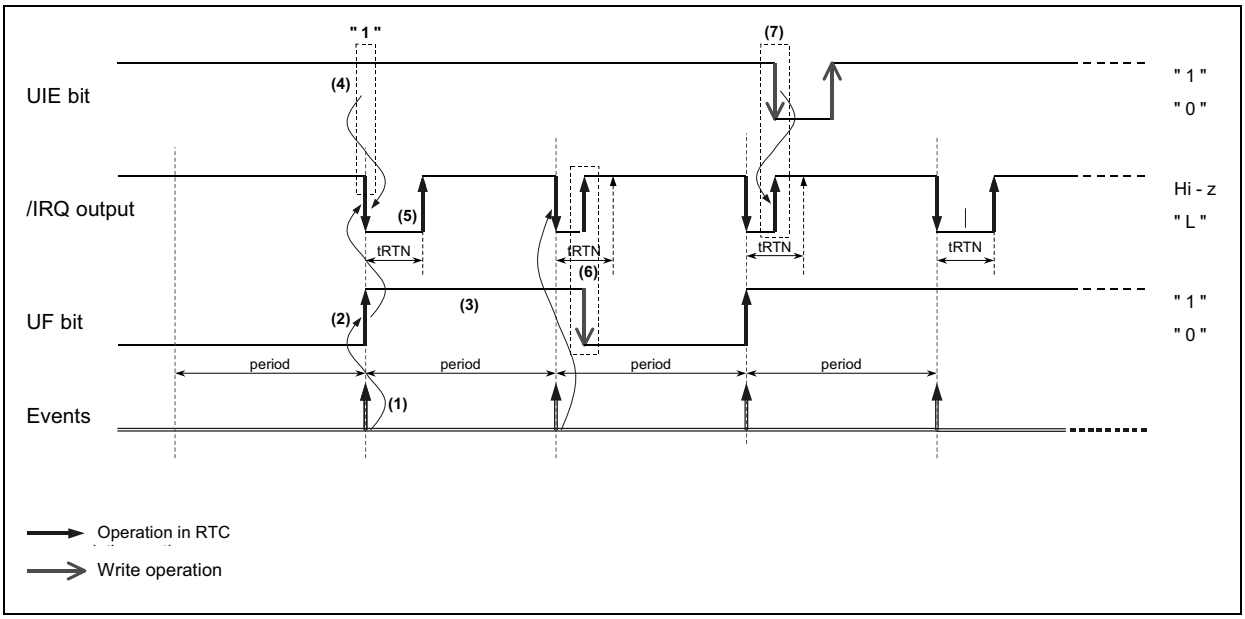
∗ The time actually set to the timer is adjusted by adding the time described above to the communication time for the serial data transfer clock used for the setting.

9.3. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) 7.8 ms (fixed value) after the interrupt occurs.



9.3.1. Time update interrupt function diagram



(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.
* But, actually, it is an interrupt that occurs when the source clock is in second update mode is not linked to the internal clock. (Instead, a dedicated 1 Hz timer circuit is used for independent operation.)

(2) When a time update interrupt event occurs, the UF bit value becomes "1".

(3) When the UF bit value is "1" its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /IRQ pin output is low if UIE = "1".
* If UIE = "0" when a timer update interrupt occurs, the /IRQ pin status remains Hi-Z.

(5) Each time an event occurs, /IRQ pin output is low only up to the tRTN time (which is fixed as 7.1825 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
* /IRQ pin output goes low again when the next interrupt event occurs.

(6) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the UF bit value changes from "1" to "0".

(7) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

9.3.2. Related registers for time update interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Control Register0	TEST1	WADA	USEL	TE	○	○	TSEL1	TSEL0
0E	Control Register1	VDET	VLOW	UF	TF	AF	○	VLF	PON
0F	Control Register2	TEST2	○	UIE	TIE	AIE	○	STOP	RESET

∗ Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" time update interrupt events do not occur.

∗ Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /IRQ pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write / Read	0	Selects "second update" (once per second) as the timing for generation of interrupt events ∗ But, actually, it is an interrupt that occurs when the source clock is in second update mode is not linked to the internal clock. (Instead, a dedicated 1 Hz timer circuit is used for independent operation.)
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-Z) when an time update interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Time update interrupt events are not detected.
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

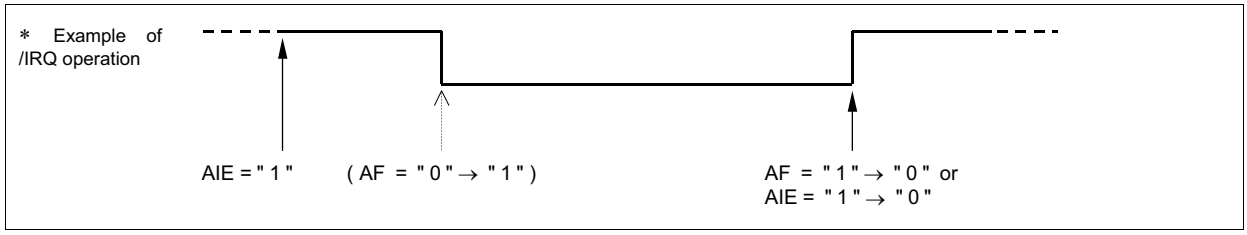
3) UIE bit (Update Interrupt Enable)

When a time update interrupt event occurs (UF bit value changes from "0" to "1"), this bit selects whether to generate an interrupt signal (/IRQ status changes from Hi-Z to low) or to not generate it (/IRQ status remains Hi-Z).

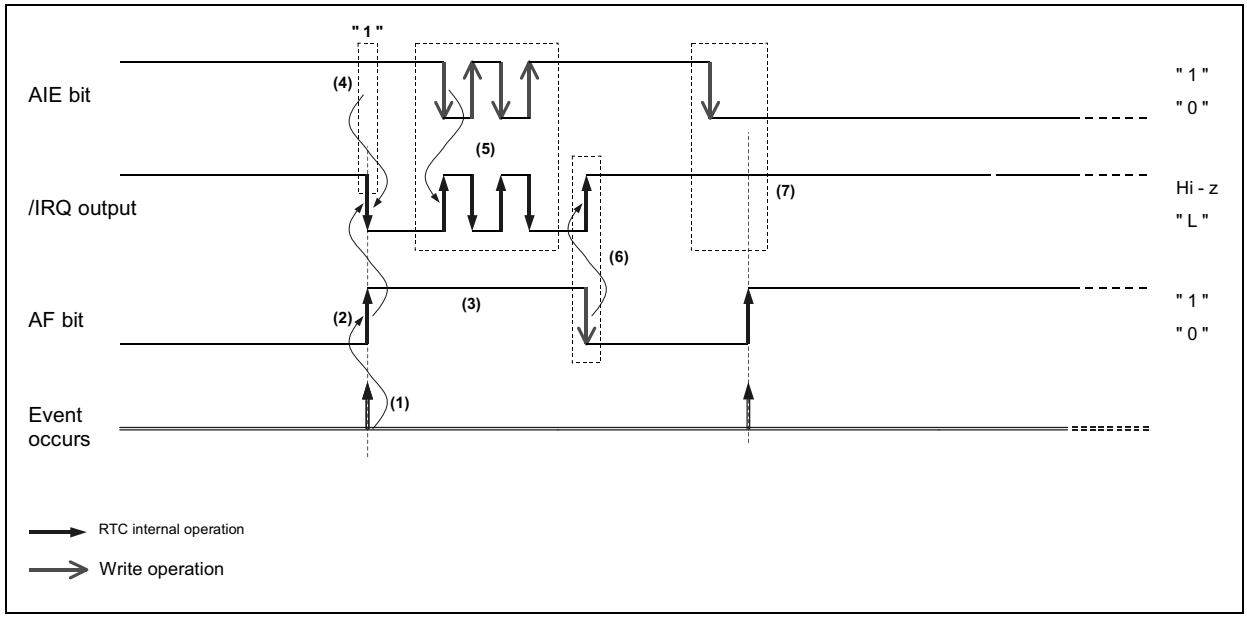
UIE	Data	Description
Write / Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs (/IRQ remains Hi-Z) 2) Cancels interrupt signal triggered by time update interrupt event (/IRQ changes from low to Hi-Z). ∗ Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-Z) when an time update interrupt event has occurred.
	1	When a time update interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). ∗ When a time update interrupt event occurs, low-level output from the /IRQ pin occurs only when the UIE bit value is "1". Up to 7.8 ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low to Hi-Z).

9.4. Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.



9.4.1. Diagram of alarm interrupt function



(1) The hour, minute, date or day when an alarm interrupt event is to occur is set in advance along with the WADA bit, and when the setting matches the current time an interrupt event occurs.
(Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /IRQ pin output goes low.
* When an alarm interrupt event occurs, /IRQ pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /IRQ is low, the /IRQ status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /IRQ status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /IRQ is low, the /IRQ status immediately changes from low to Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /IRQ pin status remains Hi-Z.

9.4.2. Related registers for Alarm interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01	MIN	○	40	20	10	8	4	2	1
02	HOUR	○	○	20	10	8	4	2	1
03	WEEK	○	6	5	4	3	2	1	0
04	DAY	○	○	20	10	8	4	2	1
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D	Control Register0	TEST1	WADA	USEL	TE	○	○	TSEL1	TSEL0
0E	Control Register1	VDET	VLOW	UF	TF	**AF**	○	VLF	PON
0F	Control Register2	TEST2	○	UIE	TIE	**AIE**	○	STOP	RESET

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ When the AIE bit value is "1" and the Alarm registers (Reg - 08h to 0Ah) is being used as a RAM register, /IRQ may be changed to low level unintentionally.

1) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write / Read	0	Sets WEEK as target of alarm function (DAY setting is ignored)
	1	Sets DAY as target of alarm function (WEEK setting is ignored)

2) Alarm registers (Reg – 08[h] to 0A[h])

The hour, minute, date or day when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg - A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /IRQ pin goes low.

∗ The register that "1" was set to "AE" bit, doesn't compare alarm.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - A):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only an hour and minute accords with alarm data.

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-Z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

When an alarm interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/IRQ status changes from Hi-Z to low) or is not generated (/IRQ status remains Hi-Z).

AIE	Data	Description
Write / Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-Z). * Even when the AIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). * When an alarm interrupt event occurs, low-level output from the /IRQ pin occurs only when the AIE bit value is "1". This value is retained (not automatically cleared) until the AF bit is cleared to zero.

9.4.3. Examples of alarm settings

1) Example of alarm settings when "Day" has been specified (and WADA bit = "0")

Day is specified WADA bit = "0"	Reg – A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	HOUR Alarm	MIN Alarm
Monday through Friday, at 7:00 AM * Minute value is ignored	0	0	1	1	1	1	1	0	07 h	80 h ~ FF h
Every Saturday and Sunday, for 30 minutes each hour * Hour value is ignored	0	1	0	0	0	0	0	1	80 h ~ FF h	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Reg - A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	HOUR Alarm	MIN Alarm
First of each month, at 7:00 AM * Minute value is ignored	0	0	0	0	0	0	0	1	07 h	80 h ~ FF h
15th of each month, for 30 minutes each hour * Hour value is ignored	0	0	0	1	0	1	0	1	80 h ~ FF h	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

9.5. Detection of External Event and Time Stamp Function

It is functions to detect event signal that is input to max. 4 input pins and transfer selected clock data to internal memory with arbitrarily transfer cycle. This function detect rise up or fall down (selectable) of signal, and it is disregarded if holding time of signal is less than chattering cancel cycle. Event in one port within the same memory transfer cycle is recorded as one event. Don't access to RTC register during transfer memory of event data.

9.5.1. Interrupt output function & Flag Register

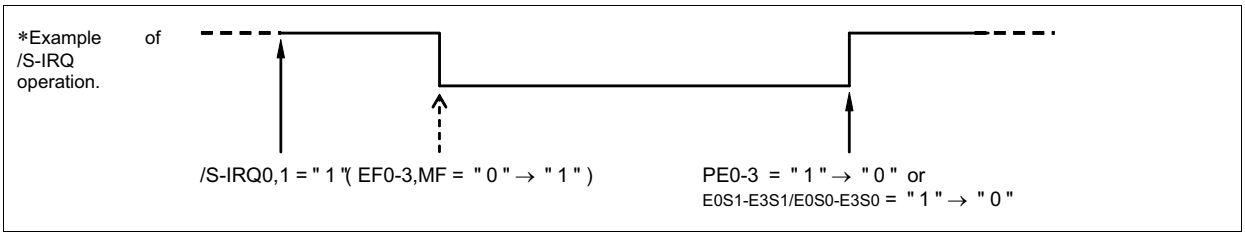
When detect event, EF0-3bit is set to " 1 " , so that you know event occurrence, and /S-IRQ0, 1 pin can output by setting (E0S1-E3S1,E0S0-E3S0bit).

And if memory for event record is over specified data volume, MF bit is set to " 1 ", and /S-IRQ0,1 pin can output by setting (MS1, MS0 bit).

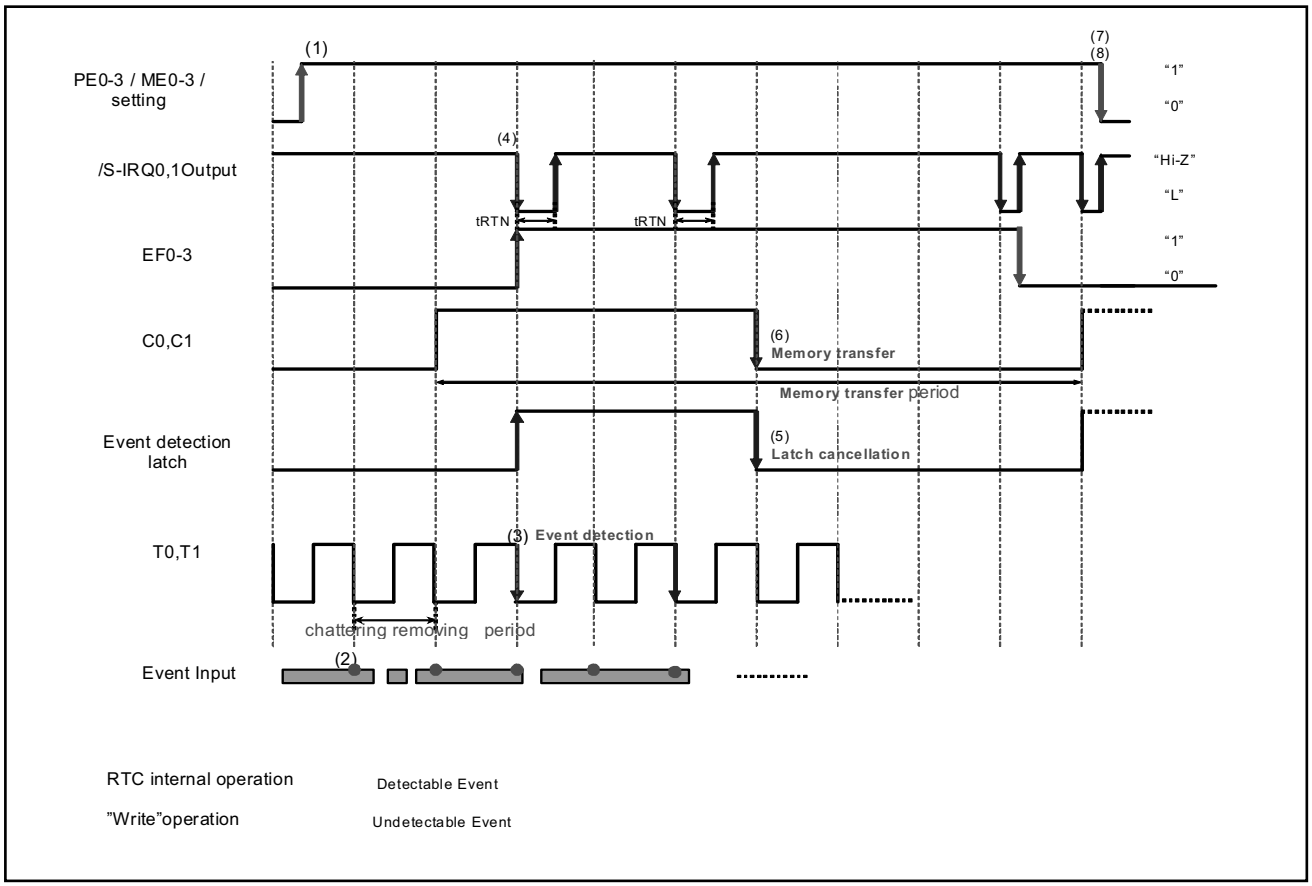
EF0-3 and MF bit hold the results until "0 " cleared.

∗ Output of /S-IRQ0,1 =" L " after giving interrupt event is automatically cancelled (/s-IRQ0.1 = "L" → Hi-z) with 7.813ms (fixed value) after interrupting.

It is also possible to cancel Interupt output by writing PE0-3,EF0-3,MF,E0S1-E3S1/E0S0-E3S0 bit = " 0 ".



9.5.2. Event detecting function diagram



(1) It is able to detect event of each event input pin by setting PE0-3 bit to " 1 ". And it is able to record event data in internal memory by setting ME0-3 bit to " 1 ".

(2) If event input condition is holded over 2 continuous fall edges of chattering cancel clock, input of event is detected. Chattering cancel cycle can be selected with T0, T1bit.

(3) If event input is detected, detection result is latched. If event is detected during a latch, it is recorded as one event, but interrupt output is detected every event detection.

(4) If interrupt output is set to /S-IRQ0,1, EF0-3bit is set to " 1 " and detection of event input and interrupt signal is given.

/S-IRQ0,1 output "L" only during tRTN time (when event interrupt is output, it is fixed to 7.813ms) at every event, and then it is automatically cancelled to Hi-z.

(5) Memory transfer preparation is started with fall edge of memory transfer clock. Clock data on that time is transferred to memory after **62.5ms from its edge.** Memory transfer clock is able to select memory transfer clock with C0, C1 bit.

(6) Event signal latched in (3) is cancelled after latching from preparation of memory transfer to start of memory transfer in (5). After cancellation, it comes to stand by condition for next event.

(7) If write of PE,"1" →"0" is done during /S-IRQ0,1 = " L ", it is switched to /S-IRQ0,1 = " L " → Hi-z.

(8) If write of E0S1-E3S1/E0S0-E3S0, " 1 " → " 0 " is done during /S-IRQ0,1 = " L ", it is switched to /S-IRQ, " L " → Hi-z.

*If event detection is done at the same time as multiple event input pins, memory is transferred in order of pin number from smallest to biggest. In this case, all event data are recorded the same time.

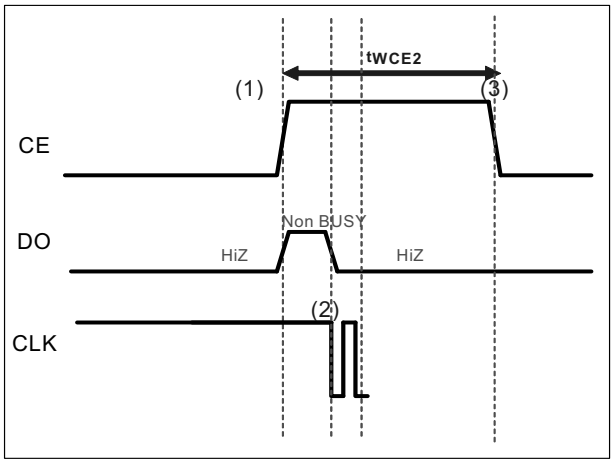
9.5.3. RTC access during event record

It is impossible to access to internal register during memory transfer of event data. And if access to RTC register is done during memory transfer of event data, BF bit is set to "1". By confirming DO pin output when set to CE="H", it is able to confirm that it is in operation to transfer memory. There is setting up time (=In-BUSY) with 62.5 ms before start transfer of event data, and after that data transfer is started.

In addition to setup time, it needs 25ms for one input port to transfer one time of event. If detect event with 4 input port at the same time, approx. 100ms is needed.

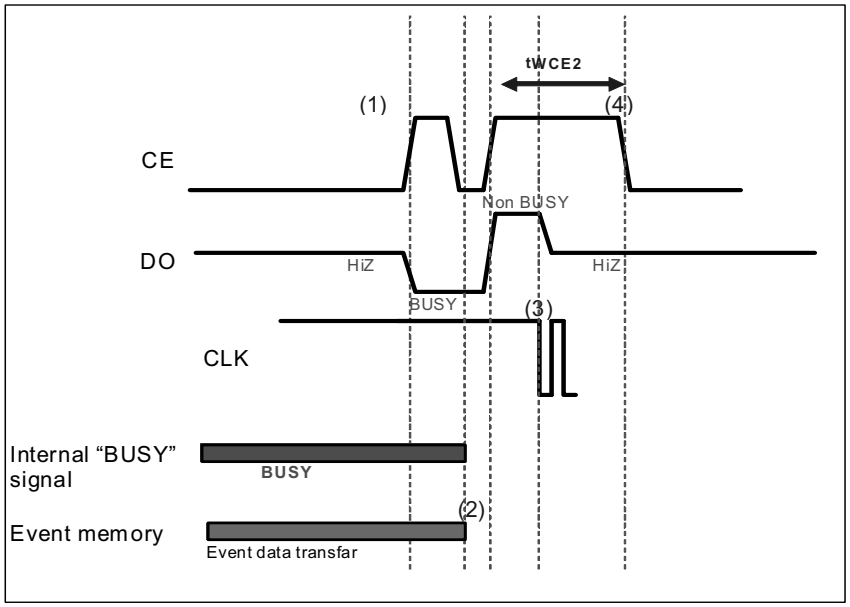
(1) When set to CE="H", In case of DO pin output ="H"(Non BUSY)
RTC is not in transfer of event memory, it is able to access to RTC register. (Non-BUSY condition).

In case of Non BUSY, user is requested to finish RTC access within $t_{WCE2.}$(Please make finish up to CE="L").



1. When CE="H", RTC is not in transfer of event memory, it output DO="H".
2. With the first fall down edge of CLK, cancel DO pin output ="H"and comes to HiZ.
→ Please execute access to RTC.
3. Make finish access with CE="L". W/R is guaranteed by completion CE="H"→ ""L" within $t_{WCE2.}$

(2)When set to CE="H", In case of DO pin output ="L"(BUSY)
RTC is in transfer of event memory, so user cannot execute RTC access. (BUSY-condition).
After you set CE=L, Please repeat the input to CE till a Busy condition is finished.

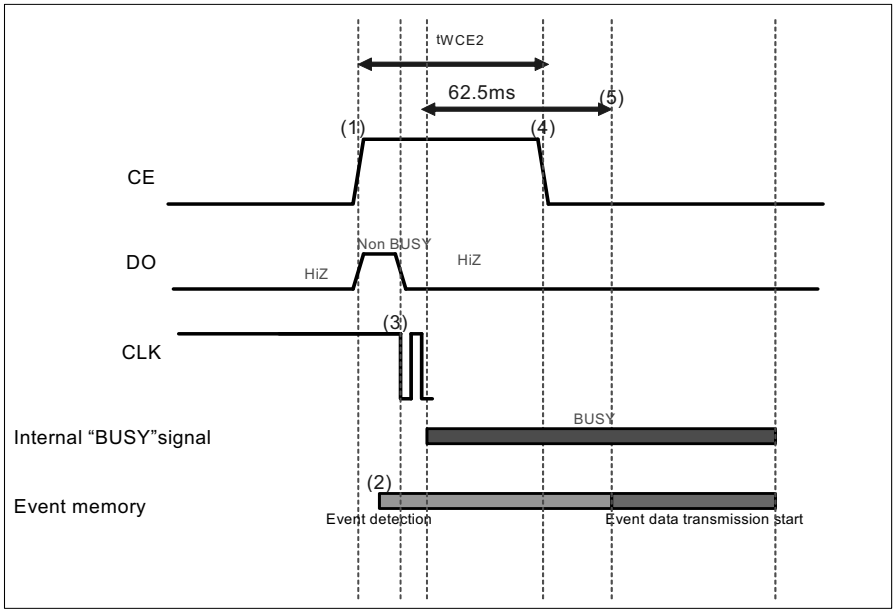


1.When CE="H", RTC is in transfer of event memory, therefore output DO="L".
2.Output of DO pin is held during CE="H", and DO pin is opened by returning DO pin →CE="L"and comes to HiZ. Change over input of CE pin repeatedly until access BUSY confirmation result comes to DO="H" and confirm. If memory transfer is finished, it comes to access BUSY condition→Non BUSY condition, and if set to CE="H" in this time, DO="H" is output.
3. Cancel DO pin output = "H" with the first shut down edge of CLK and comes to HiZ.
→ Execute access to RTC.
4. Make finish access with CE="L". W/R is guaranteed by completion of access within $t_{WCE2.}$

(3)When set to CE="H", In case of change to internal BUSY condition during access with DO pin ="H".

1, When CE="H", RTC is not in transfer of event memory, it output DO="H".
2, Event input pin detects event and latches the result.
3, Cancel DO pin output = "H" with the first fall down edge of CLK, and comes to HiZ.
→ Execute access to RTC.
4, Access is finished with CE="L". W/R is guaranteed by completion of sccess within $t_{WCE2.}$
5, Access BUSY signal is output 62.5ms before event memory transfer.

*During event memory transfer, RTC internal bus is monopolized for event memory.



Instructions about RTC access during an event record

When an event record sequence (event data transmission to memory) and access to RTC occur at the same time and occurred, inside bus is monopolized for event record sequences with this IC, and an event record sequence is given priority. Access to RTC is stopped forcibly then by internal control.
In this state, you can input a signal into an external terminal(CE,CLK,DI).Therefore, when you input a signal, an input signal seems to be accepted, but actually access to RTC is not carried out inside by a control signal because access to RTC is a state intercepted forcibly.

You can know state (BUSY or Non BUSY) of an event record sequence by the input to a CE pin before starting access to RTC.
In the case of DO pin output = Low, there is a possibility that access to RTC (Read / Write) is not performed.
You can confirm an end state of access to RTC by reading BF bit.
In the case of BF = 0, access to RTC is completed normally.
In the case of BF=1, access to RTC and an event record sequence occurred at the same time.
Access to RTC is terminated abnormally.

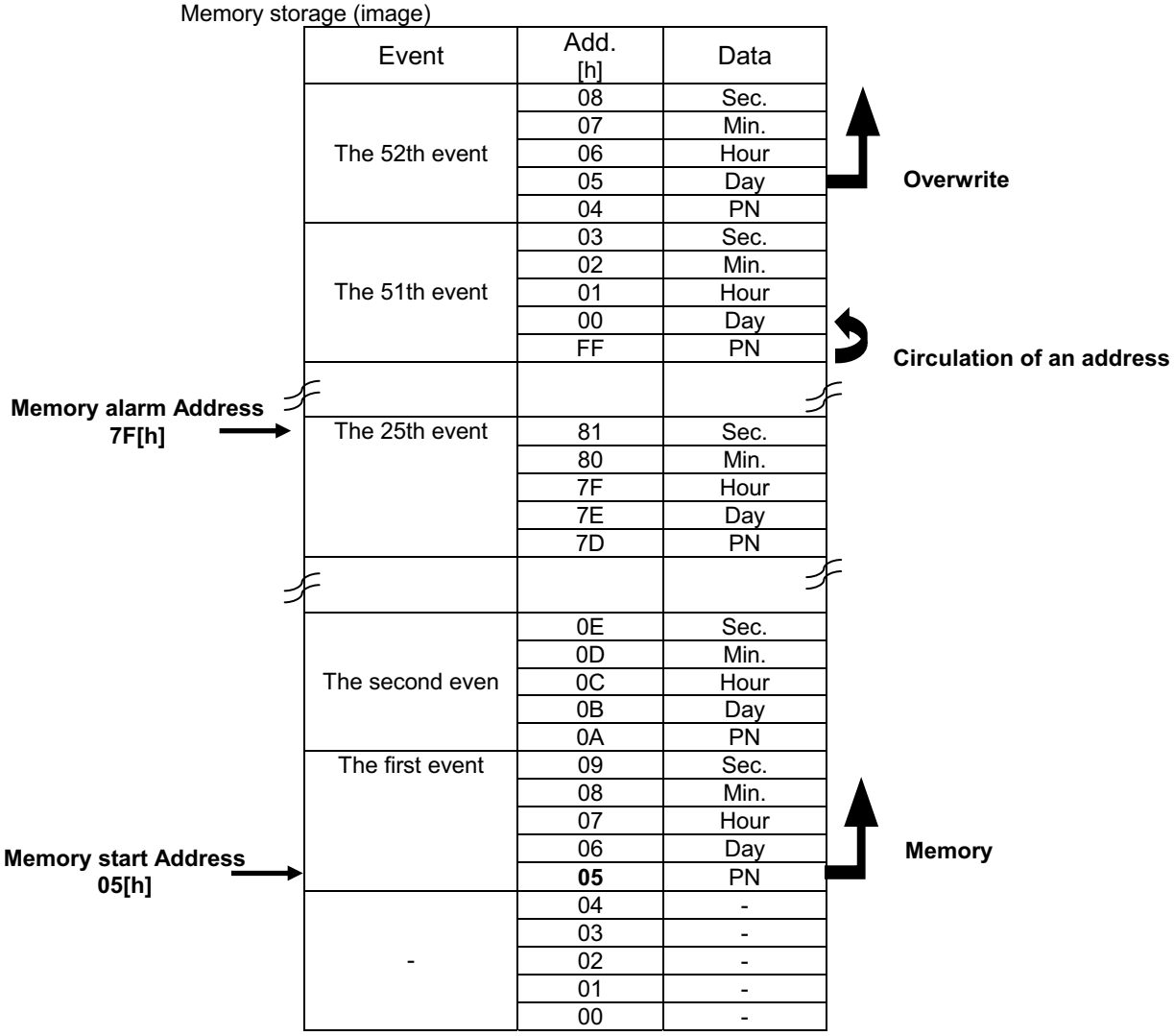
You carry out access to RTC again, and please confirm states of RTC data.
When you access it once again from the state that access to RTC became the forced end, please refer to the following content.
1) Practice of a access to RTC end sequence
Please carry out a access processing sequence as [CE =High(Enable) ⇒ Low(Disable)] between CLK = High states.
2) Practice of a access to RTC start sequence
Please carry out a [CE=Low(Disable) ⇒ CE=High(Enable)] ,and please start a CLK signal, and DI signal input.

Access data become a decision / availability by a timing of rise of eight clock of 8bit serial transfer. Therefore, it is valid data when you invited rise of eight clocks before access to RTC occurs with an event record sequence.
However, before rise of eight clocks, when an event record sequence and access to RTC occurred at the same time, the data become invalid so that access to RTC is intercepted at that point.

9.5.4. Example of event record
Register setting
In case of MP bit (Address 24[h], bit 2) " 0 "
Setting of Memory data selection (10010111: PN-Day-Hour-Min.-Sec.)
Setting of event memory address (05[h])
Setting of memory alarm (7F[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
25	Memory Data Slect	**PN**	Year	Month	**Day**	Week	**Hour**	**Min.**	**Sec.**
26	Memory Address	128	64	32	16	8	**4**	2	**1**
27	Memory Alarm	128	**64**	**32**	**16**	**8**	**4**	**2**	**1**

Memory storage (image)



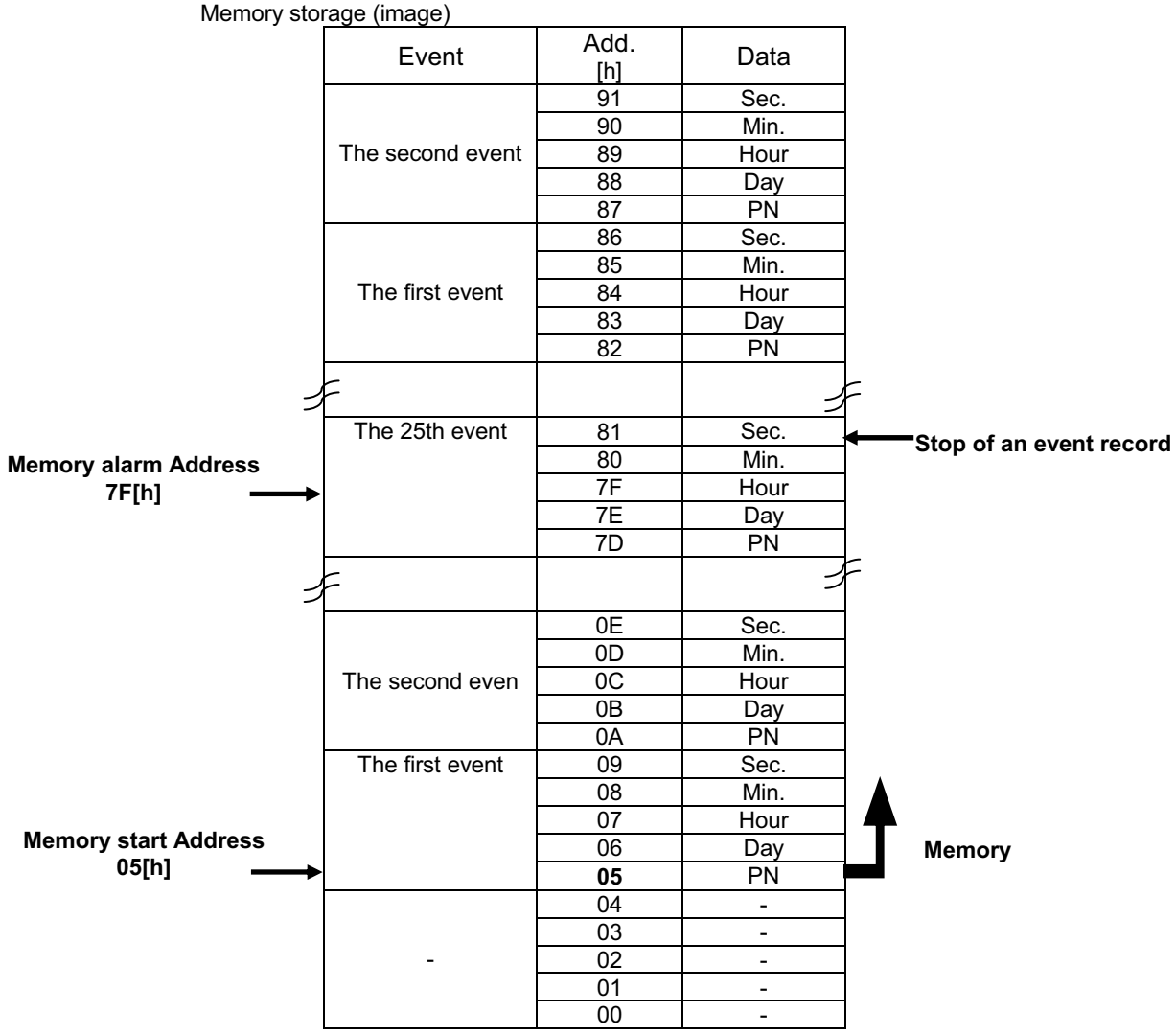
Event	Add. [h]	Data
The 52th event	08	Sec.
	07	Min.
	06	Hour
	05	Day
	04	PN
The 51th event	03	Sec.
	02	Min.
	01	Hour
	00	Day
	FF	PN
The 25th event	81	Sec.
	80	Min.
	7F	Hour
	7E	Day
	7D	PN
The second even	0E	Sec.
	0D	Min.
	0C	Hour
	0B	Day
	0A	PN
The first event	09	Sec.
	08	Min.
	07	Hour
	06	Day
	05	PN
-	04	-
	03	-
	02	-
	01	-
	00	-

Memory is stored in order of high-ranking bit (PN) of specified event data. Address is started from “05[h] and an automatic increment is done every data record.
Automatic increment of address is cycled and address“00[h]”is come after address“FF[h]”.
If data is stored in address “7F[h]”, memory flag (MF) become to“1”. If MS0,1 bit is set to ”1”, it is able to give interrupt output from /S-IRQ0,1 pin.
If data is already stored in object address when data is recorded, it is overwritten and new recorded event data is stored.

Register setting
In case of Mpbit (Address24[h], bit 2) " 1 "
Setting of Memory data selection (10010111:PN-Day-Hour-Min.-Sec.)
Setting of event memory address (05[h])
Setting of memory alarm (7F[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
25	Memory Data Slect	**PN**	Year	Month	**Day**	Week	**Hour**	**Min.**	**Sec.**
26	Memory Address	128	64	32	16	8	**4**	2	**1**
27	Memory Alarm	128	**64**	**32**	**16**	**8**	**4**	**2**	**1**

Memory storage (image)

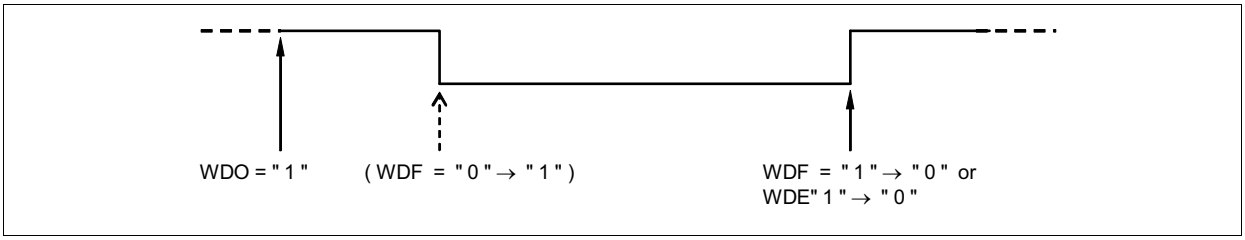


Memory is housed in order of high-ranking bit (PN) of specified event data. Address is started from “05[h] and an automatic increment is done every data record.
Automatic increment of address is cycled and address“00[h]”is come after address“FF[h]”.
If data is housed in address “7F[h]”, memory flag (MF) is set to“1”. If MS0,1 bit is set to ”1”, it is able to give interrupt output from /S-IRQ0,1 pin.
If data is housed in object address when data is recorded, it is overwritten and new recorded event data is housed.

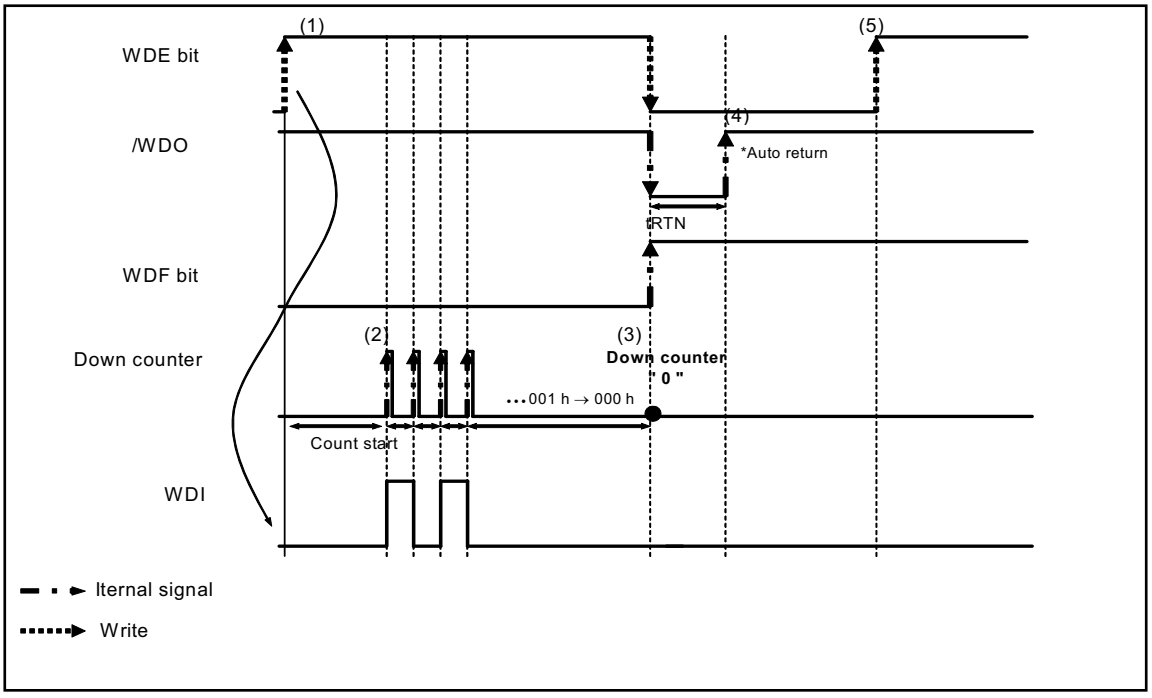
9.5.5. Power system of event input pin.
Event input pin is operated by time Stamp function operation voltage “VCH”.
VCH comes to electric potential of VDD or higher VBK.

9.6. Watchdog Function

This function is detecting stop more than arbitrarily time, and WDF bit becomes to " 1 " and WDO pin = " L ".
Interrupt signal of WDO pin is automatically cancelled (WDO = " L " → Hi-z) by clock cycle specified with WDP bit. And it is also possible to cancel output by write of WDF bit, WDE bit = " 0".
Watchdog function is only effective when this module is operated with VDD voltage. If VBK voltage operation due to dropping of VDD voltage start, WDE bit becomes to " 0 " at the same time as VDET=" 1 ". In case of return to VDD voltage operation, it is necessary to set up WDE bit again. In case of resetting WDE bit, down counter is reset and countdown is started from preset value in advance.



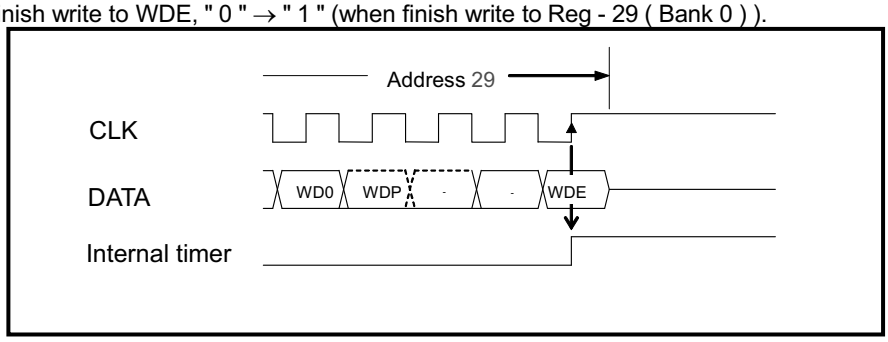
9.6.1. Watchdog functional diagram



(1) By write of WDE, " 0 " → " 1 " , start countdown of down counter from preset value.
(2) Make count value of downcounter countdown with a source clock cycle, and interrupt signal is output when downcount reaches 001h → 000h. If there is clock input to WDI pin before " 0 " borrow, counter value is reset and restart countdown from preset value.
(3) If downcounter is " 0 " borrow, it comes to WDF bit =" 1 " and WDO pin = " L ". WDF bit hold the result until "0" cleared.
(4) WDO pin output is automatically cancelled (" L " → Hi-z) after clock cycle (tRTN) specified by WDP bit.
When WDO pin = " L " , execute write of WDF bit= " 0" or WDE bit =" 0 " , output is immediately cancelled.
(5) After setting WDF=" 0 ", please set WDE=" 1 " to let a function restart.

9.6.2. Watchdog start timing

Time countdown of watchdog function is started from CLK starting up edge (when finish bit 0 communication) when finish write to WDE, " 0 " → " 1 " (when finish write to Reg - 29 (Bank 0)).

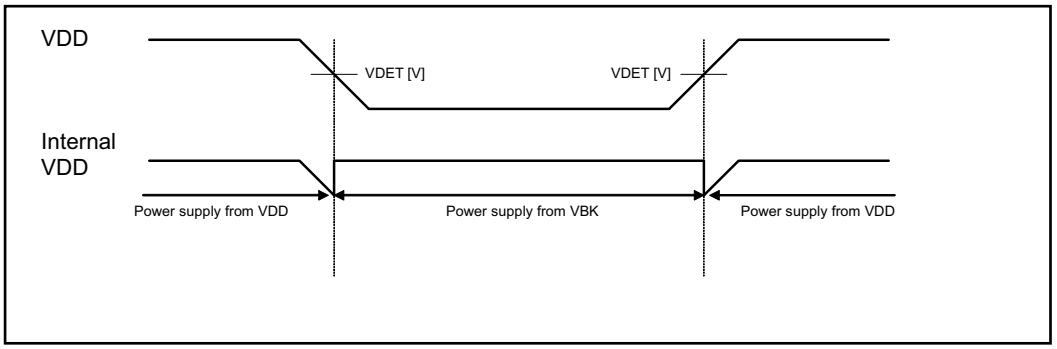


9.7. Main Power/backup Power Change Over Function

Power voltage is always checked, and if VDD voltage value is higher than VDET set value, electric potential is supplied from main power (VDD). If VDD voltage value is lower than VDET set value, electric potential is supplied from backup power (VBK).

To prevent wrong operation, hysteresis is given to VDET set value. When start up VDD, VDET voltage threshold is increased for hysteresis(ca. 50mV).

Power change circuit is always operated by VDD system power. If VDD voltage value comes lower than 1.60V, normal operation is not guaranteed.

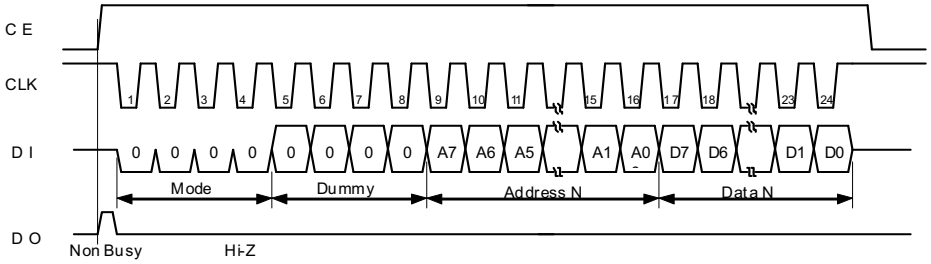


9.8. Read/Write of data

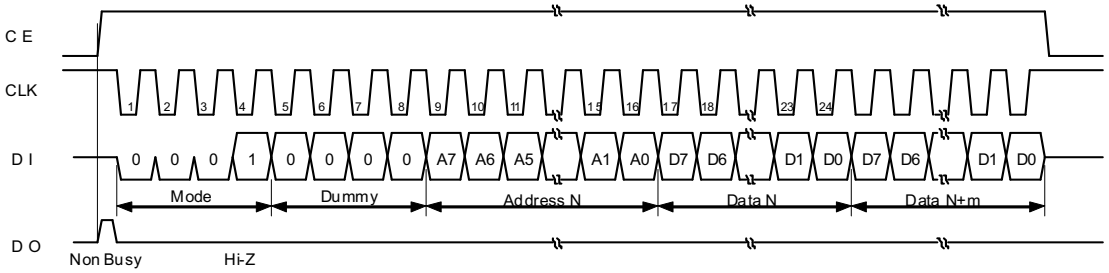
For both read and write, first set up chip condition (internally CE="H") to CE0="H" and CE1="H", then specify the 8-bits address, and finally read or write in 8-bits units.
Both read and write use MSB-first. In continuous operation, objected address is auto incremented.
Auto incrementing of the address is cyclic, so address " FF hex " is followed by address "0".

9.8.1. Write of data

1) One-shot writing



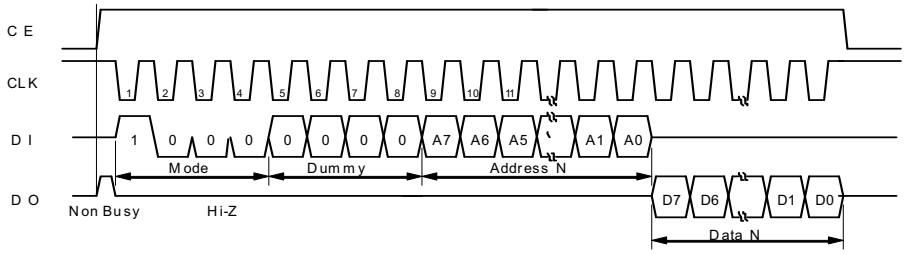
2) Continuous writing



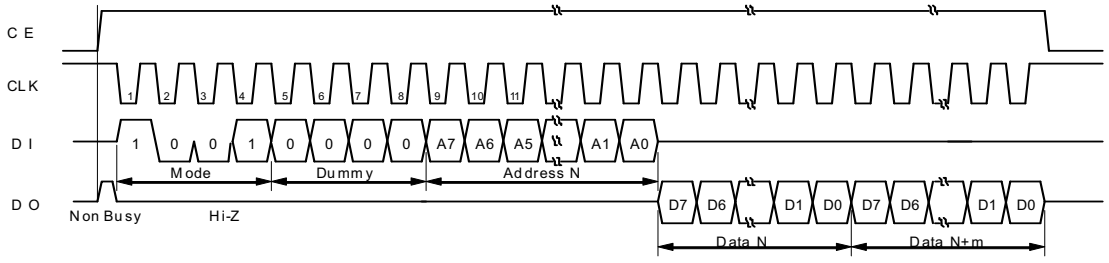
*When writing data, the data needs to be entered in 8-bits units.
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

9.8.2. Read of data

1) One-shot reading



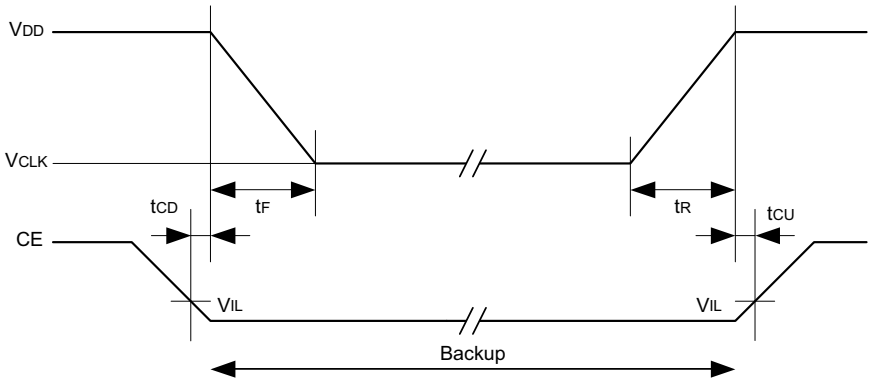
2) Continuous reading



9.8.3. Read / Write mode setting cord

Mode	Bank 0	Bank 1
Read	8 h	9 h
Write	0 h	1 h

9.9. Shifting to backup and returning



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CE time before power drop	tCD	-	0			µs
Power drop time	tF	-	2			µs/ V
Power rise time	tR	-	1			µs/ V
CE time after power rise	tCU	-	0			µs

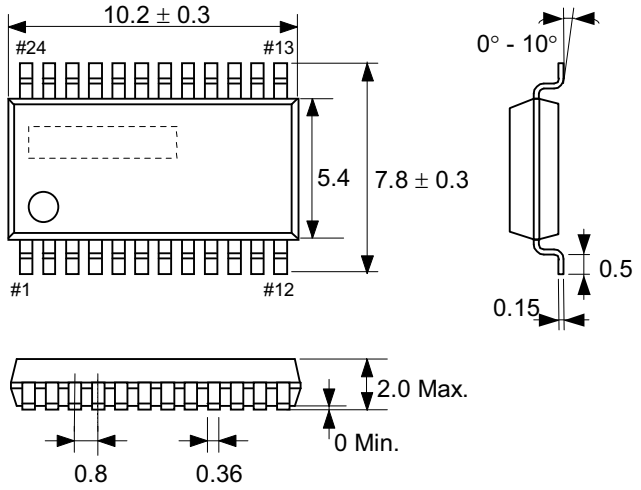
* When RTC switch into the backup-mode, CE keeps low level sure and, set the RTC into a disable state.

10. External dimension / Marking layout

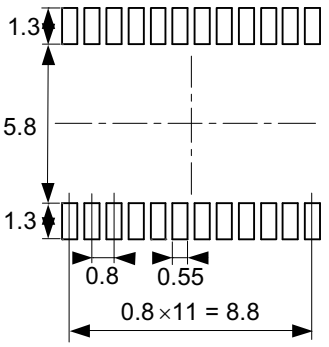
10.1. External dimensions

RX – 5412F

• External dimensions



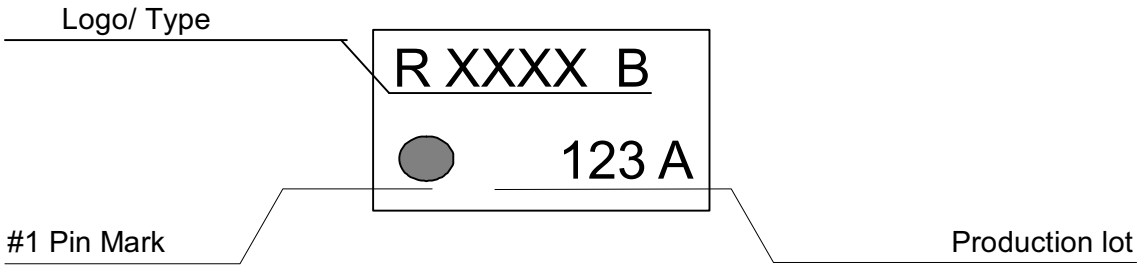
• Recommended soldering pattern



Unit : mm

10.2. Marking layout

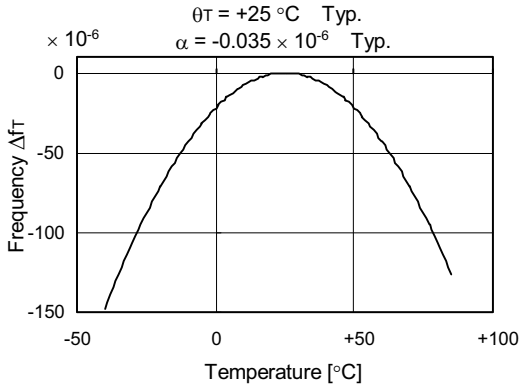
RX – 5412SF



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

11. Reference data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha\ (\theta_T - \theta_X)^2$

Δf_T		: Frequency deviation in any temperature
α	($1 / °C^2$)	: Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6} / °C^2$
θ_T	(°C)	: Ultimate temperature (+25±5 °C)
θ_X	(°C)	: Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

$\Delta f/f$	: Clock accuracy (stable frequency) in any temperature and voltage
$\Delta f/fo$	: Frequency precision
Δf_T	: Frequency deviation in any temperature
Δf_V	: Frequency deviation in any voltage

3. How to find the date difference

Date difference = $\Delta f/f \times 86400$ (seconds)

* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

EPSON TOYOCOM

Application Manual

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