ETM29E-01

EPSON TOYOCOM

Application Manual

Real Time Clock Module

RX-8571NB

EPSON TOYOCOM CORPORATION

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Contents

LOW BACKUP CURRENT
I²C-BUS -INTERFACE REAL TIME CLOCK MODULE

RX – 8571 NB

- Built-in 32.768-kHz crystal resonator (with controlled frequency precision).
- Interface type : I²C-BUS
- Interface voltage range : 1.6 V to 5.5 V
- Voltage when during hold (timer hold) : 1.3 V to 5.5 V
- Low current consumption during backup : 200 nA (Typ.) / 3 V
- 32.768-kHz output function with output control : C-MOS output With Control Pin
- User register : Built in 128 bit RAM
- Real-time clock function
  Clock/calendar function, auto leap year correction function, alarm interrupt function, etc.

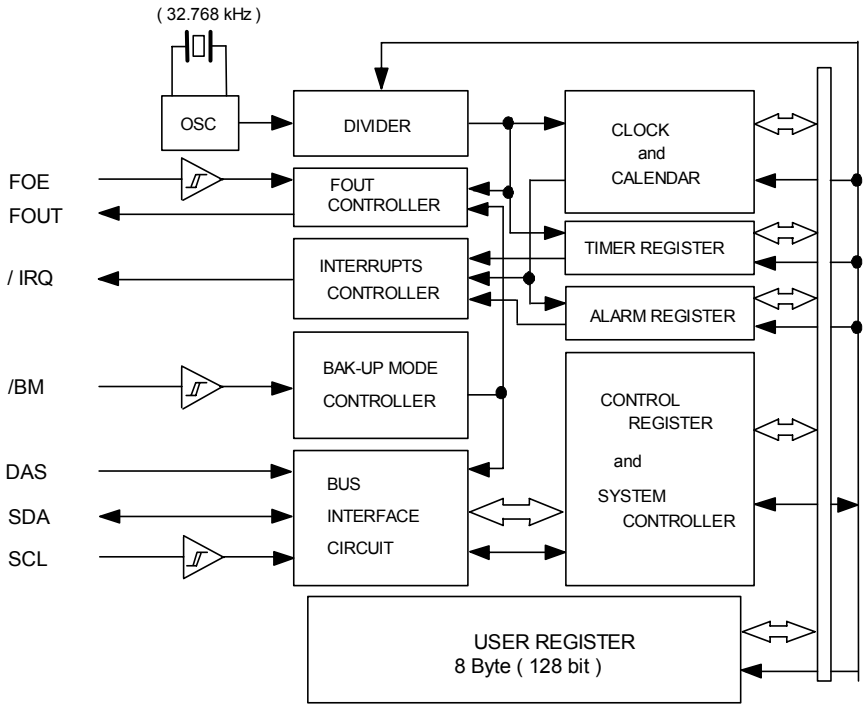
1. Overview

This is a real-time clock module of the I²C-BUS interface system that incorporates a 32.768 kHz crystal oscillator.

The real-time clock function incorporates not only a calendar and clock counter for the year, month, day, day of the week, hour, minute, and second, but also a time alarm, interval timer, and time update interruption, among other features.

All of these many functions are implemented in a thin, compact SOP package, which makes it suitable for various kinds of mobile telephones and other small electronic devices.

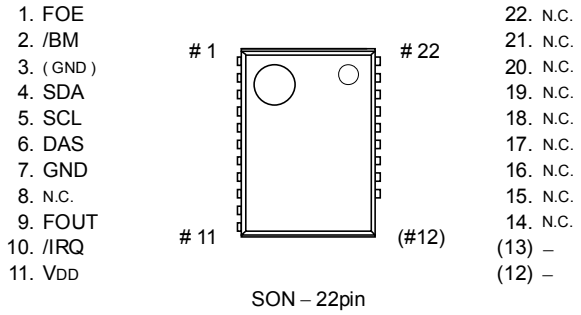
2. Block Diagram



3. Terminal description

3.1. Terminal connections

RX – 8571 NB



SON – 22pin

3.2. Pin Functions

Signal name	I/O	Function
SDA	Bi-directional	Addresses, data, acknowledge bits, etc. are input and output in synchronization with the I^2C-BUS communication serial clock. An appropriate pull-up resistance in accordance with the capacity of the signal cable must be connected to this terminal, which is an open drain at the time of output. It is able to input up to 5.5V regardless of V_{DD} applied voltage.
SCL	Input	The serial clock for I^2C-BUS communication is input here. It is able to input up to 5.5V regardless of V_{DD} applied voltage.
DAS	Input	Device Address select pin. This pin selects device address with 7 bits, which is composed I^2C-BUS. It is able to input up to 5.5V regardless of V_{DD} applied voltage. DAS pin: " H " → Slave address: 0110010; DAS pin: "L " → Slave address: 1010001
/BM	Input	It is a backup mode change input pin. Shift to a backup mode (/BM="L"), can suppress a current consumption to a minimum. In that case, the FOUT output stops, and access becomes invalid. It is able to input up to 5.5V regardless of V_{DD} applied voltage.
FOUT	Output	The FOUT terminal is a 32.768-kHz clock output terminal provided with output control. The FOE terminal is an input terminal for controlling the FOUT output. The FOE terminal is able to input up to 5.5V regardless of V_{DD} applied voltage. FOUT terminal when stops output becomes high impedance. However, while backup mode (/BM="L"), power output is stopped.
FOE	Input	

/BM pin input	FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin output
" H "	" H "	0	0	32768 Hz Output (C-MOS output) *
		0	1	1024 Hz Output (C-MOS output)
		1	0	1 Hz Output (C-MOS output)
	" L "	X	X	OFF (high impedance)
	X	1	1	OFF (high impedance)
" L "	X	X	X	OFF (high impedance)

X : don't care

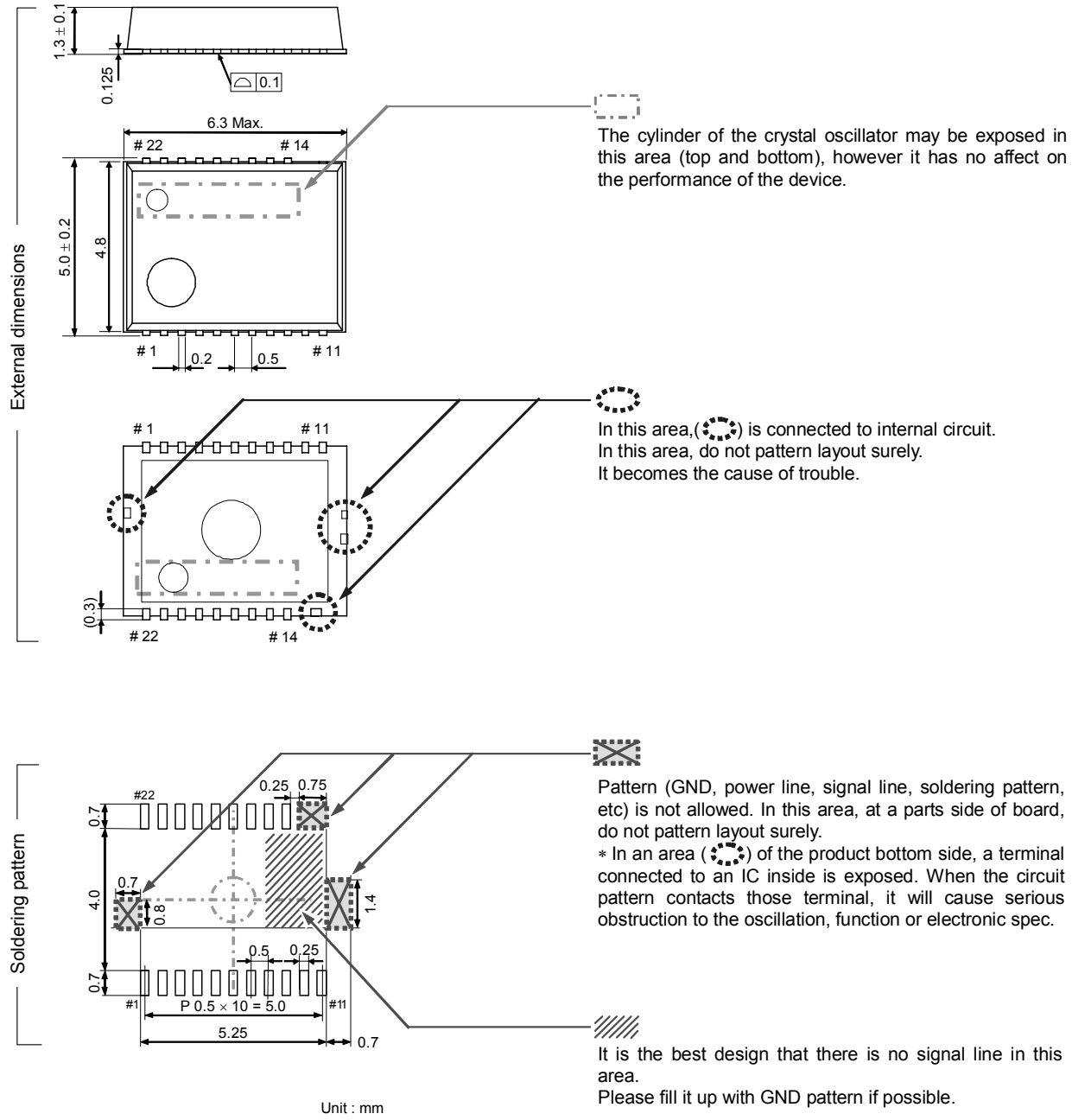
/ IRQ	Output	This terminal outputs interrupt signals ("L" level) for alarm interval timers, time update interruptions, and the like. This is an N-ch open-drain output terminal. It is able to Pull-up to 5.5V regardless of V_{DD} applied voltage.
V_{DD}	–	This is a power-supply terminal for the of the main power supply.
GND	–	This terminal is connected to the negative side (Ground) of the power supply.
N.C.	–	This pin is not connected internally. Be sure to connect using OPEN, or GND or V_{DD}.

Note : Be sure to connect a bypass capacitor rated at least 0.1 µF between V_{DD} and GND.

4. External Dimensions / Marking Layout

4.1. External Dimensions

RX – 8571 NB (SON – 22pin)



The cylinder of the crystal oscillator may be exposed in this area (top and bottom), however it has no affect on the performance of the device.

In this area,( ) is connected to internal circuit.
In this area, do not pattern layout surely.
It becomes the cause of trouble.

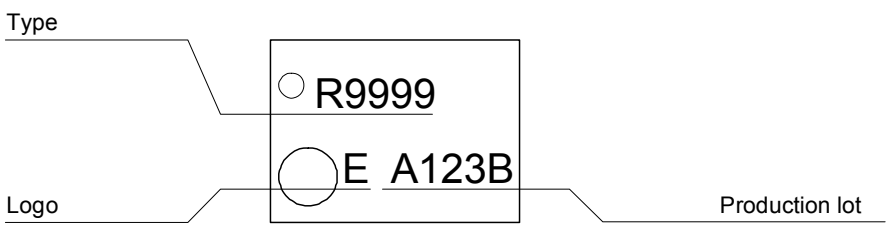
Pattern (GND, power line, signal line, soldering pattern, etc) is not allowed. In this area, at a parts side of board, do not pattern layout surely.
∗ In an area ( ) of the product bottom side, a terminal connected to an IC inside is exposed. When the circuit pattern contacts those terminal, it will cause serious obstruction to the oscillation, function or electronic spec.

It is the best design that there is no signal line in this area.
Please fill it up with GND pattern if possible.

Unit : mm

4.2. Marking Layout

RX – 8571 NB (SON – 22pin)



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

5. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	−0.3 to +6.5	V
Input voltage	VIN	DAS, SCLK, SDA, /BM,(FOE pins	GND−0.3 to +6.5	V
Output voltage (1)	VOUT1	FOUT pins	GND−0.3 to V_{DD}+0.3	V
Output voltage (2)	VOUT2	SDA, /IRQ pin	GND−0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	−55 to +125	°C

6. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	−	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	−	V_{LOW}	3.0	5.5	V
Low voltage detection	V_{LOW}	−			1.3	V
Applied voltage when OFF	V_{PUP}	DAS, SCLK, SDA, /BM, FOE, /IRQ pin			5.5	V
Operating temperature	T_{OPR}	No condensation	−40	+25	+85	°C

7. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition	Rating			Unit
Output frequency	fo			32.768 (Typ.)		kHz
Frequency/voltage characteristics	$\Delta f / f$	Ta = +25 °C V_{DD} = 3.0 V		5 ± 23 (*1)		$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta = +25 °C V_{DD} = 2.0 V ~ 5.0 V	−2		+2	$\times 10^{-6}$ / V
Frequency/temperature characteristics	Top	Ta = −20 °C to +70 °C, V_{DD} = 3.0 V ; +25 °C reference	−120		+10	$\times 10^{-6}$
Oscillation start time	t_{STA}	Ta = +25 °C, V_{DD} = 1.6 V		0.3	1.0	s
		Ta = − 40 °C to +85 °C V_{DD} = 1.6 V			3.0	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V ; first year	−5		+5	$\times 10^{-6}$ / year

*1) This difference is 1 minute by 1 month. (excluding offset)

8. Electrical Characteristics

8.1. DC characteristics

8.1.1. DC characteristics (1)

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +85 °C

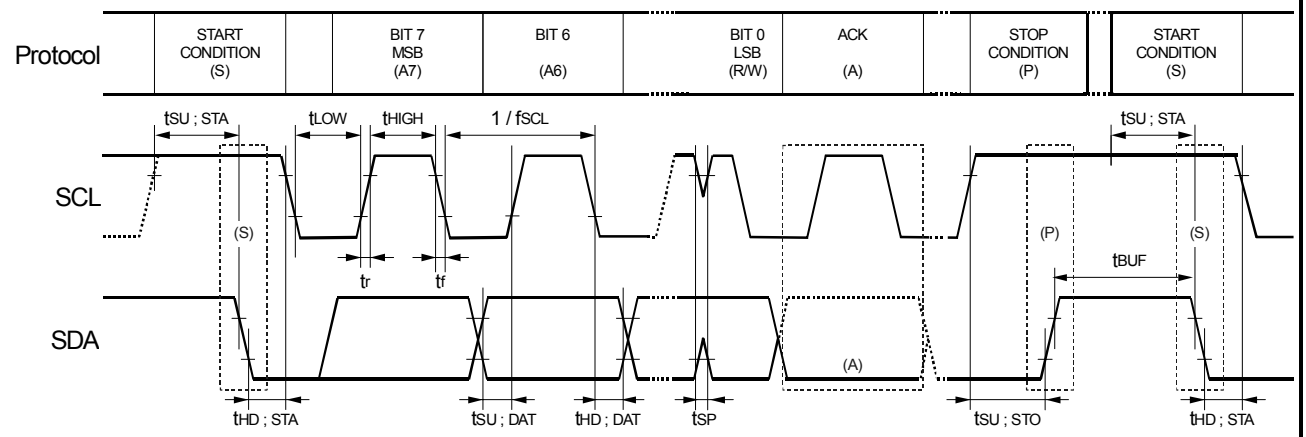
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	/BM=FOE="L", /IRQ = OFF fSCL=0Hz, Ta = +25 °C	V_{DD} = 3 V		200	400	nA
Current consumption (2)	I_{DD2}	/BM=FOE="L" /IRQ = OFF fSCL=0Hz Ta = Ta = ±0 °C to +50 °C	V_{DD} = 5 V		220	450	nA
Current consumption (3)	I_{DD3}		V_{DD} = 3 V		200	420	
Current consumption (4)	I_{DD4}	/BM=FOE="L" fSCL = 0 Hz, /IRQ = OFF	V_{DD} = 5 V			600	nA
Current consumption (5)	I_{DD5}		V_{DD} = 3 V			550	
Current consumption (6)	I_{DD6}	/BM=H, FOE="L" fSCL = 0 Hz, /IRQ = OFF	V_{DD} = 5 V		360	800	nA
Current consumption (7)	I_{DD7}		V_{DD} = 3 V		340	700	
Current consumption (8)	I_{DD8}	fSCL = 0 Hz, /IRQ = OFF, FOE = V_{DD}	V_{DD} = 5 V		1.6	3.3	µA
Current consumption (9)	I_{DD9}	FOUT : 32.768 kHz ON, C_L = 0 pF	V_{DD} = 3 V		1.0	2.1	
Current consumption (10)	I_{DD10}	fSCL = 0 Hz, /IRQ = OFF, FOE = V_{DD}	V_{DD} = 5 V		4.0	7.0	µA
Current consumption (11)	I_{DD11}	FOUT : 32.768 kHz ON, C_L = 15 pF	V_{DD} = 3 V		2.5	4.0	
High-level input voltage	V_{IH1}	FOE, DAS, /BM pin		0.8 × V_{DD}		6.5	V
	V_{IH2}	SCL, SDA pin		0.8 × V_{DD}		6.5	V
Low-level input voltage	V_{IL}	Input pin		GND – 0.3		0.2 × V_{DD}	V
High-level output voltage	V_{OH1}	FOUT pin	V_{DD}=5 V, I_{OH}=–1 mA	4.5		5.0	V
	V_{OH2}		V_{DD}=3 V, I_{OH}=–0.5 mA	2.7		3.0	
	V_{OH3}		V_{DD}=3 V, I_{OH}=–100 µA	2.9		3.0	
Low-level output voltage	V_{OL1}	FOUT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD}=3 V, I_{OL}=0.5 mA	GND		GND+0.3	
	V_{OL3}		V_{DD}=3 V, I_{OL}=100 µA	GND		GND+0.1	
	V_{OL4}	/IRQ pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.4	
	V_{OL6}	SDA pin	V_{DD} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V
Input leakage current	I_{LK}	Input pin, V_{IN} = V_{DD} or GND		–0.1		0.1	µA
Output leakage current	I_{OZ}	Input pin, V_{OUT} = V_{DD} or GND		–0.1		0.1	µA

8.2. AC characteristics

* Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Standard-Mode (f_{SCL}=100kHz)		Fast-Mode (f_{SCL}=400kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Start condition setup time	$t_{SU;STA}$	4.7		0.6		µs
Start condition hold time	$t_{HD;STA}$	4.0		0.6		µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Data hold time	$t_{HD;DAT}$	0		0		ns
Stop condition setup time	$t_{SU;STO}$	4.0		0.6		µs
Bus idle time between start condition and stop condition	t_{BUF}	4.7		1.3		µs
Time when SCL = "L"	t_{LOW}	4.7		1.3		µs
Time when SCL = "H"	t_{HIGH}	4.0		0.6		µs
Rise time for SCL and SDA	t_r		1.0		0.3	µs
Fall time for SCL and SDA	t_f		0.3		0.3	µs

Timing chart



Caution: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access **should be completed within 0.95 seconds**.
If such communication requires **0.95 seconds** or longer, the I^2C bus interface is reset by the internal bus timeout function.

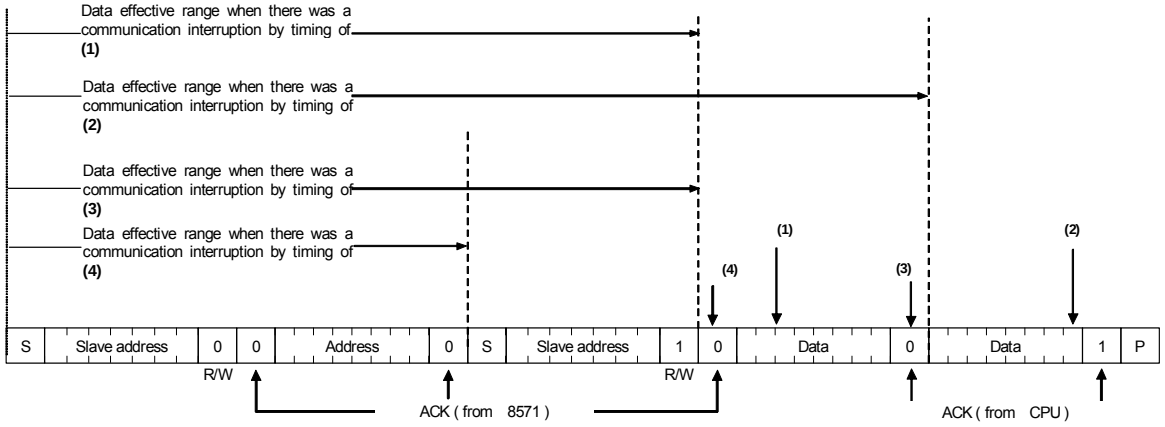
Data writing : It's necessary to input the data of 8-bit units.
During inputting the data of 8-bit units, a state of suspension occurs,
the data are not written appropriately.

9. Matters that demand special attention on use

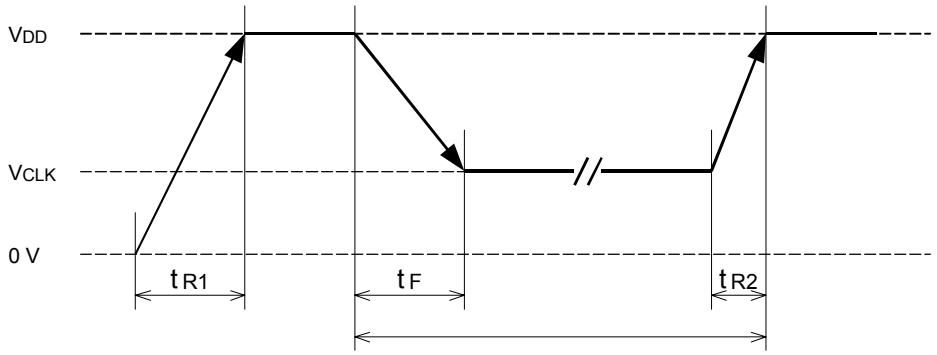
9.1. About data when communication is stopped

(1) If access is interrupted with timing in transmission of acknowledge signal and timing except in checking (following drawing (1), (2)), up to data that passed and confirmed just before acknowledge signal is available.

(2) If access is interrupted with timing in transmission of acknowledge signal and in checking (following drawing (3), (4)), up to data that passed and confirmed last acknowledge signal is available.



9.2. Migrating to backup, and returning



Parameter	Symbol	Min.	Typ.	Max.	Unit
Power drop time	t_F	2			μs / V
Power rise time	t_{R1}	5			μs / V
Clock maintenance power-up time	t_{R2}	0			μs

9.3. Restrictions on Access Operations During Power-on Initialization and Recovery from Backup

- RTC-register (Reg - 00[h] ~ 0F[h]) operations are linked to the internal quartz oscillator's clock signal, so normal operation is not possible if there is no internal oscillation (= oscillation is stopped).

  Therefore, we recommend that the initial setting to be set during power-on initialization or backup and restore operations (i.e., when the power supply voltage is recovered after oscillation has stopped due to a voltage drop, etc.) should be "first start internal oscillation, then wait for the oscillation stabilization time (see tSTA standard) to elapse".

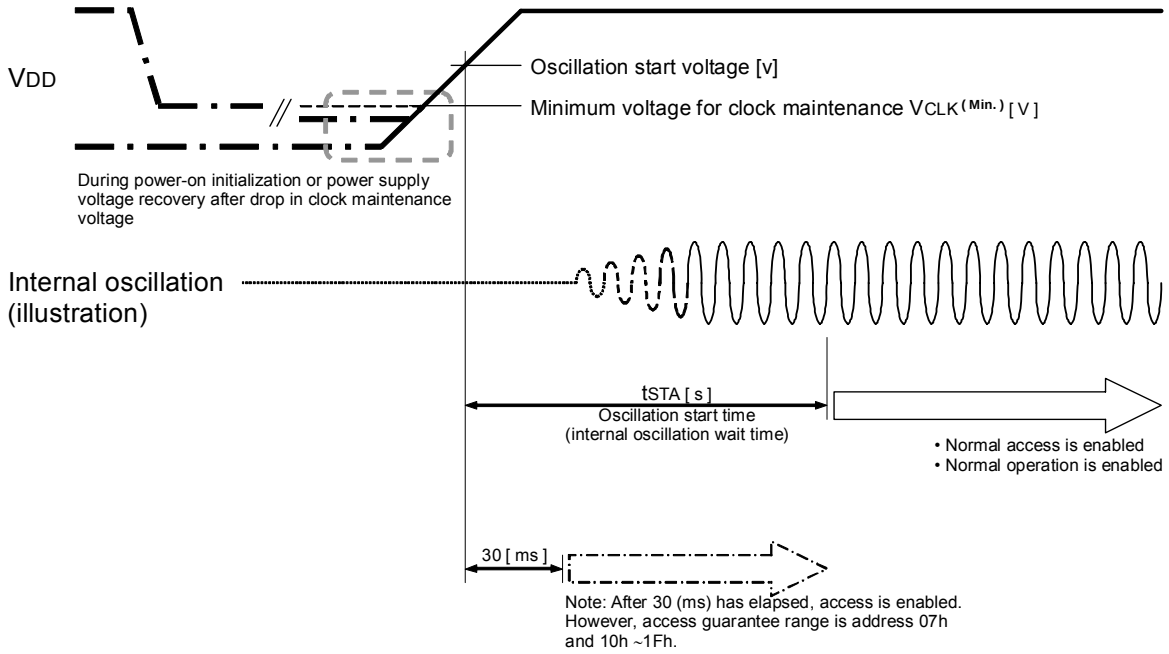
- Note the following caution points concerning access operations during power-on initialization or when restoring the power supply voltage from backup mode (hereafter referred to as "switching to the operating voltage").

  1) Before switching to the operating voltage, read the VLF-bit (which indicates the RTC error status).

  2) Initialization is required when the value read from the VLF-bit is "VLF = 1 (error status)".
  Before initializing in response to this VLF = "1" result, we recommend first waiting for the internal oscillation stabilization time (see the tSTA standard) to elapse.

Initialization is required when the status after reading a VLF-bit value of "1" is either of the following. (Status 1) During power-on initialization (Status 2) When the clock setting is invalid, such as due to a voltage drop during backup

  ∗ Access timing during power-on initialization and when recovering the power supply voltage after a drop in the voltage used to maintain the clock



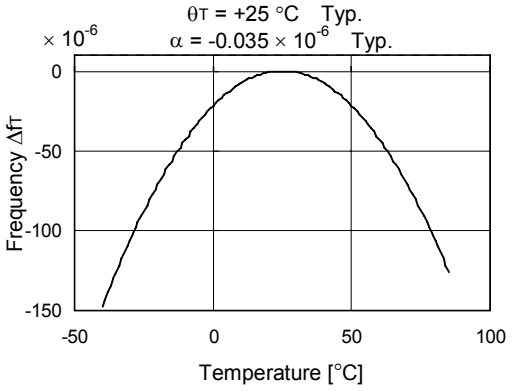
  3) When the read VLF-bit value is "VLF = 0 (normal status)", access is enabled without waiting for stabilization of oscillation.

Normal operation is enabled under the following two statuses when "0" is read as the VLF-bit value. (Status 1) When correct operation is enabled (except for settings errors while in use) (Status 2) When data is retained normally while switching to the operating voltage from backup mode

10.1. Reference information

10.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

   $\Delta f_T = \alpha (\theta_T - \theta_X)^2$

   - Δf_T : Frequency deviation in any temperature
   - α [1 / °C^2] : Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6}$ / °C^2
   - θ_T [°C] : Ultimate temperature ($+25 \pm 5$ °C)
   - θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

   $\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

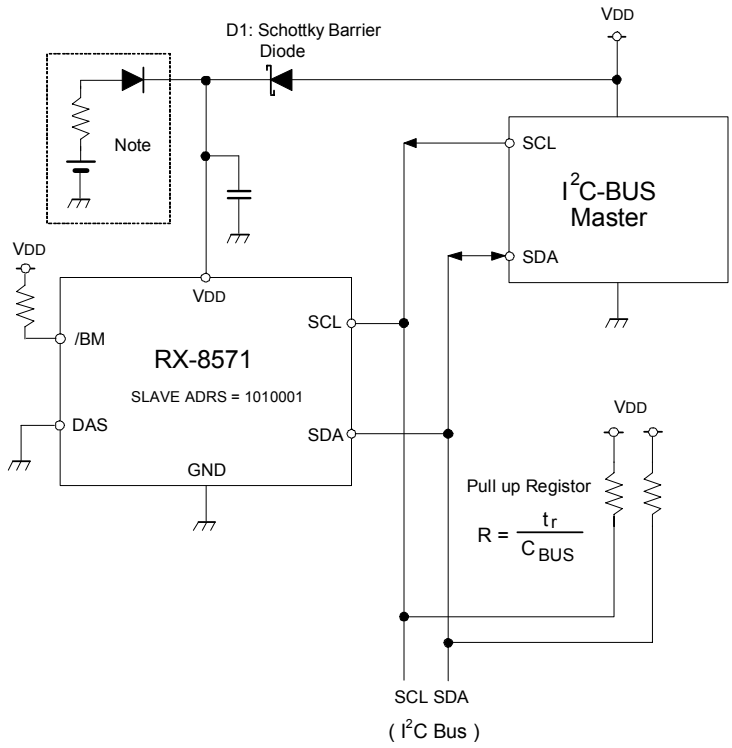
   - $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
   - $\Delta f/fo$: Frequency precision
   - Δf_T : Frequency deviation in any temperature.
   - Δf_V : Frequency deviation in any voltage.

3. How to find the date difference

   Date Difference = $\Delta f/f \times$ 86400(Sec)

   ∗ For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

10.2. External connection example



Note :

It uses the secondary battery or a lithium battery. When using the seconding battery, the diode is not required. When using the lithium battery, the diode is required. For detailed value on the resistance, please consult a battery maker.

11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

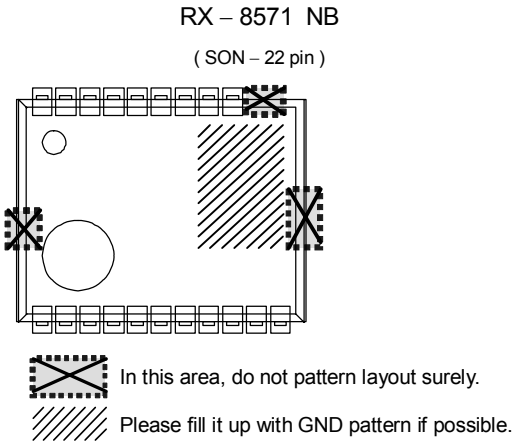
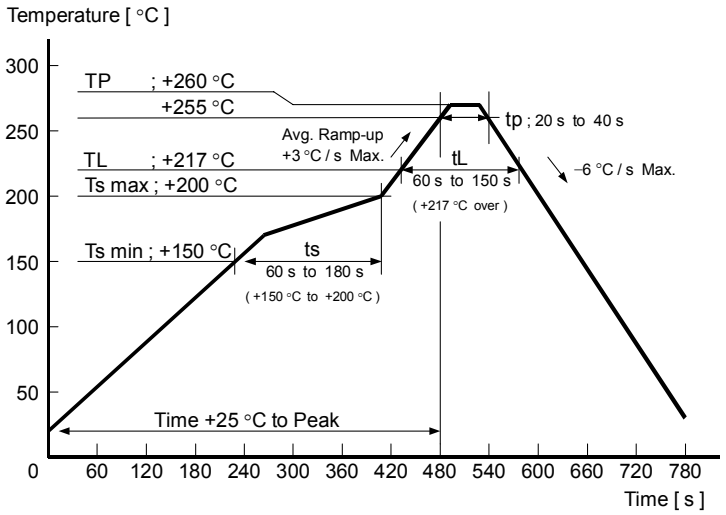


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



12. Overview of Functions and Description of Registers

12.1. Overview of Functions

1) Clock functions

This function is used to set and read out month, day, hour, date, minute, second, and year (last two digits) data. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.

2) Fixed-cycle Timer Interrupt function

The fixed-cycle timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 65535 hours.

When an interrupt event is generated, the /TIRQ pin goes to low level ("L") and "1" is set to the TF bit to report that an event has occurred..

3) Long-Timer function

It is able to use fixed cycle timer interrupt function as Long-Timer that deals with for approx. 7.5 years.

∗ For details, see "13.2. Fixed-cycle Interrupt Function".

4) Alarm interrupt function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.

5) Time update interrupt function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock. When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred.

6) Voltage detection function (VLF)

This function indicates the retained status of clock operations or internal data.

7) Clock output function

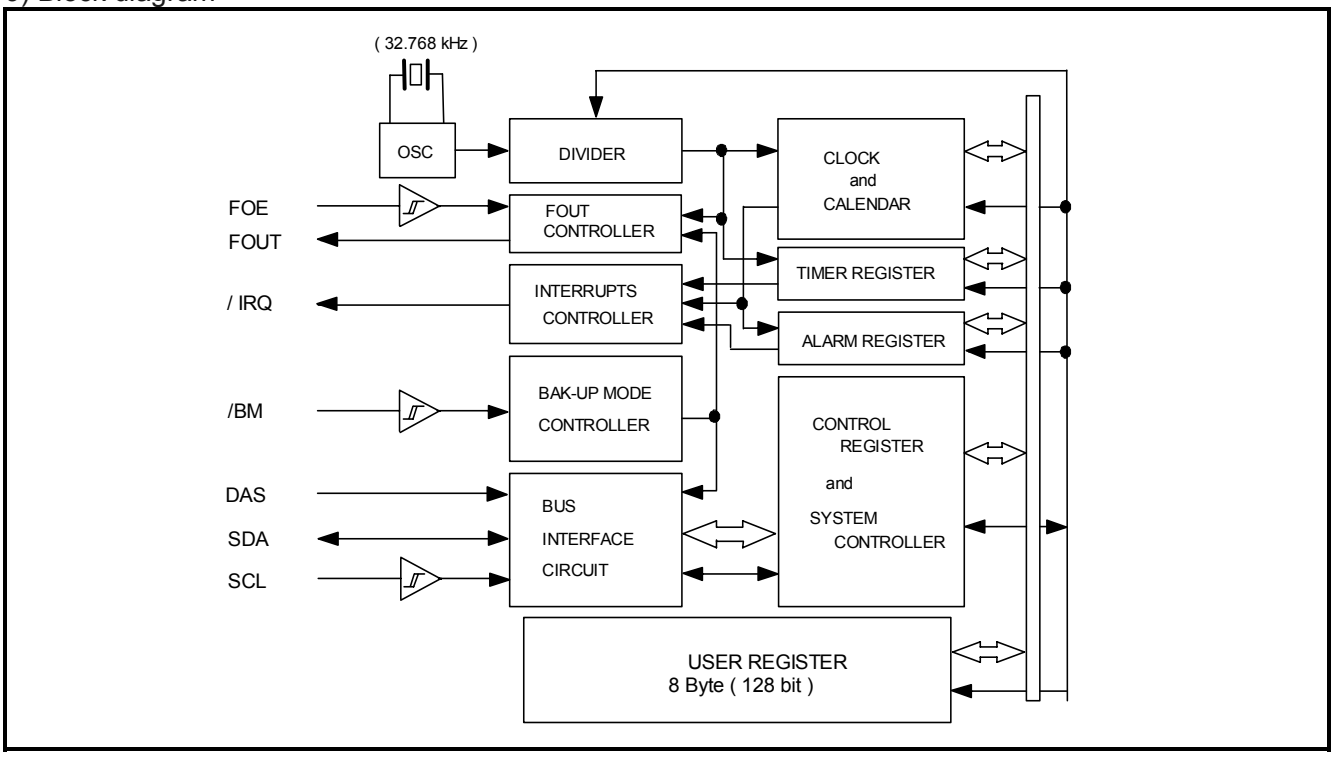
A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin (CMOS output).

8) User RAM

RAM register is read/write accessible for any data.

Up to max. 176 bits can be expanded.

9) Block diagram



12.2. Register table

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
00	SEC	○	40	20	10	8	4	2	1	∗2
01	MIN	○	40	20	10	8	4	2	1	∗2
02	HOUR	○	○	20	10	8	4	2	1	∗2
03	WEEK	○	6	5	4	3	2	1	0	∗2
04	DAY	○	○	20	10	8	4	2	1	∗2
05	MONTH	○	○	○	10	8	4	2	1	∗2
06	YEAR	80	40	20	10	8	4	2	1	
07	RAM	•	•	•	•	•	•	•	•	∗3, ∗4
08	MIN Alarm	AE	40	20	10	8	4	2	1	
09	HOUR Alarm	AE	•	20	10	8	4	2	1	∗3
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	∗3
	DAY Alarm		•	20	10	8	4	2	1	
0B	Timer Counter 0	128	64	32	16	8	4	2	1	
0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	
0D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0	∗2
0E	Flag Register	***TEST1***	***TEST2***	UF	TF	AF	***TEST3***	VLF	○	∗1, ∗2
0F	Control Register	○	○	UIE	TIE	AIE	TSTP	STOP	○	∗2

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
10 | 1F	RAM	User Register 128 bit (16 word x 8 bit)								∗3, ∗4, ∗5

Note During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.
When doing this, be careful to avoid setting incorrect data as the date or time, as timed operations cannot be guaranteed if incorrect date or time data has been set.

∗1. The ***TEST1***, ***TEST2***, ***TEST3*** bits are Epson Toyocom test bits.
∗ Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing.
∗ The four ***TEST**** bits are undefined when read. Those bits should be masked after being read.

∗2. The ' ○ ' mark indicates a write-prohibited bit, which returns a "0" when read.

∗3. The ' • ' mark indicates a read/write-accessible RAM bit for any data.

∗4. As for Address 07[h] and User Register, R/W is enabled after 30ms after arrival the V_{DD} voltage in a Operating voltage range at initial power-on (from 0 V).

∗5 The User Register is read/write accessible for any data in the range from 00 h to FF h.

12.3. Description of Functions

12.3.1. Clock & Calendar Register (Reg - 00[h] ~ 06[h])

The clock and the calendar consists of seconds, minutes, hours, day of the week, day, month, and year.

∗ For details, see "13.1. Clock functions".

12.3.2. RAM Register (Reg - 07[h] and Reg - 10[h] ~ 1F[h])

This RAM register is read/write accessible for any data in the range from 00 h to FF h.

R/W is enabled after 30ms after arrival the V_{DD} voltage in an Operating voltage range at initial power-on.

12.3.3. Alarm Register (Reg - 08[h] ~ 0A[h])

The alarm interrupt function is used, along with the AE, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values. When the settings in the alarm registers and the WADA bit match the current time, the /IRQ pin goes to low level and "1" is set to the AF bit to report that and alarm interrupt event has occurred.

When this function is not used, this register is read/write accessible for any data by setting to AIE=”0”.

∗ For details, see "13.2. Alarm Interrupt Function".

12.3.4. Timer setting and Timer counter register (Reg - 0B[h] ~ 0C[h])

To use the fixed-cycle timer interrupt function, the TE, TF, TIE, TSEL0, TSEL1 and TSEL2 bits are set and used. When this down counter's count value changes from 0001h to 0000h, when TF bit = "1", or when the /IRQ pin is at low level ("L"), it indicates that a fixed-cycle timer interrupt event has occurred. When this function is not used, This register is read/write accessible for any data by writing "0" to the TE and TIE bits.

∗ For details, see "13.3. Fixed-cycle Timer Interrupt Function.

12.3.5. Extension-related register (Reg - 0D[h] ~ 0F[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
0E	Flag Register	***TEST1***	***TEST2***	UF	TF	AF	***TEST3***	VLF	○
0F	Control Register	○	○	UIE	TIE	AIE	TSTP	STOP	○

1) FSEL1, FSEL0 bits (Frequency Select)

A combination of the FSEL1 and FSEL0 bits is used to select the frequency to be output.

The choice is possible by a combination of FSEL-bits and FOE-pin, select the frequency of clock output or inhibit the clock output. Setting example when a this function is not used. (The FOE terminal is connected to GND, FSEL0,1 = “0”) ∗ For details, see "13.7. Fout Function.

2) USEL, UF, UIE bits (Time update Interrupt)

These are bits to control an action of the Time update interrupt function.

Setting example when a time this function is not used. (USEL , UIE = “0”, Ignore UF)

∗ For details, see "13.4. Time update interrupt Function.

3) TE, TF, TIE, TSEL2, TSEL1, TSEL0, TSTP bit (Fixed-cycle timer interrupt)

These are bits to control an action of the Fixed-cycle timer interrupt function.

Setting example when a time this function is not used.

(TE,TIE,TSTP, TSEL1,TSEL0=“0”, TSEL2=”1”, Ignore TF)

∗ For details, see "13.3. Fixed-cycle Timer Interrupt Function ".

4) WADA, AF, AIE bit (Alarm interrupt)

These are bits to control an action of the Alarm interrupt function.

Setting example when a time this function is not used. (WADA, AIE = “0”, Ignore AF)

∗ For details, see "13.2. Alarm Interrupt Function".

5) ***TEST*** bit

Those bits are the manufacturer's test bit. Always leave this bit value as "0" except when testing.

Be careful to avoid writing to this bit when writing "1" to other bits in this register.

6) VLF bit(Voltage Low Flag)

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

∗ For details, see "13.6. Voltage detection function".

7) STOP bit

This bit is used to stop functions related to the RTC's internal counter operations.

Writing a "1" to this bit stops the counter operations.

There is the following influence at the time of STOP bit “1”.

∗ 1) All the update of a clock and a calendar action stops.
With it, an alarm interrupt and time update interrupt events does not occur.

∗ 2) One part of a fixed-cycle timer function stops.
A count stops at the time of 64Hz, 1Hz, 1min, 1h source clock setting of a fixed-cycle timer.
(A fixed-cycle timer can work only in 4096Hz.)

∗ 3) The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz and 1024Hz output is possible. But 1Hz output is disabled.

13.1. How to use

13.1. Description of Clock & Calendar function

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end. Therefore it recommends that the access to a clock calendar has continuous access by the auto increment function.

Setting example: Sun, 29-Feb-88 17:39:45 (leap year)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	SEC	0	1	0	0	0	1	0	1
01	MIN	0	0	1	1	1	0	0	1
02	HOUR	0	0	0	1	0	1	1	1
03	WEEK	0	0	0	0	0	0	0	1
04	DAY	0	0	1	0	1	0	0	1
05	MONTH	0	0	0	0	0	0	1	0
06	YEAR	1	0	0	0	1	0	0	0

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

13.1.1. Clock counter (Reg - 00[h] ~ 02[h])

1) [SEC] & [MIN] counter (Reg - 00[h] ~ 01[h])

These registers are 60-base BCD counters. These registers are incremented at the timing when carry is generated from a lower register. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.
When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512Hz ~ 1 Hz) is cleared to 0.

2) Hour counter (Reg - 02[h])

This register is a 24-base BCD counter (24 hour format).These registers are incremented at the timing when carry is generated from a lower register.

13.1.2. . Week counter (Reg - 03[h])

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.

- The correspondence between days and count values is shown below.

Day	bit	bit 6	bit 5	bit 4	bit 3	bit 2	bi	bit 0	Data [h]
Sunday	0	0	0	0	0	0	0	**1**	01 h
Monday	0	0	0	0	0	0	**1**	0	02 h
Tuesday	0	0	0	0	0	**1**	0	0	04 h
Wednesday	0	0	0	0	**1**	0	0	0	08 h
Thursday	0	0	0	**1**	0	0	0	0	10 h
Friday	0	0	**1**	0	0	0	0	0	20 h
Saturday	0	**1**	0	0	0	0	0	0	40 h

∗ Do not set "1" to more than one day at the same time.

13.1.3. Calendar counter (Reg - 04[h] ~ 06[h])

1) [DAY] & [MONTH] register (Reg - 04 [h])

The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is 12-base BCD counter. when carry is generated from a lower register.

		Jan.	Feb.	Mar	Apr.	May	June	July	Aug.	Sep.	Oct.	Nov.	Dec.
Days	Normal year	31	28	31	30	31	30	31	31	30	31	30	31
	Leap year		29										

2) [YEAR] register (Reg - 06 [h])

This register is a BCD counter for years 00 to 99.
The leap year is automatically determined, which reflects in the DAY register.

13.2. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 65535 hours.
This function can stop at one time and is available as a accumulative timer.
After the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low-level to Hi-z).
At the time of source clock setting 1Hz or 1/60Hz or 1/3600Hz, IRQ outputs "L" after 7.813ms from event occurrence at the maximum.

13.2.1. Related registers for function of fixed-cycle timer interrupt function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C	Timer Counter 1	**32768**	**16384**	**8192**	**4096**	**2048**	**1024**	**512**	**256**
0D	Extension Register	FSEL1	FSEL0	USEL	**TE**	WADA	**TSEL2**	**TSEL1**	**TSEL0**
0E	Flag Register	TEST1	TEST2	UF	**TF**	AF	TEST3	VLF	○
0F	Control Register	○	○	UIE	**TIE**	AIE	**TSTP**	STOP	○

∗ Before entering operation settings, we recommend first clearing the TE bit to "0" .
∗ When the fixed-cycle timer function is not being used, the fixed-cycle timer control register (Reg – 0B to 0C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) Down counter for fixed-cycle timer (Timer Counter 1, 0)
This register is used to set the default (preset) value for the counter. Any count value from 1 (0001 h) to 65535 (FFFFh) can be set.
Be sure to write "0" to the TE bit before writing the preset value. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

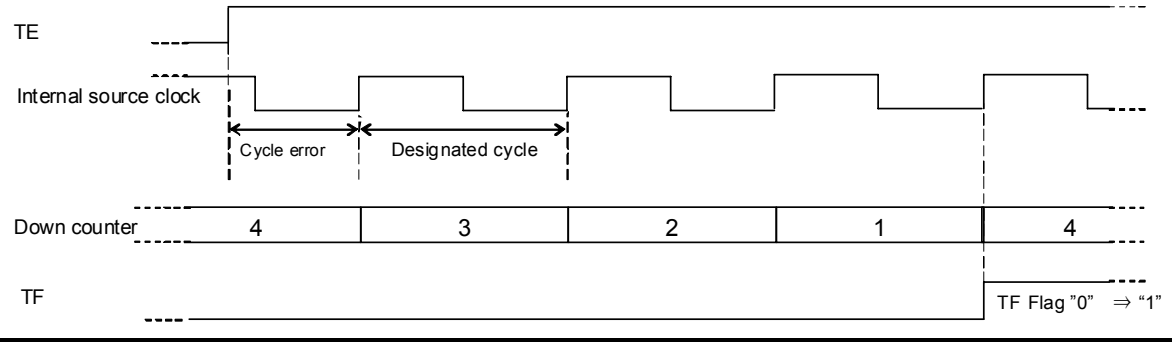
∗ When TE=0, read out data of timer counter is default(Preset) value.
And when TE=1, read out data of timer counter is just counting value.
But, when access to timer counter data, counting value is not held.
Therefore, for example, perform twice read access to obtain right data, and a way to adopt the case that two data accorded is necessary.

2) TSEL2, TSEL1, TESL0 bits (Timer Select 2, 1, 0)
The combination of these three bits is used to set the countdown period (source clock) for this function.
Be sure to write "0" to the TE bit before writing the source clock value.

TSEL2, 1, 0	TSEL1 (bit 1)	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN	Effects of STOP and RESET bits
W / R	0	0	0	4096 Hz /Once per 244.14 μs	122 μs	–
	0	0	1	64 Hz /Once per 15.625 ms	7.813 ms	∗ Does not operate when the STOP bit value is "1".
	0	1	0	1 Hz /Once per second	7.813 ms	
	0	1	1	1/60 Hz /Once per minute	7.813 ms	
	1	0	0	1/3600 Hz /Once per hour	7.813 ms	

∗1) The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.
∗2) The first countdown shortens than a source clock.
It is linked with carry update of inner timing, for example, if timer movement is started at 50 minute, the first countdown is performed after 10 minutes. (After the second time, countdown is performed with proper cycle of 1 minute)

The example of the error of the first countdown: A value to preset is 0004h



3) TE bit (Timer Enable)

When TE bit is "0", the default (preset) can be checked by reading this register.

TE	Data	Description
Write	0	Stops fixed-cycle timer interrupt function. ∗ Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z).
	1	Starts fixed-cycle timer interrupt function. ∗ The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z).
	1	This bit is invalid after a "1" has been written to it.
Read	0	–
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when a fixed-cycle timer interrupt event has occurred.

TIE	Data	Description
Write	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z). ∗ Even when the TIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-z to low).

6) TSTOP bit (Timer stop)

This bit is used to stop fixed-cycle timer count down.

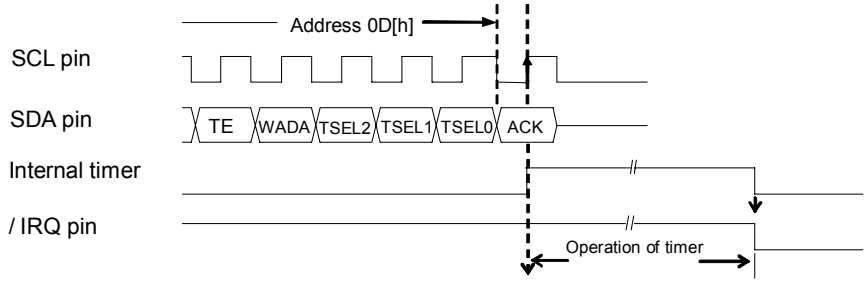
∗ It is linked with carry update of inner timing, therefore stop shorter period than source clock may not be reflected.

* For example, even if select source clock 1/3600 Hz and suspend countdown from 3 o'clock 5 minutes to 3 o'clock 55 minutes of time counter, countdown is performed 5 minutes later at 4 o'clock 0 minute similar to the case without suspend.

TSTP	Data	Description
Write	0	Writing a "0" to this bit cancels stop status (restarts timer count down).
	1	Writing a "1" to this bit stops the timer count down. ∗ The /IRQ output does not change.

13.2.3. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL (ACK output) signal that occurs when the TE value is changed from "0" to "1".

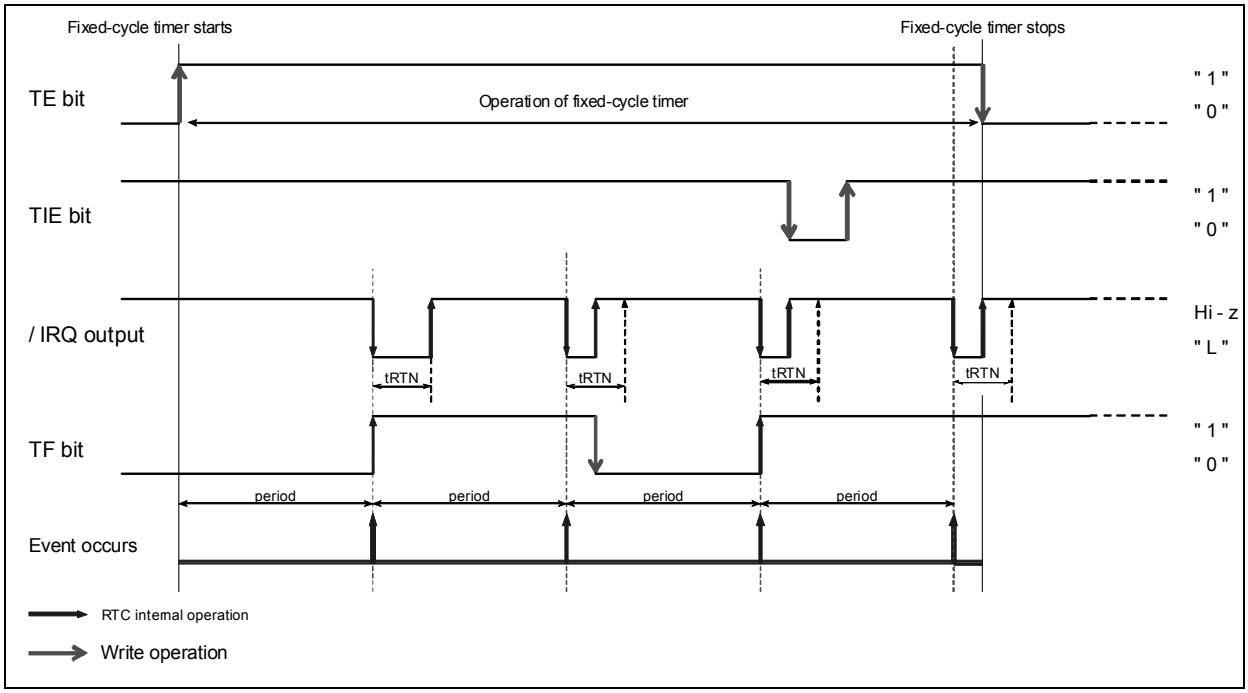


13.2.4. Fixed-cycle timer interrupt interval (example)

The combination of the source clock settings (settings in TSEL2, TSEL1 and TSEL0) and fixed-cycle timer countdown setting (Reg–0B to Reg-0C setting) sets the fixed-cycle timer interrupt interval, as shown in the following examples.

Timer Counter setting 1 ~ 65535	Source clock				
	4096 Hz TSEL2 = 0 TSEL1, 0 = 0, 0	64 Hz TSEL2 = 0 TSEL1, 0 = 0, 1	1 Hz TSEL2 = 0 TSEL1, 0 = 1, 0	1 / 60 Hz TSEL2 = 0 TSEL1, 0 = 1, 1	1 / 3600 Hz TSEL2 = 1 TSEL1, 0 = 0, 0
0	–	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min	1 h
2	488.28 μs	31.250 ms	2 s	2 min	2 h
:	:	:	:	:	:
41	10.010 ms	640.63 ms	41 s	41 min	41 h
128	31.250 ms	2.000 s	128 s	128 min	128 h
320	78.125 ms	5.000 s	320 s	320 min	320 h
410	100.10 ms	6.406 s	410 s	410 min	410 h
:	:	:	:	:	:
3840	0.9375 s	60.000 s	3840 s	3840 min	3840 h
:	:	:	:	:	:
4096	1.0000 s	64.000 s	4096 s	4096 min	4096 h
:	:	:	:	:	:
65535	15.9998 s	1023.984 s	65535 s	65535 min	65535 h

13.2.5. Diagram of fixed-cycle timer interrupt function



∗ After the interrupt event that occurs when the count value changes from 0001h to 0000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

∗ The count down that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

13.3. Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings.

When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred. AF bit and IRQ output change after 1.46ms from alarm agreement at the maximum.

∗ /IRQ"L" output when occurs alarm interruption event is not cancelled automatically unless giving intentional cancellation and /IRQ"L" is maintained.

13.3.1. Related registers for Alarm interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	TSEL2	TSEL1	TSEL0
0E	Flag Register	TEST1	TEST2	UF	TF	**AF**	TEST3	VLF	○
0F	Control Register	○	○	UIE	TIE	**AIE**	TSTP	STOP	○

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ Even if use alarm register (Rag - 08h ~ 0Ah) as RAM register, inside of RTC is processed as alarm setting, therefore it is able to prevent unintentional alarm occurrence (/IRQ"L" occurrence) due to unexpected agreement with writing data and timer condition by means of setting to AIE="0".

1) Alarm registers (Reg – 08[h] to 0A[h])

In the WEEK alarm /Day alarm register (Reg - 0A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

∗1) The register that "1" was set to "AE" bit, doesn't compare alarm.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 0A):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only an hour and minute accords with alarm data.

∗2) If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

∗3) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

2) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	–
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when an Alarm interrupt event has occurred.

AIE	Data	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-z to low).

∗The AIE bit is only output control of the /IRQ terminal. It is necessary to clear an AF flag to cancel alarm.

13.3.2. Examples of alarm settings

1) Example of alarm settings when "Day" has been specified (and WADA bit = "0")

Day is specified WADA bit = "0"	Reg – A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	HOUR Alarm	MIN Alarm
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07 h	AE bit = 1
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	AE bit = 1	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

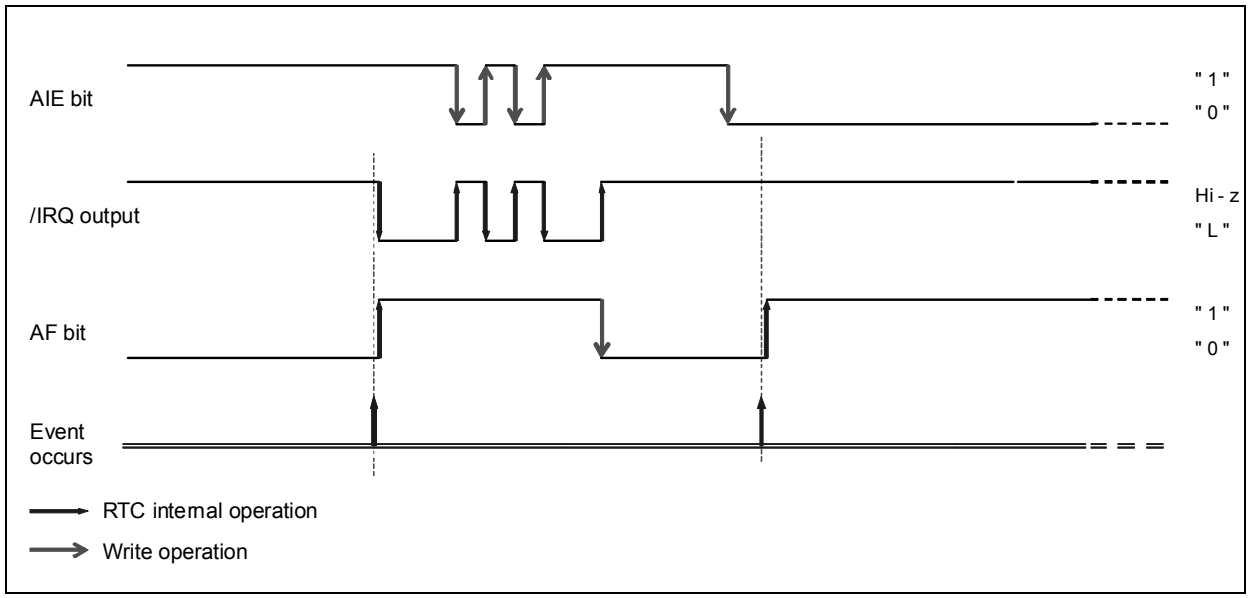
X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Reg - A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	HOUR Alarm	MIN Alarm
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	07 h	AE bit = 1
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	AE bit = 1	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

13.3.3. Diagram of alarm interrupt function



13.4. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
This /INT status is automatically cleared (/INT status changes from low level to Hi-z 7.813ms after the interrupt occurs. IRQ outputs "L" after 23.44ms from time update at the maximum.

13.4.1. Related registers for time update interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	TSEL2	TSEL1	TSEL0
0E	Flag Register	TEST1	TEST2	**UF**	TF	AF	TEST3	VLF	○
0F	Control Register	○	○	**UIE**	TIE	AIE	TSTP	STOP	○

∗ Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.
∗ When the STOP bit value is "1" time update interrupt events do not occur.
∗ Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /IRQ pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

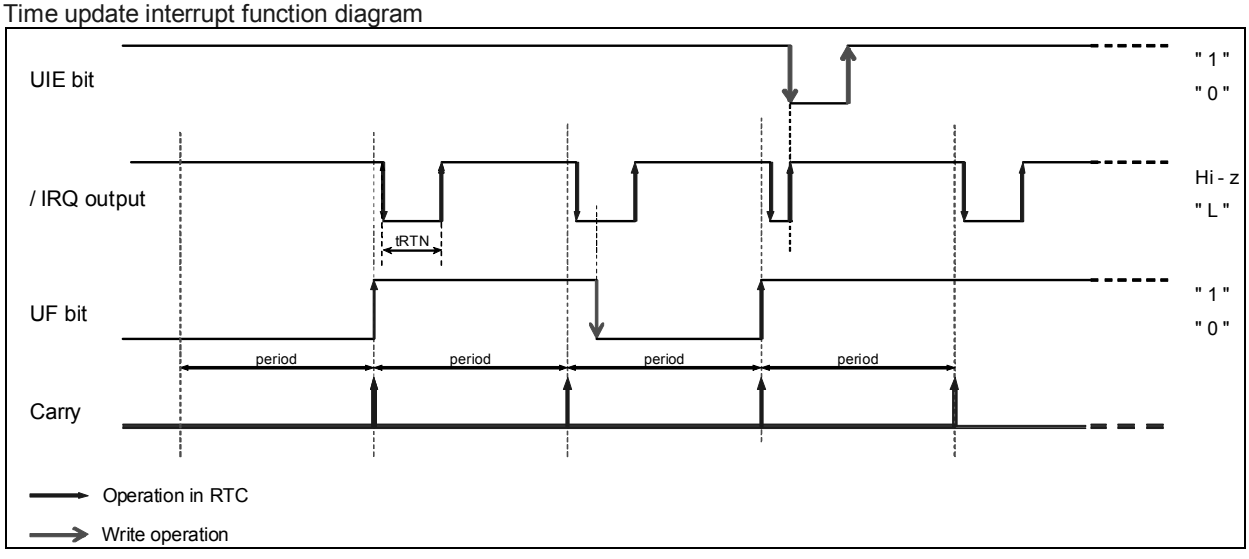
UF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-z) when an time update interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	–
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

3) UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

UIE	Data	Description
Write / Read	0	1) Does not generate an interrupt signal. (/IRQ remains Hi-z) 2) Cancels interrupt signal triggered by time update interrupt event (/IRQ changes from low to Hi-z).
	1	When an Update interrupt event occurs, an interrupt signal is generated .

13.4.2. Time update interrupt function diagram



13.5. /IRQ "L" Interrupt Output When Interrupt Function Operates

1) Setting interrupt events to occur in response to /IRQ "L" interrupt output

The /IRQ interrupt output pin is shared as the output pin for three kinds of interrupt events: events related to the fixed-cycle timer interrupt function and events related to the time update interrupt function and events related to the alarm interrupt function.

When an interrupt occurs (when /IRQ is at low level ("L")), read the TF and UF and AF flags to determine which type of interrupt event occurred (which flag value changed to "1").

2) How to prevent /IRQ pin from going to low level ("L")

To prevent the /IRQ pin from going to low level ("L"), clear all TIE and UIE and AIE bits to zero.
To detect when an interrupt event has occurred without having to set the /IRQ pin to low level, monitor the TF and AF flag bit values to see if the target interrupt event has occurred (i.e., to see if either flag bit value changes from "0" to "1").

13.6. Voltage detection function (VLF)

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.

VLF	Data	Description
Write	0	The VLF is cleared to 0, and waiting for next low voltage detection.
	1	It is impossible to write in 1 to VLF.
Read	0	RTC register data are valid.
	1	RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

13.7. FOUT function [clock output function]

The clock signal can be output (as C-MOS output) via the FOUT pin.

13.7.1. FOUT control register.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	TSEL2	TSEL1	TSEL0

By a combination of FSEL and FOE, an FOUT terminal outputs 32768Hz and 1024Hz and 1Hz and can stop the output.

13.7.2. FOUT function table.

/BM pin	FOE pin	FSEL1	FSEL0	FOUT pin output
"H"	"H"	0	0	32768 Hz Output (C-MOS output)
		0	1	1024 Hz Output (C-MOS output)
		1	0	1 Hz Output (C-MOS output)
	"L"	X	X	OFF (high impedance) ***1**
	X	1	1	OFF (high impedance) ***2**
"L"	X	X	X	OFF (high impedance) ***3**

*1 At initial power-on , in case of FOE input is high, 32768Hz is selected automatically by power-on-reset-function.

*2 When control about ON and OFF of the output from FOUT by only FSEL, should FOE=H.

*3 When /BM pin is "L", FOUT output is disabled, without being concerned with setting of a FSEL bit and FOE.

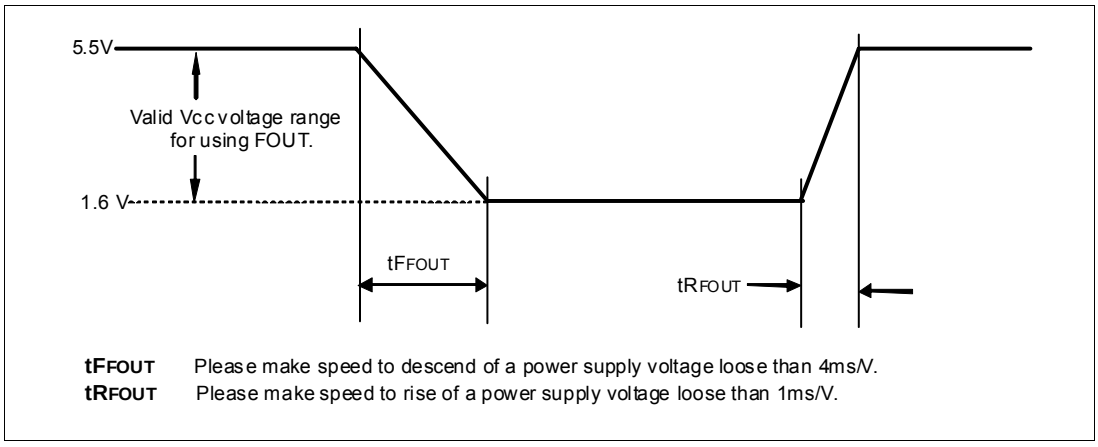
13.7.3. Attention of FOUT function.

Note 1
Valid voltage range for FOUT function is 1.6V to 5.5V. (Please see operating voltage.)

Note 2
A disappearance of the FOUT output when the voltage sharply went up and down.

For example, VDD voltage of the RTC is come and go between Main power and backup battery.
The clock output from FOUT disappears then during several milli-seconds when a sharp voltage change happens.
Please check that there is not a problem by this characteristic on your system.

An reference example of a power up and down timing without affect to FOUT.



tFFOUT Please make speed to descend of a power supply voltage loose than 4ms/V.
tRFOUT Please make speed to rise of a power supply voltage loose than 1ms/V.

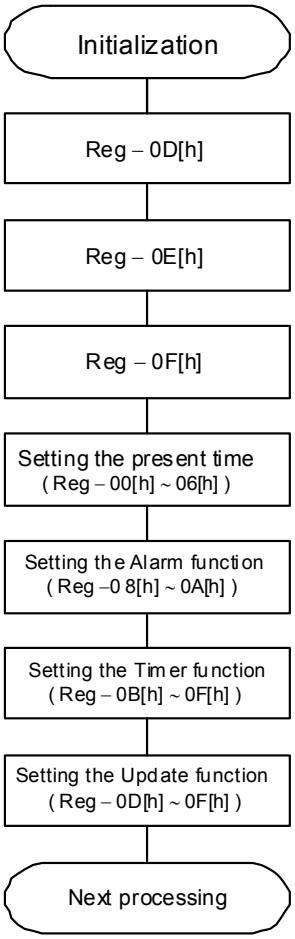
Note 3
The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz and 1024Hz output is possible.
But 1Hz output is disabled.

13.8. Flow-chart

The following flow-chart is one instance.
Mention for easy understanding takes precedence over others; therefore there are some inefficient cases for the actual processing. If you wish to take more efficient process, perform some processes at the same time or try to confirm and adjust some part where is no hindered from transposing of operation procedure. (Unnecessary processing may be included in mentioned items according to conditions to use.
To get movement according to your expectation, please surely adjust according to conditions to use (use environment).

1) An example of the initialization

Ex.1 Initialize



- Set TE bit to “0”.
- Set FSEL1, 0 bit optionally.

- Surely set TEST1, TEST2, and TEST3 bit to " 0 ".
- Clear VLF bit to “0”.

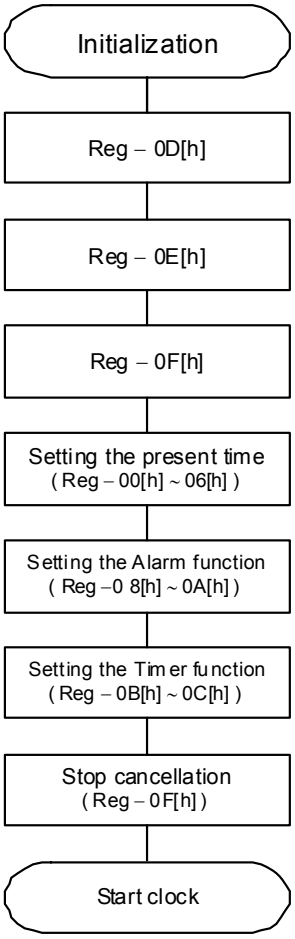
- Set AIE, TIE, UIE bit to “0 " to prevent unprepared interruption output.

- Set the present time.
  ∗ Setting the present time concerned, please refer to item of [Clock and calendar writing] .

- Set the Alarm interrupt function.
  When the alarm interrupt function is not being used, the Alarm registers (Reg - 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
- Set the fixed-cycle Timer function.
  When the fixed-cycle timer function is not being used, the fixed-cycle timer register (Reg – 0B to 0C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.
- Set the Update interrupt function.

∗ When initialization is finished, be sure to set STOP bit to “0”.

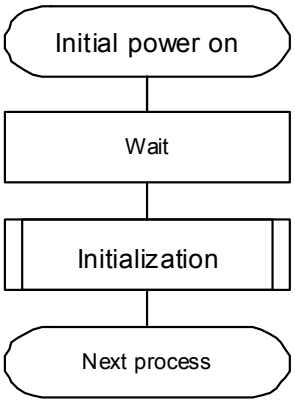
Ex.2 This example is use only for clock functions.



- Write 04[h]
- Write 00[h]
- Write 02[h]
  Set STOP bit to "1" to prevent timer update in time setting.
- Set the present time.
- The alarm function stops by initialization of Reg 0F[h].
  Reg - 08h to 0Ah can be used as a RAM register.
- The Timer function stops by initialization of Reg - 0E[h] and Reg – 0F[h].
  Reg – 0Bh to 0Ch can be used as a RAM register.
- Write 00[h]
  Cancel STOP bit to "0" and start (restart) clock.

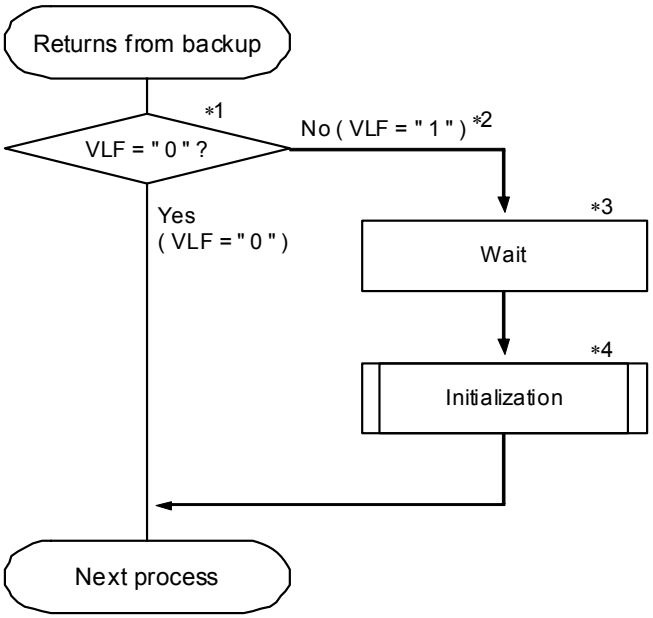
∗ When initialization is finished, be sure to set STOP bit to "0".

2) Processing example of the initial power on.



- Please wait time for oscillation of inner crystal oscillator.
  (The standard of waiting time concerned, please refer to the specification of oscillation start time (tSTA [s])
- Be sure to initialize all registers.
  (Please refer to item of [initialization]).

3) Processing when RTC returned from backup



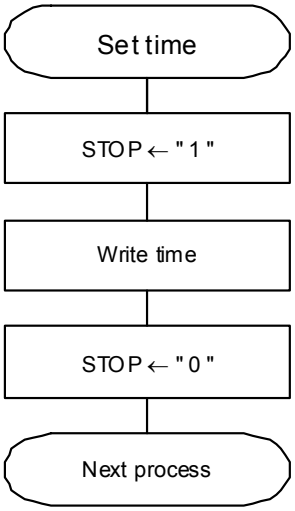
∗1) Check of a VLF bit

∗2) If VLF bit is "1", some abnormality may be occurred in backup (timer data and register setting are disappeared due to voltage dropping), please therefore surely initialize.

∗3) If power voltage is dropped, waiting time until inner crystal oscillator is oscillated again is needed.

∗4) Initialization concerned, please surely take initial setting of all register.
(Please refer to item of [initialization]).

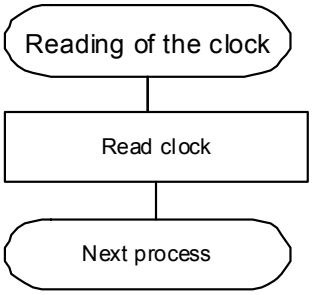
4) The setting of a clock and calendar



- Set STOP bit to "1" to prevent timer update in time setting.
- Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset). In case of initialization, please initialize all data.
- Cancel STOP bit to "0" and start (restart) timer movement. Timer is started when set STOP bit to "0".

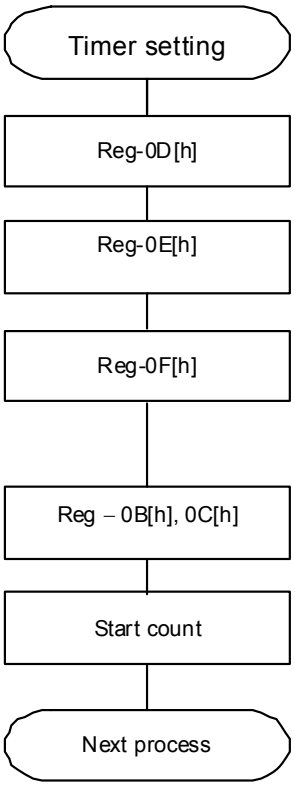
∗ It is able to set time even if not combined use of STOP bit. Please note that [clock is started at the time of writing [second]] in case STOP bit is not used.

5) The reading of a clock and calendar



- Please complete access within 0.95 seconds
  The STOP bit holds "0".
  (It causes the clock delay to set STOP bit to "1")
- At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.
- The access to a clock calendar recommends to have access to continuation by a auto increment function.

6) The setting example of the fixed-cycle timer interrupt function



- Clear TE bit to “0” to stop timer-interrupt function.
- The countdown period is fixed by the combination of the TSEL2, TSEL1, TSEL0 bit.

- Clear TF bit to “0” to cancel last timer interrupt output (/IRQ output).

- Select and set /IRQ output
  (if output “L” level interrupt output or not) when event occurs.
  If output “L” level interrupt output, set TIE bit to “1”.

- Set initial value of down counter.

- Set TE bit to "1" to start timer interrupt function.

When start timers interrupt function, please surely set/reset (*implement 2) initial value of down counter in advance.

∗1 Countdown is suspended with TSTP, " 0 " → " 1 " and countdown is performed again with TSTP, " 1 " → " 0 "

∗2 When you want to restart from a pre-set value, please set a TE bit to “1” again after setting a TE bit to “0”.

13.9. Reading/Writing Data via the I²C Bus Interface

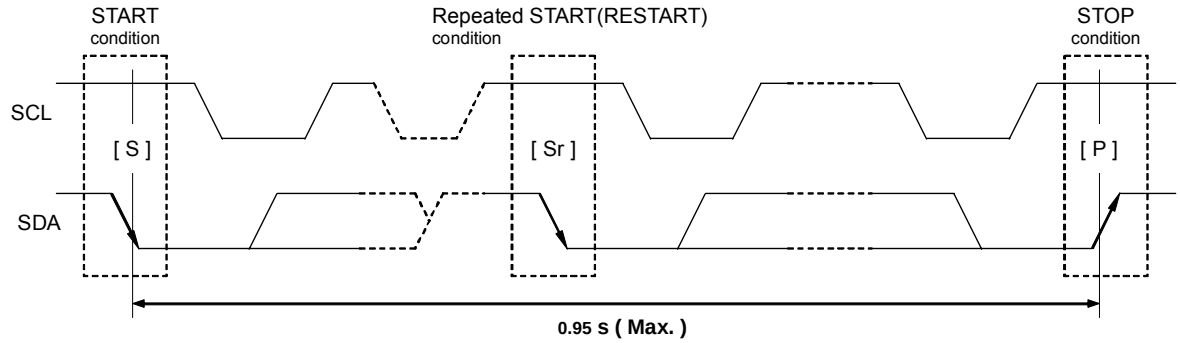
13.9.1. Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.
The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

13.9.2. Starting and stopping I²C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition
- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition
- This condition regulates how communications on the I²C -BUS are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)
- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

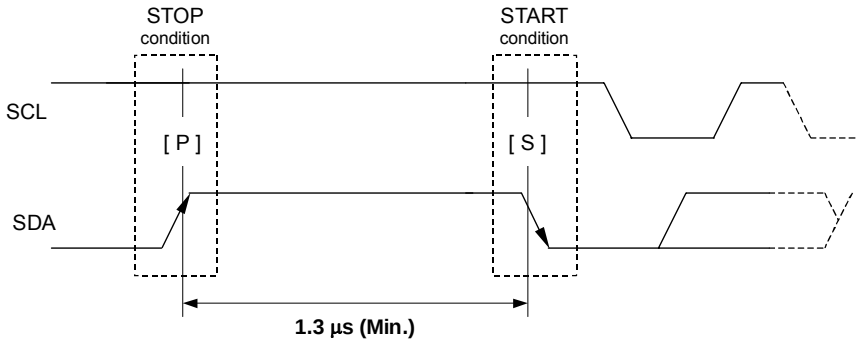
∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

∗3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within 0.95 seconds. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur within 0.95 seconds.)

If this series of operations requires 1 seconds or longer, the I²C bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1"). Restarting of communications begins with transfer of the START condition again

∗4) When communicating with this RTC module, wait at least 1.3 µs (see the tBUF rule) between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications).



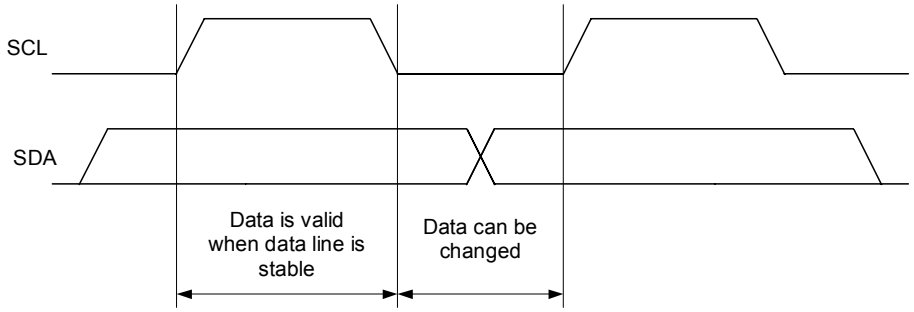
13.9.3. Data transfers and acknowledge responses during I^2C -BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. (However, the transfer time must be no longer than 0.95 seconds.)

The address auto increment function operates during both write and read operations.
After address Fh, incrementation goes to address 0h.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) receives data while the SCL line is at high level.

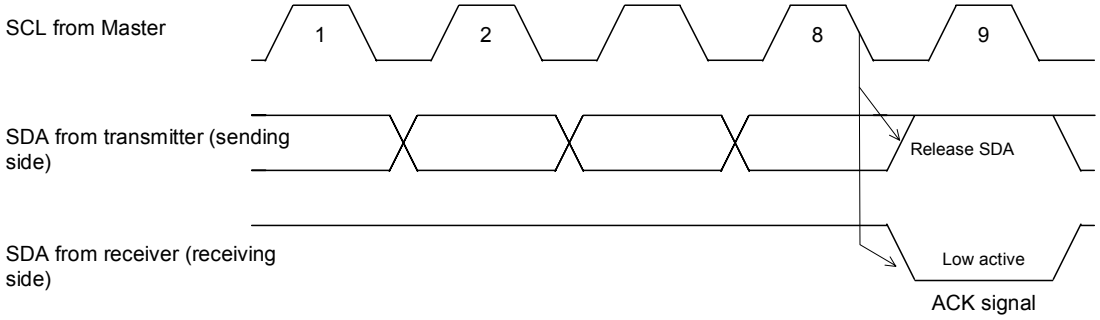


∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

13.9.4. Slave address

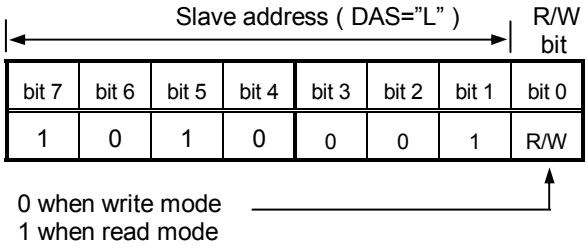
The I^2C-BUS devices do not have any chip select or chip enable pins. All I^2C-BUS devices are memorized with a fixed unique number in it. The chip selection on the I^2C-BUS is executed, when the interface starts, the master device send the required slave address to all devices on the I^2C-BUS. The receiving device only reacts for interfacing, when the required slave address is agreed with its own slave address.

In case, two RX-8571s are installed on a system, it is possible to select each device using DAS terminal logic level. Note that if more RX-8571s are installed, it is possible to access each device by using dynamic control to the DAS pins.

RX-8571 slave address

DAS pin	Slave address						
" H "	0	1	1	0	0	1	0
" L "	1	0	1	0	0	0	1

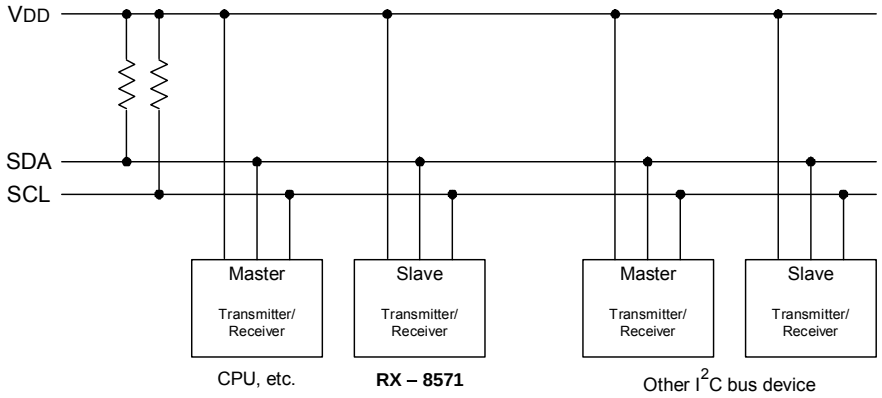
During in actual data transmission, the transmitted data contains the slave address and the data with R/W (read/write) bit.



13.9.5. System configuration

All ports connected to the I^2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the V_{DD} line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Any device that controls the data transmission and data reception is defined as a "Master".
and any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

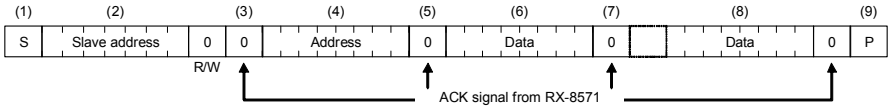
13.9.6. I²C bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RX-8581 is the slave.

1) Address specification write sequence

Since the RX-8571 includes an address auto increment function, once the initial address has been specified, the RX-8571 increments (by one byte) the receive address each time data is transferred.

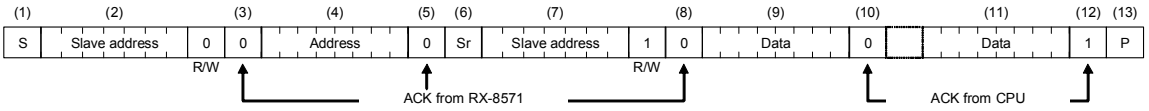
(1) CPU transfers start condition [S].
(2) CPU transmits the RX-8571's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX-8571.
(4) CPU transmits write address to RX-8571.
(5) Check for ACK signal from RX-8571.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RX-8571.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



2) Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

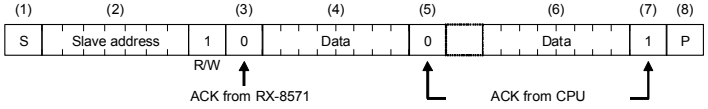
(1) CPU transfers start condition [S].
(2) CPU transmits the RX-8571's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX-8571.
(4) CPU transfers address for reading from 8571.
(5) Check for ACK signal from RX-8571.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RX-8571's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RX-8571 (from this point on, the CPU is the receiver and the RX-8571 is the transmitter).
(9) Data from address specified at (4) above is output by the RX-8571.
(10) CPU transfers ACK signal to RX-8571.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].



3) Read sequence when address is not specified

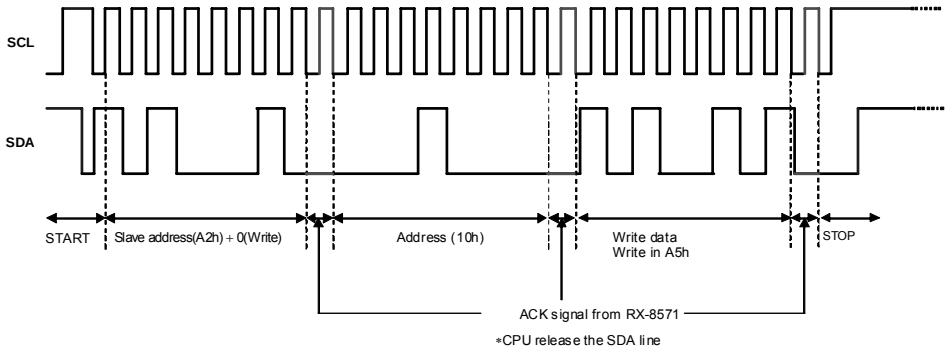
Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX-8571's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RX-8571 (from this point on, the CPU is the receiver and the RX-8571 is the transmitter).
(4) Data is output from the RX-8571 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RX-8571.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RX-8571.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].

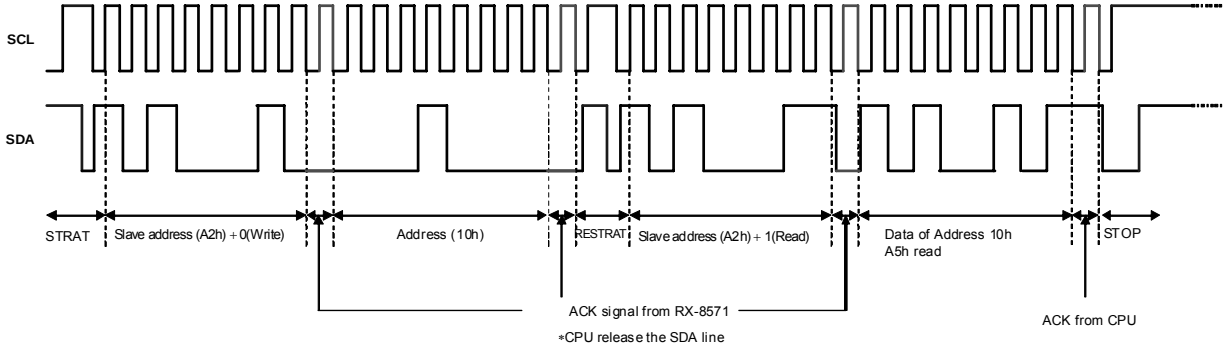


13.9.7. The example of the communication wave pattern

1) Address specification read sequence
When write in A5h for address 10h:



2) Address specification read sequence
When read A5h from address 10h:



EPSON TOYOCOM

Application Manual

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