MICROCHIP

TC1266

200mA PCI LDO

Features

- Glitch Free Transition Between Input Sources
- Automatic Input Source Selection
- External PMOS Bypass Switch Control
- Built-in 5V Detector
- 1% Regulated Output Voltage Accuracy
- 200mA Load Current Capability
- Kelvin Sense Input
- Low Dropout Voltage (240mV @ Full Load)
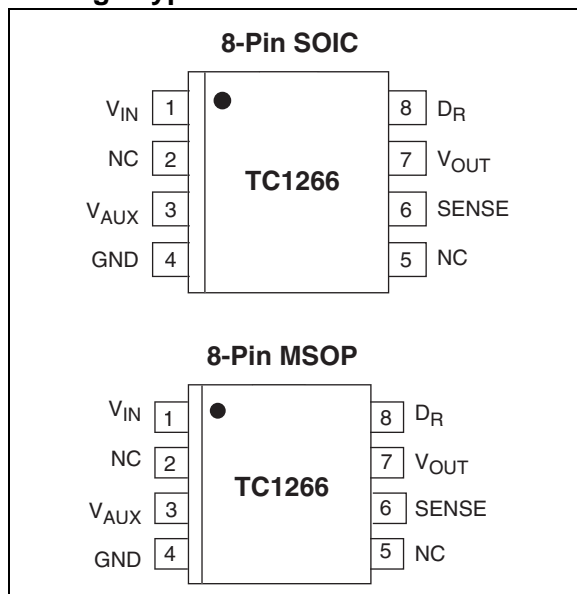- Low Ground Current, Independent of Load

Applications

- PCMCIA
- PCI
- Network Interface Cards (NICs)
- Cardbus™ Technology

Device Selection Table

Part Number	Package	Junction Temp. Range
TC1266VOA	8-Pin SOIC (Narrow)	-5°C to +125°C
TC1266VUA	8-Pin MSOP	-5°C to +125°C

Package Type

8-Pin SOIC

		TC1266		
V_{IN}	1		8	D_R
NC	2		7	V_{OUT}
V_{AUX}	3		6	SENSE
GND	4		5	NC

8-Pin MSOP

|		TC1266		
V_{IN}	1		8	D_R
NC	2		7	V_{OUT}
V_{AUX}	3		6	SENSE
GND	4		5	NC

General Description

The TC1266 is an application-specific, low dropout regulator (LDO), specifically intended for use in PCI peripheral card applications complying with PCI Power Management (PCI 2.0). It provides an uninterrupted, 3.3V, 200mA (max) output voltage when the main (5V) or auxiliary (3.3V) input voltage supplies are present.

The TC1266 consists of an LDO, a voltage threshold detector, external switchover logic and gate drive circuitry. It functions as a conventional LDO as long as the voltage on the main supply input (V_{IN}) is above the lower threshold (3.90V typical). Should the voltage on V_{IN} fall below the lower threshold, the LDO is disabled and an external P-channel MOSFET is automatically turned on, connecting the auxiliary supply input to $V_{OUT,}$ and ensuring an uninterrupted 3.3V output. The main supply is automatically selected, if both the main and auxiliary input supplies are present, and transition from one input supply to the other is ensured glitch-free. High integration, automatic secondary supply switchover, Kelvin sensing, and small size make the TC1266 the optimum LDO for PCI 2.0 applications.

Functional Block Diagram

TC1266
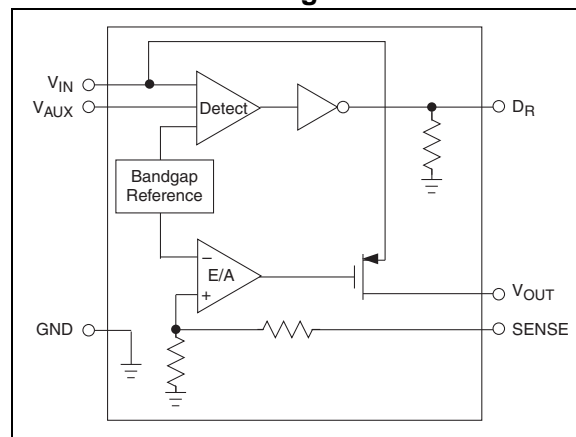
1.0   ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Input Supply Voltage (V_{IN})..............-0.5V to +7V (Max)

Auxiliary Supply Voltage (V_{AUX}) .....-0.5V to +7V (Max)

LDO Output Current (I_{OUT}).................................200mA

Thermal Impedance,
   Junction-to-Ambient (θ_{JA})............130°C/W for SOIC

ESD Rating .... 2 KV

Operating Temperature Range (T_A)........-5°C to +70°C

Storage Temperature Range (T_{STG})...-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC1266 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = +25°C, V_{IN} = 5V, V_{AUX} = 3.3V, I_{OUT} = 0.1mA, C_{OUT} = 4.7μF, unless otherwise noted. **Boldface** type specifications apply over full operating temperature range.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IN}	Supply Voltage	**4.3**	**5.0**	**5.5**	V	V_{AUX} = 0V
I_{GND}	Ground Current	—	230	**450**	μA	V_{AUX} = 0V **(Note 6)**
		—	260	**500**		V_{AUX} = 3.3V **(Note 6)**
I_{VIN}	Reverse Leakage from V_{AUX}	—	-0.1	**-1.0**	μA	V_{AUX} = 3.6V, V_{IN} = 0V, I_{OUT} = 0mA
V_{AUX}	Supply Voltage	**3.0**	**3.3**	**3.6**	V	
$I_{Q(AUX)}$	Quiescent Current	—	50	70	μA	V_{IN} = 0V, I_{OUT} = 0mA
		—	—	**100**		
		—	60	80	μA	V_{IN} = 5V, I_{OUT}= 0mA
		—	—	**120**		
I_{VAUX}	Reverse Leakage from V_{IN}	—	-0.1	**-1.0**	μA	V_{IN} = 5,5V, V_{AUX} = 0V, I_{OUT} = 0mA
$V_{TH(LO)}$	5V Detector Low Threshold Voltage	—	3.90	—	V	V_{IN} Falling **(Notes 2, 3)**
		3.75	—	**4.05**		
V_{HYST}	5V Detector Hysteresis Voltage	—	260	—	mV	**(Notes 2, 3)**
		200	—	**300**		
$V_{TH(HI)}$	5V Detector High Threshold Voltage	—	4.15	—	V	V_{IN} Rising **(Notes 2, 3)**
		4.0	—	**4.30**		
V_{OUT}	LDO Output Voltage	—	3.300	—	V	I_{OUT} = 20mA
		3.234	—	**3.366**		4.3V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 200mA
		3.000	—	—		3.75V ≤ V_{IN} ≤ 4.3V, 0mA ≤ I_{OUT} ≤ 200mA **(Note 4)**
I_{OUT}	Output Current	200	—	—	mA	
$REG_{(LINE)}$	Line Regulation	—	0.05	—	%	V_{IN} = 4.3V to 5.5V
		-0.5	—	**0.5**		
$REG_{(LOAD)}$	Load Regulation	—	0.05	—	%	I_{OUT}= 0.1mA to 200mA
		-0.5	—	**0.5**		

Note   1:   Ensured by design.
   2:   See 5V Detect Thresholds, Figure 4-1.
   3:   Recommended source impedance for 5V supply: ≤ 0.25Ω. This will ensure that I_{OUT} x R_{SOURCE} < V_{HYST}, thus avoiding D_R toggling during 5V detect threshold transitions.
   4:   In Application Circuit, Figure 3-1.
   5:   See Timing Diagram, Figure 4-2.
   6:   Ground Current is independent of I_{LOAD}.

TC1266 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: T_A = +25°C, V_{IN} = 5V, V_{AUX} = 3.3V, I_{OUT} = 0.1mA, C_{OUT} = 4.7μF, unless otherwise noted. **Boldface** type specifications apply over full operating temperature range.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{DR}	Drive Voltage	V_{IN} - 0.2 **V_{IN} - 0.3**	V_{IN} - 0.1 —	— —	V	$4.3V \leq V_{IN} \leq 5.5V$, I_{DR} = 200μA
		— —	35 —	150 **200**	mV	$V_{IN} < V_{TH(LO)}$, I_{DR} = 200μA
$I_{DR(PK)}$	Peak Drive Current	7 **6**	— —	— —	mA	Sinking: V_{IN} = 3.75V, V_{DR} = 1V; Sourcing: V_{IN} = 4.3V, $V_{IN} - V_{DR}$ = 2V
t_{DH}	Drive High Delay **(Notes 1, 5)**	— —	4 —	— **8**	μsec	C_{DR} = 1.2nF, V_{IN} ramping up, measured from $V_{IN} = V_{TH(HI)}$ to V_{DR} = 2V
t_{DL}	Drive Low Delay **(Notes 1, 5)**	— —	0.6 —	1.5 **3.0**	μsec	C_{DR} = 1.2nF, V_{IN} ramping down, measured from $V_{IN} = V_{TH(LO)}$ to V_{DR} = 2V

Note 1: Ensured by design.
2: See 5V Detect Thresholds, Figure 4-1.
3: Recommended source impedance for 5V supply: $\leq 0.25\Omega$. This will ensure that I_{OUT} x R_{SOURCE} < V_{HYST}, thus avoiding D_R toggling during 5V detect threshold transitions.
4: In Application Circuit, Figure 3-1.
5: See Timing Diagram, Figure 4-2.
6: Ground Current is independent of I_{LOAD}.
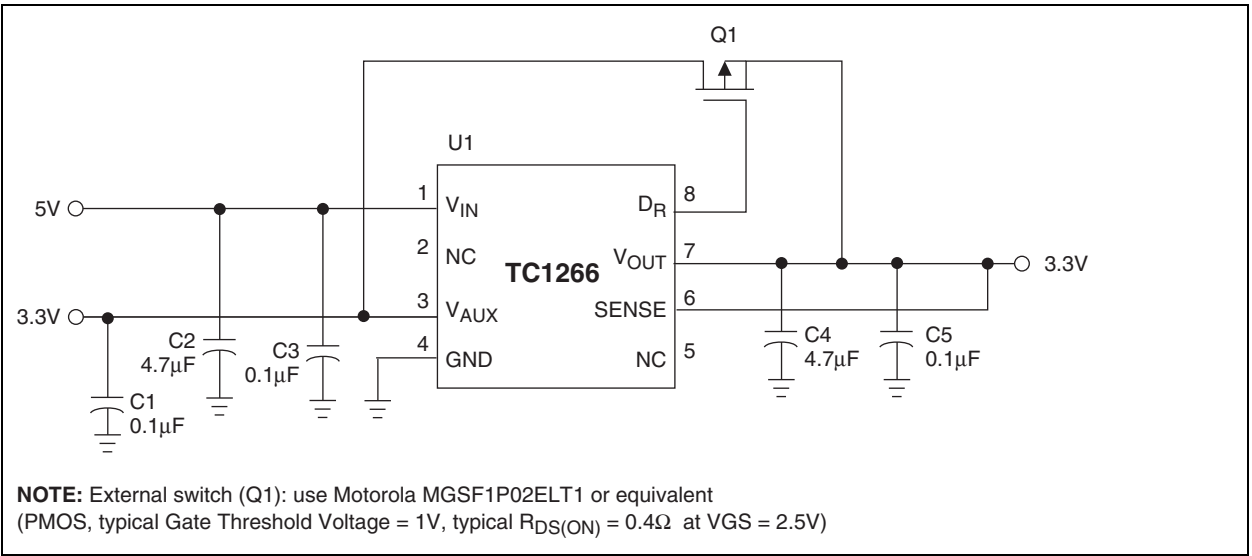
TC1266

2.0   PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1:   PIN FUNCTION TABLE

Pin No. (8-Pin SOIC) (8-Pin MSOP)	Symbol	Description
1	V_{IN}	Main input supply for the TC1266, nominally 5V.
2	NC	Not connected.
3	V_{AUX}	Auxiliary input supply, nominally 3.3V.
4	GND	Logic and power ground.
5	NC	Not connected.
6	SENSE	Sense pin for V_{OUT}. Connect to V_{OUT} at the load to minimize voltage drop across PCB traces.
7	V_{OUT}	LDO 3.3V output.
8	D_R	Driver output for external P-channel MOSFET pass element.

3.0   DETAILED DESCRIPTION

FIGURE 3-1:   APPLICATION CIRCUIT

NOTE: External switch (Q1): use Motorola MGSF1P02ELT1 or equivalent
(PMOS, typical Gate Threshold Voltage = 1V, typical $R_{DS(ON)}$ = 0.4Ω at VGS = 2.5V)

4.0   THERMAL CONSIDERATIONS

4.1   Thermal Shutdown

Integrated thermal protection circuitry shuts the regulator off when die temperature exceeds 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

4.2   Power Dissipation

The amount of power the regulator dissipates is primarily a function of input and output voltage, and output current. The following equation is used to calculate worst case actual power dissipation:

EQUATION 4-1:

$$P_D \approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$$

Where:

P_D = Worst case actual power dissipation
V_{INMAX} = Maximum voltage on V_{IN}
V_{OUTMIN} = Minimum regulator output voltage
$I_{LOADMAX}$ = Maximum output (load) current

The maximum allowable power dissipation (Equation 4-2) is a function of the maximum ambient temperature (T_{AMAX}), the maximum allowable die temperature (T_{JMAX}) and the thermal resistance from junction-to-air (θ_{JA}).

EQUATION 4-2:

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

Where all terms are previously defined.

Equation 4-1 can be used in conjunction with Equation 4-2 to ensure regulator thermal operation is within limits. For example:

Given:

V_{INMAX} = 5V ± 5%
V_{OUTMIN} = 3.217V
$I_{LOADMAX}$ = 200mA
T_{JMAX} = 125°C
T_{AMAX} = 70°C
θ_{JA} = 130°C/W (SOIC)

Find: 1. Actual power dissipation
2. Maximum allowable dissipation

Actual power dissipation:

$P_D \approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$

= (5.25V - 3.217V) 200mA
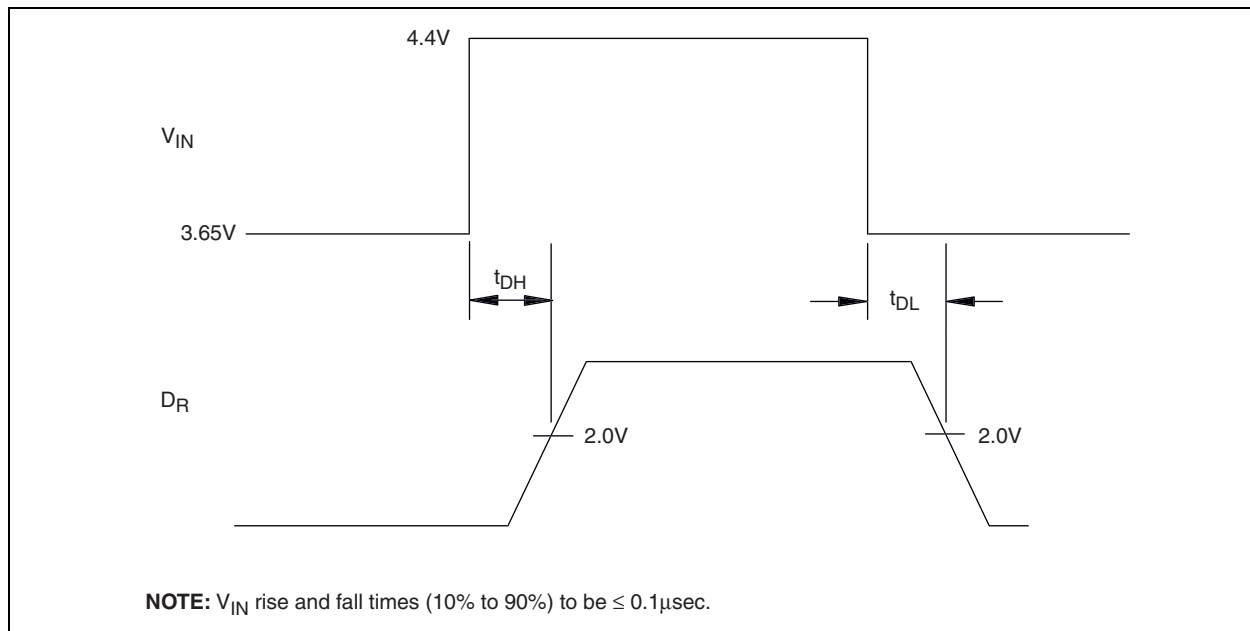
= 407mW

Maximum allowable power dissipation:

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

$$= \frac{(125 - 70)}{130}$$

= 423mW

In this example, the TC1266 dissipates a maximum of 407mW; below the allowable limit of 423mW.

TC1266

FIGURE 4-1: **5V DETECT THRESHOLD**
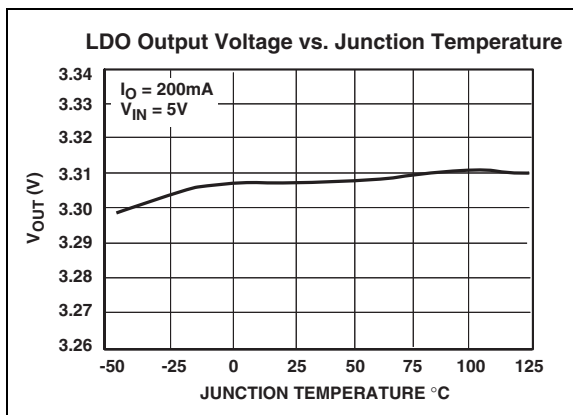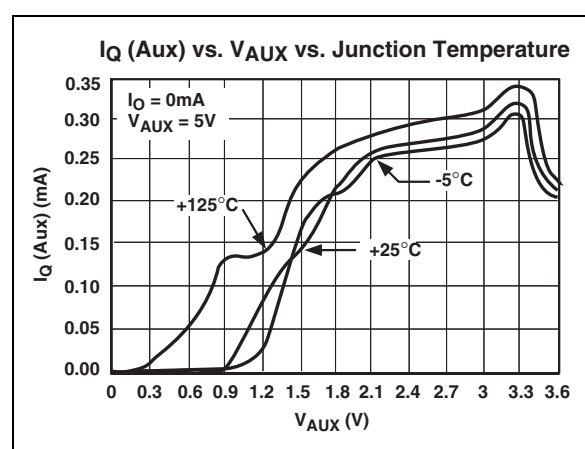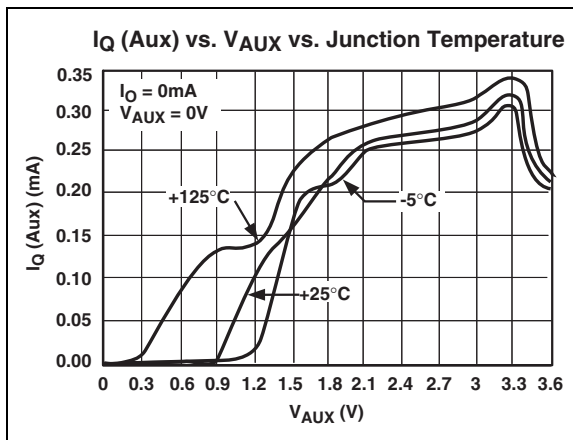

NOTE: V_{IN} rise and fall times (10% to 90%) to be $\geq$ 100µsec.
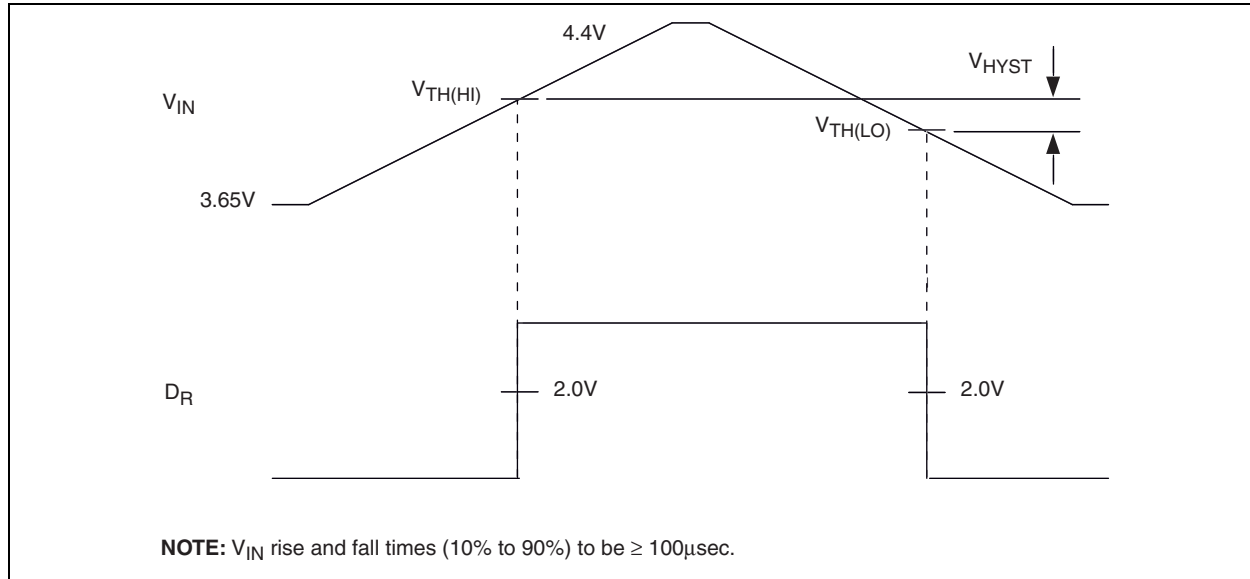
FIGURE 4-2: **TIMING DIAGRAM**

NOTE: V_{IN} rise and fall times (10% to 90%) to be $\leq$ 0.1µsec.
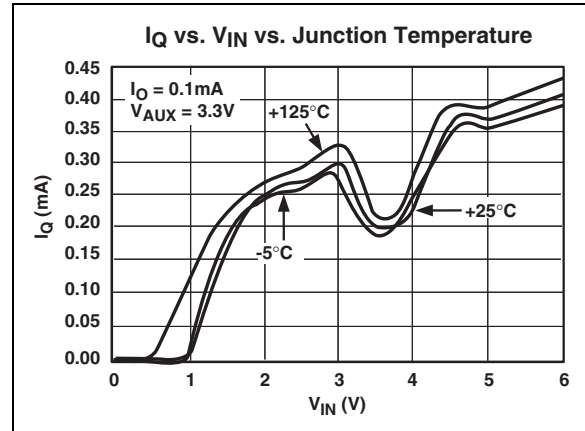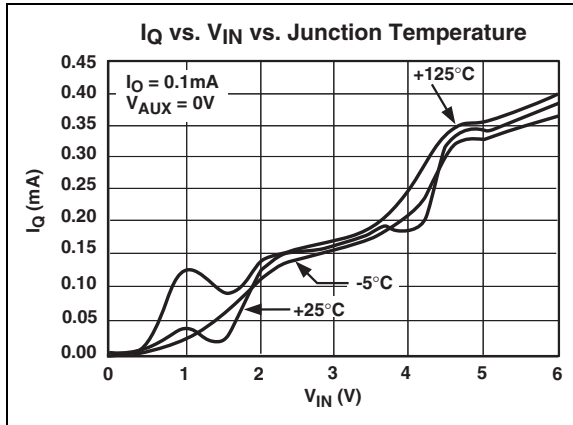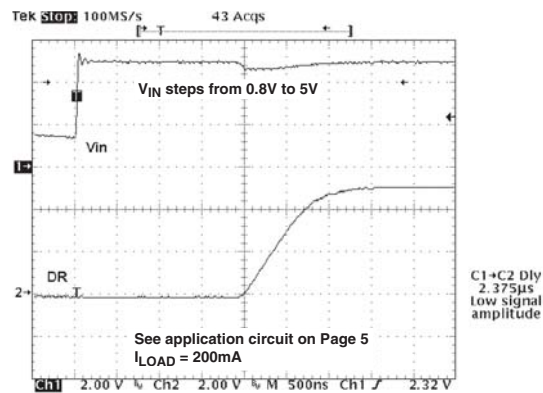
5.0   TYPICAL CHARACTERISTICS

> **Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

I_Q vs. V_{IN} vs. Junction Temperature

$I_O = 0.1mA$
$V_{AUX} = 0V$

I_Q vs. V_{IN} vs. Junction Temperature

$I_O = 0.1mA$
$V_{AUX} = 3.3V$

I_Q (Aux) vs. V_{AUX} vs. Junction Temperature

$I_O = 0mA$
$V_{AUX} = 0V$

I_Q (Aux) vs. V_{AUX} vs. Junction Temperature

$I_O = 0mA$
$V_{AUX} = 5V$

LDO Output Voltage vs. Junction Temperature

$I_O = 200mA$
$V_{IN} = 5V$

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5.0   TYPICAL CHARACTERISTICS (CONTINUED)

Drive High Delay

Trace 1: V_{IN} stepping for 0.8V to 5V
Trace 2: D_R going high at $V_{TH(HI)}$
TDH = < 4µS

Drive Low Delay
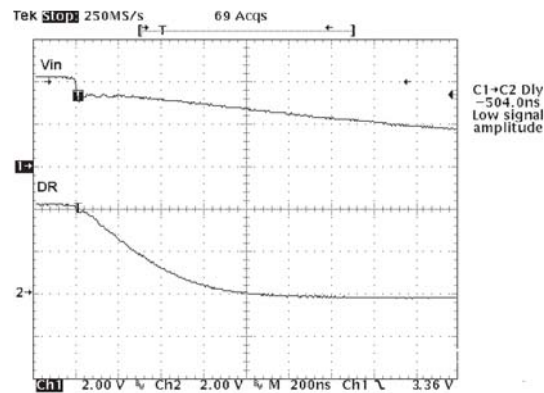
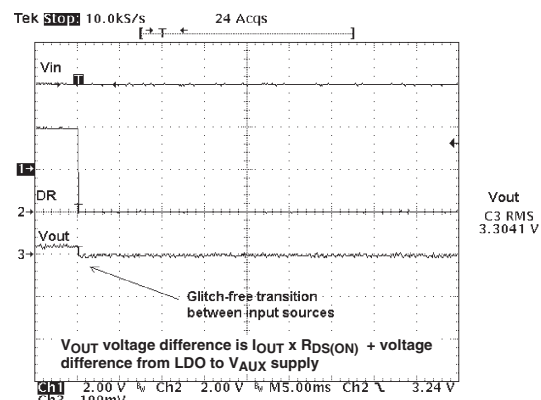

Trace 1: V_{IN} stepping for 5.5V to 0V
Trace 2: D_R going low
TDL = < 600nS

V_O (min) with V_{IN} Rising
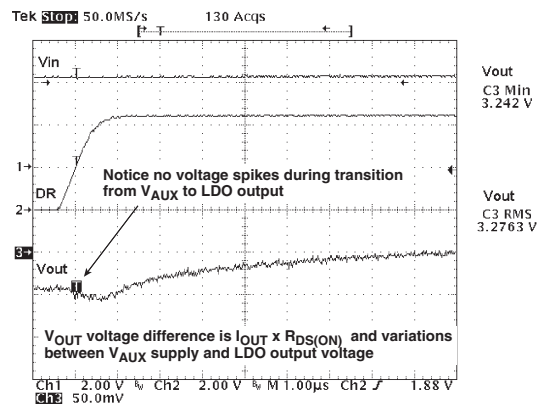
Trace 1: V_{IN} – 3A charging a 1500µF capacitor
Trace 2: D_R going high at $V_{TH(HI)}$
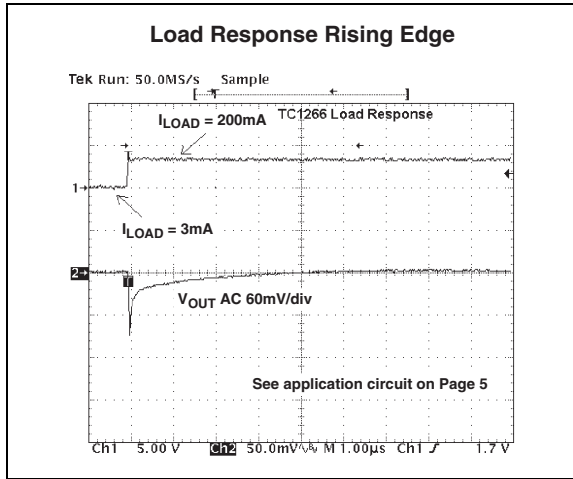Trace 3: V_{OUT}, offset 3.3V. $V_{OUT(min)}$ = 3.24V
I_{LOAD} = 200µA

V_O (min) with V_{IN} Falling

Trace 1: V_{IN} – discharging a 1500µF capacitor
Trace 2: D_R going low at $V_{TH(LO)}$
Trace 3: V_{OUT}, offset 3.3V. $V_{OUT(min)}$ = 3.14V
I_{LOAD} = 200µA

5.0   TYPICAL CHARACTERISTICS (CONTINUED)

Load Response Rising Edge
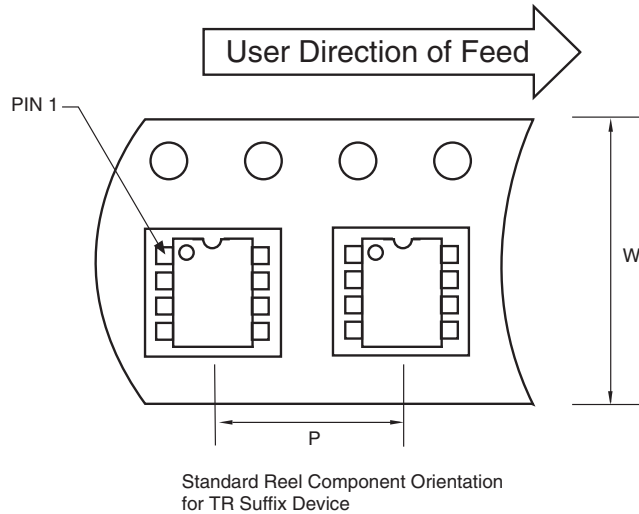

Load Response Falling Edge

TC1266
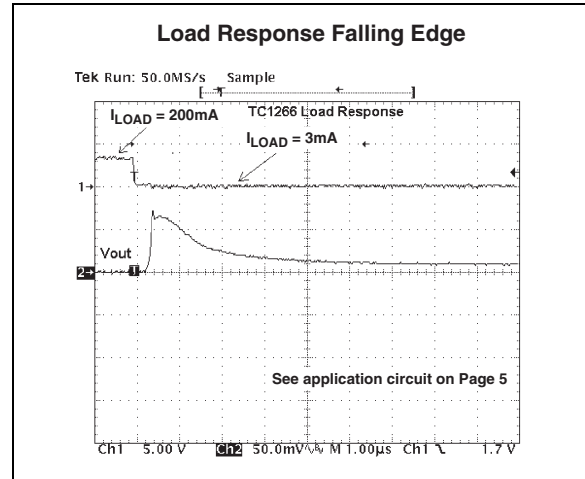
6.0   PACKAGING INFORMATION

6.1   Package Marking Information

Package marking data not available at this time.

6.2   Taping Form

Component Taping Orientation for 8-Pin MSOP Devices

User Direction of Feed

PIN 1
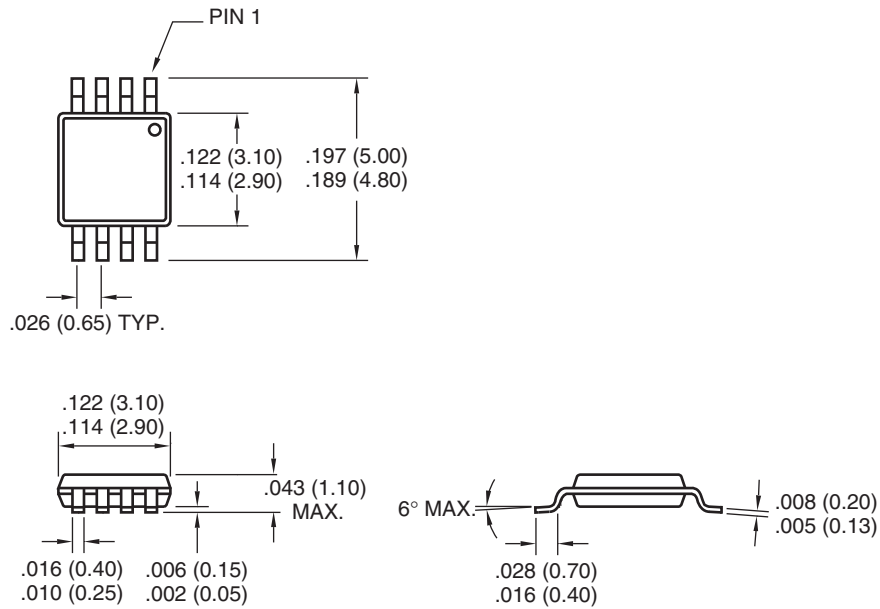
W

P

Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices
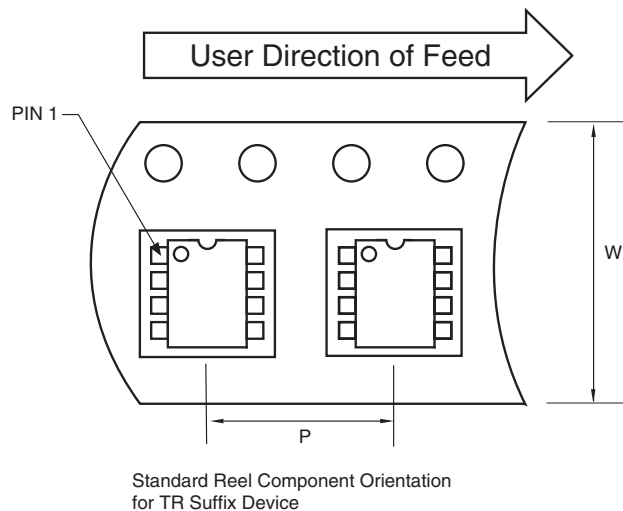
User Direction of Feed

PIN 1

W

P

Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

6.3 Package Dimensions

8-Pin MSOP

PIN 1

.122 (3.10)   .197 (5.00)
.114 (2.90)   .189 (4.80)

.026 (0.65) TYP.

.122 (3.10)
.114 (2.90)

.043 (1.10)
MAX.

6° MAX.

.008 (0.20)
.005 (0.13)

.016 (0.40)   .006 (0.15)
.010 (0.25)   .002 (0.05)

.028 (0.70)
.016 (0.40)

Dimensions: inches (mm)

TC1266

8-Pin SOIC

PIN 1

.157 (3.99)
.150 (3.81)

.244 (6.20)
.228 (5.79)

.050 (1.27) TYP.

.197 (5.00)
.189 (4.80)

.069 (1.75)
.053 (1.35)

8° MAX

.010 (0.25)
.007 (0.18)

.020 (0.51)
.013 (0.33)

.010 (0.25)
.004 (0.10)

.050 (1.27)
.016 (0.40)
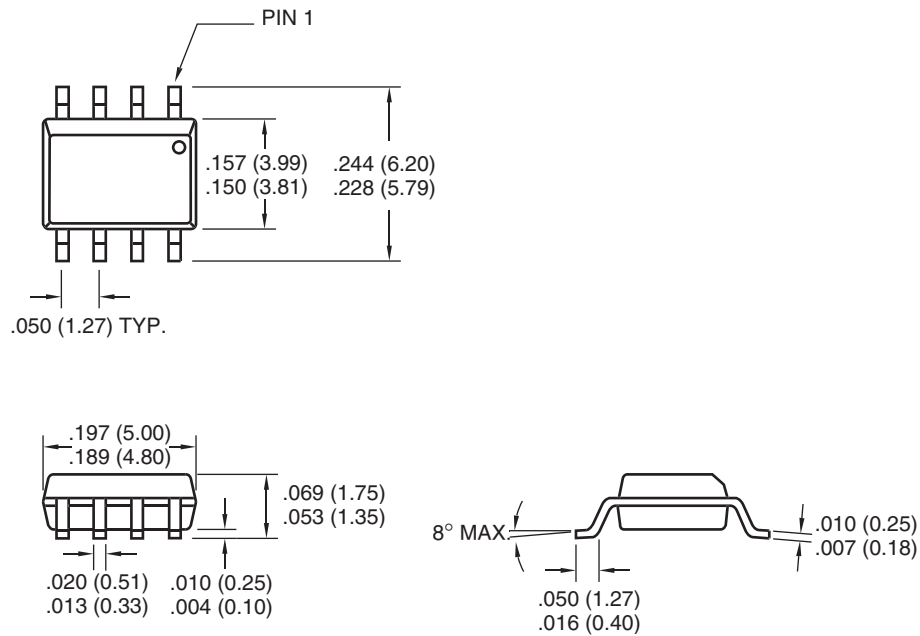
Dimensions: inches (mm)

7.0 REVISION HISTORY

Revision C (November 2012)

Added a note to each package outline drawing.

NOTES:

SALES AND SUPPORT

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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