2N4921G, 2N4922G, 2N4923G

Medium-Power Plastic NPN Silicon Transistors

These high−performance plastic devices are designed for driver circuits, switching, and amplifier applications.

Features

- Low Saturation Voltage
- Excellent Power Dissipation Due to Thermopad™ Construction
- Excellent Safe Operating Area
- Complement to PNP 2N4918, 2N4919, 2N4920
- These Devices are Pb−Free and are RoHS Compliant**

ON Semiconductor®

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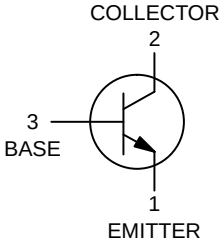
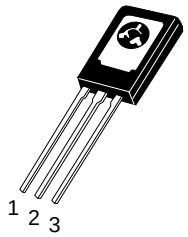
1.0 AMPERE GENERAL PURPOSE POWER TRANSISTORS 40−80 VOLTS, 30 WATTS





TO−225
CASE 77
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage 2N4921G 2N4922G 2N4923G	V_{CEO}	 40 60 80	Vdc
Collector−Emitter Voltage 2N4921G 2N4922G 2N4923G	V_{CB}	 40 60 80	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous (Note 1)	I_C	1.0	Adc
Collector Current − Peak (Note 1)	I_{CM}	3.0	Adc
Base Current − Continuous	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 30 0.24	 W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The 1.0 A maximum I_C value is based upon JEDEC current gain requirements. The 3.0 A maximum value is based upon actual current handling capability of the device (see Figures 5 and 6).

THERMAL CHARACTERISTICS (Note 2)

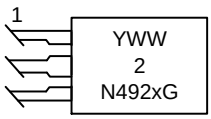
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	4.16	°C/W

2. Recommend use of thermal compound for lowest thermal resistance.

*Indicates JEDEC Registered Data.

** For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM



Y = Year
WW = Work Week
2N492x = Device Code
x = 1, 2, or 3
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
2N4921G	TO−225 (Pb−Free)	500 Units / Box
2N4922G	TO−225 (Pb−Free)	500 Units / Box
2N4923G	TO−225 (Pb−Free)	500 Units / Box

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 0.1 Adc, I_B = 0) 2N4921G 2N4922G 2N4923G	$V_{CEO(sus)}$	 40 60 80	 − − −	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4921G (V_{CE} = 30 Vdc, I_B = 0) 2N4922G (V_{CE} = 40 Vdc, I_B = 0) 2N4923G	I_{CEO}	 − − −	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C	I_{CEX}	 − −	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	 −	 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	 −	 1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	 40 30 10	 − 150 −	−
Collector−Emitter Saturation Voltage (Note 3) (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	 −	 0.6	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	 −	 1.3	Vdc
Base−Emitter On Voltage (Note 3) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	 −	 1.3	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	 3.0	 −	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	 −	 100	pF
Small−Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	 25	 −	−

3. Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.

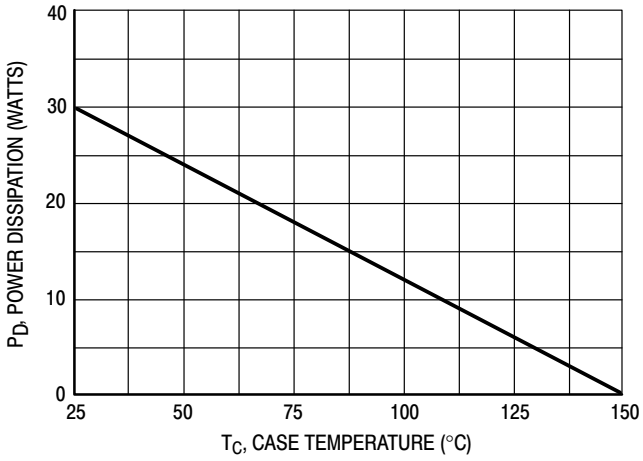


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

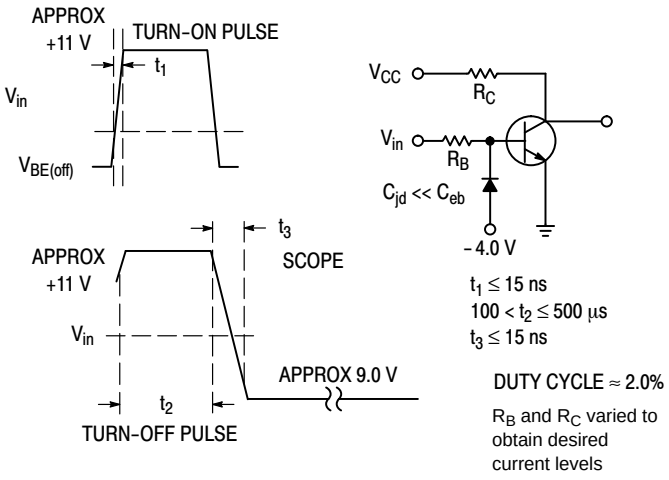


Figure 2. Switching Time Equivalent Circuit

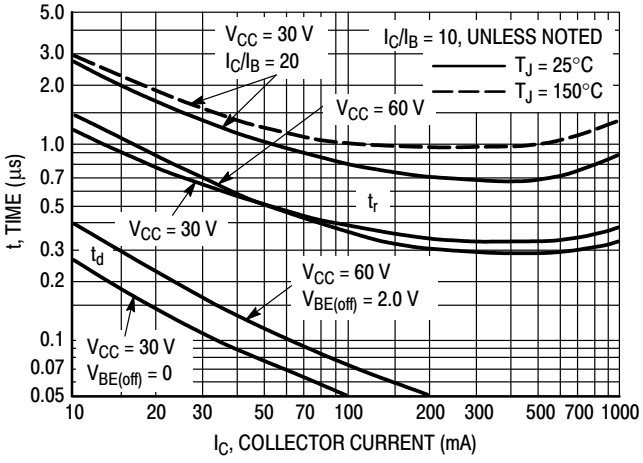


Figure 3. Turn−On Time

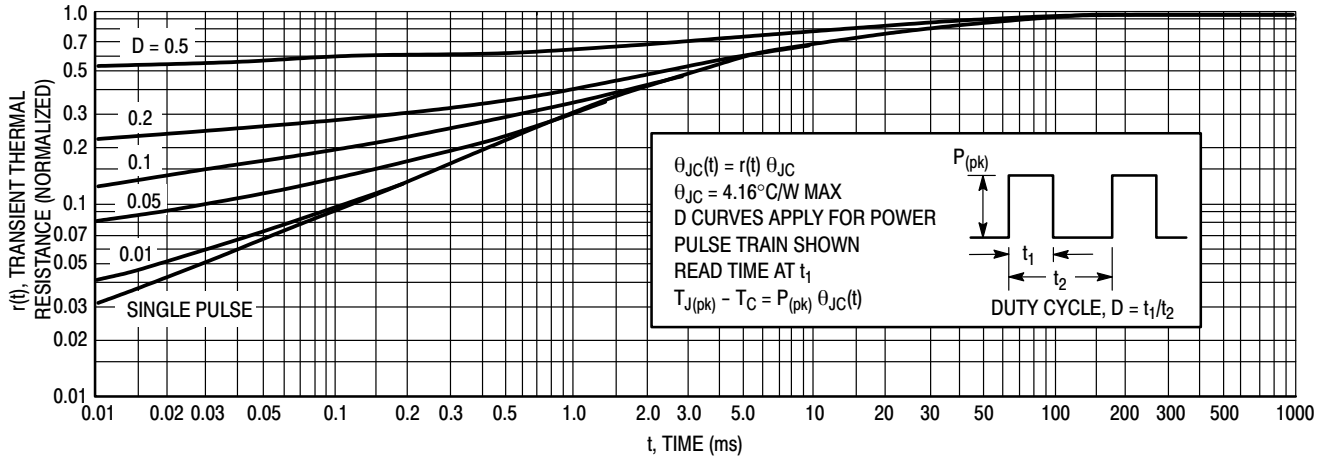


Figure 4. Thermal Response

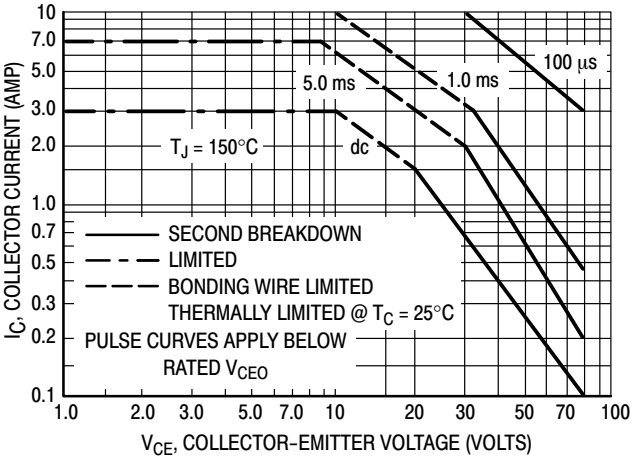


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

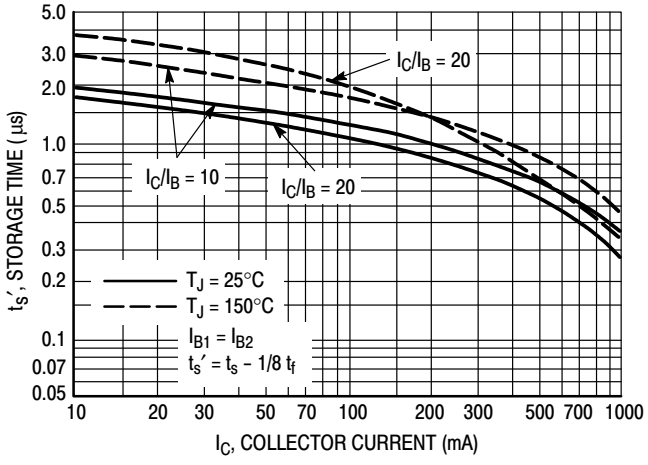


Figure 6. Storage Time

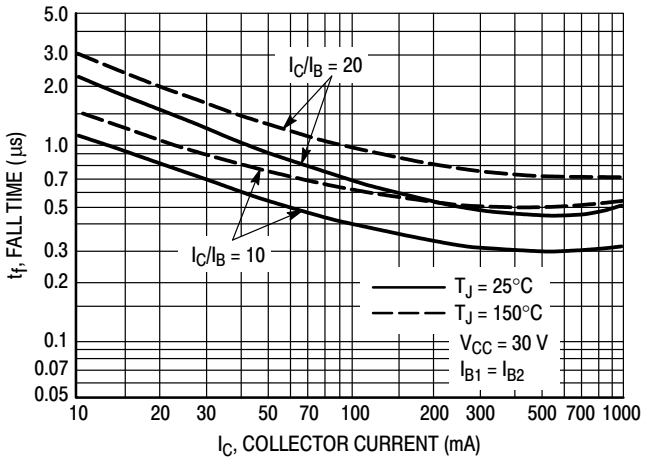


Figure 7. Fall Time

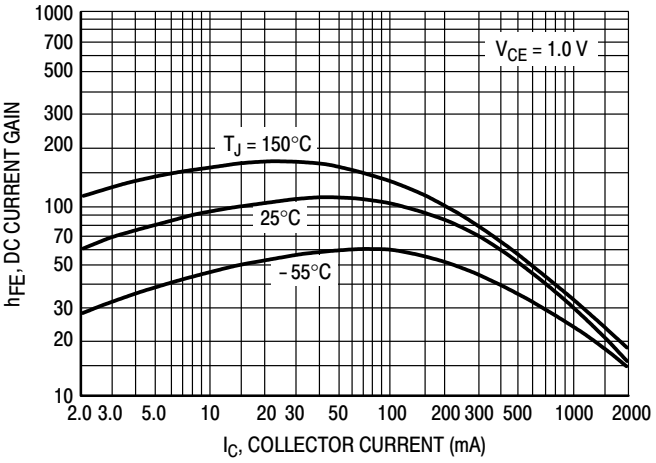


Figure 8. Current Gain

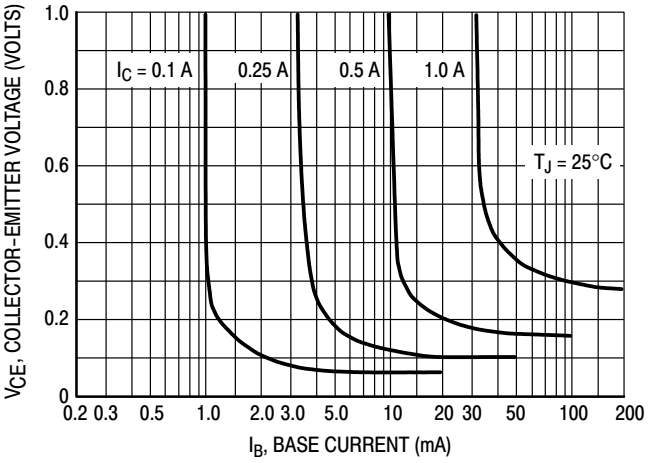


Figure 9. Collector Saturation Region

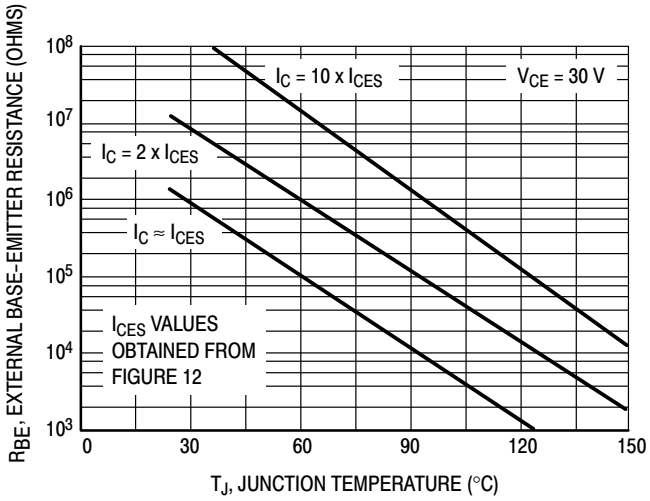


Figure 10. Effects of Base−Emitter Resistance

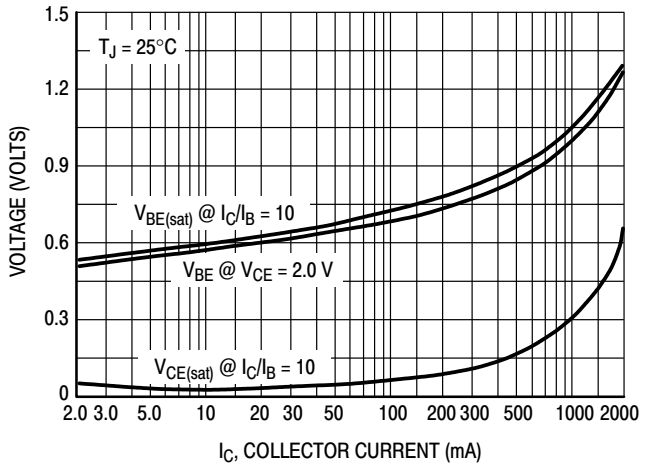


Figure 11. “On” Voltage

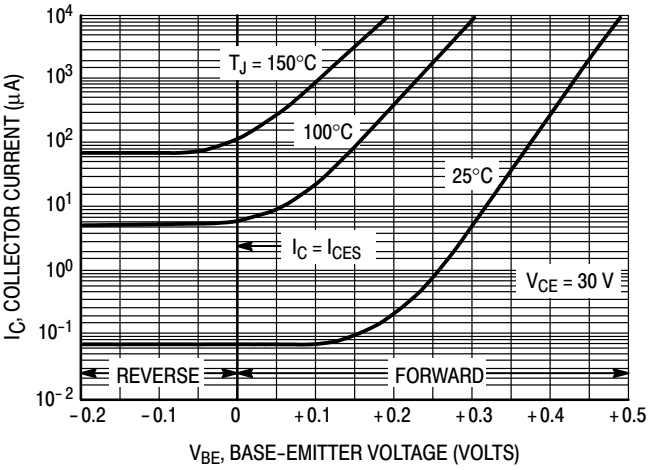


Figure 12. Collector Cut−Off Region

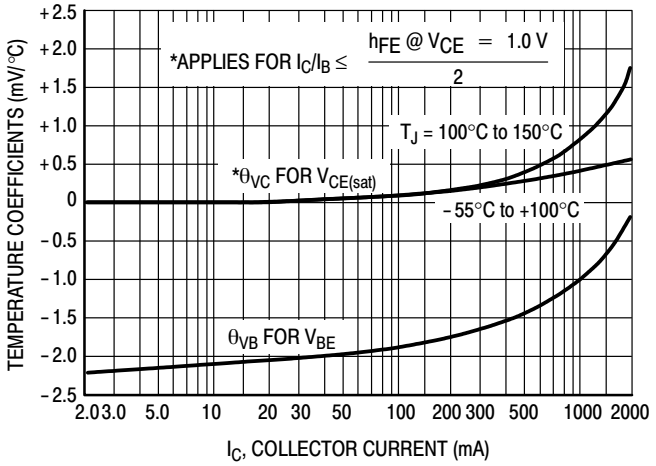
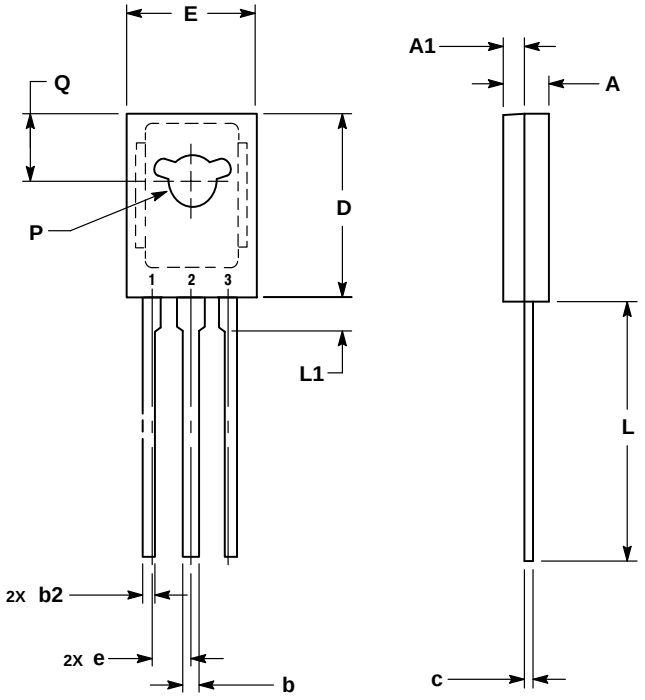


Figure 13. Temperature Coefficients

PACKAGE DIMENSIONS

TO−225
CASE 77−09
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

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PUBLICATION ORDERING INFORMATION

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