ispMACH 4000

The Industry's Fastest and Lowest Power CPLDs

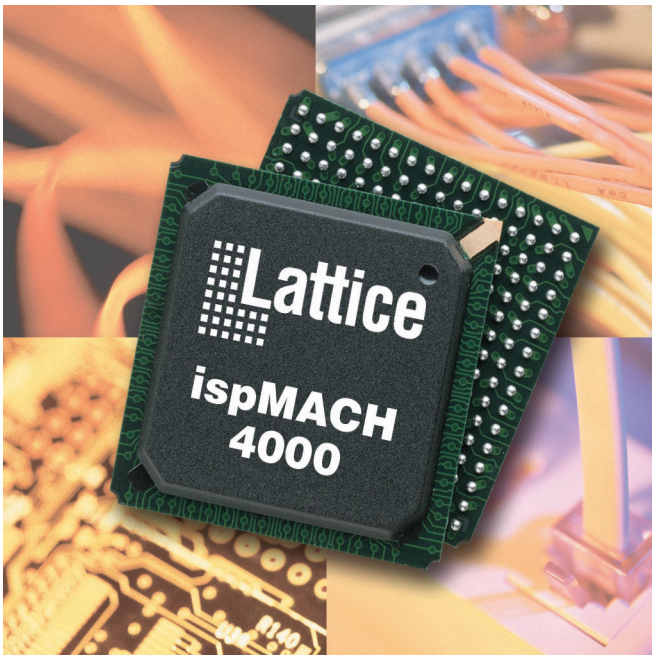
New CPLD Architecture Couples Super-FAST Performance and Low Power

The ispMACH™ 4000 is the industry's fastest and lowest power ISP™ Complex Programmable Logic Device (CPLD) Family. With a SuperFAST™ 2.5ns pin-to-pin delay and low dynamic power, the ispMACH 4000 Family is the ultimate solution for high performance systems.

The ispMACH 4000 family contains three separate sub-families, supporting 3.3V (ispMACH 4000V), 2.5V (ispMACH 4000B), and 1.8V (ispMACH 4000C).

Utilizing Lattice's latest generation E²CMOS® process technology, the ispMACH 4000 architecture combines the best features of Lattice's ispMACH4A and ispLSI® 2000 families and provides high speed, low dynamic power consumption, enhanced logic control, and flexible I/O.

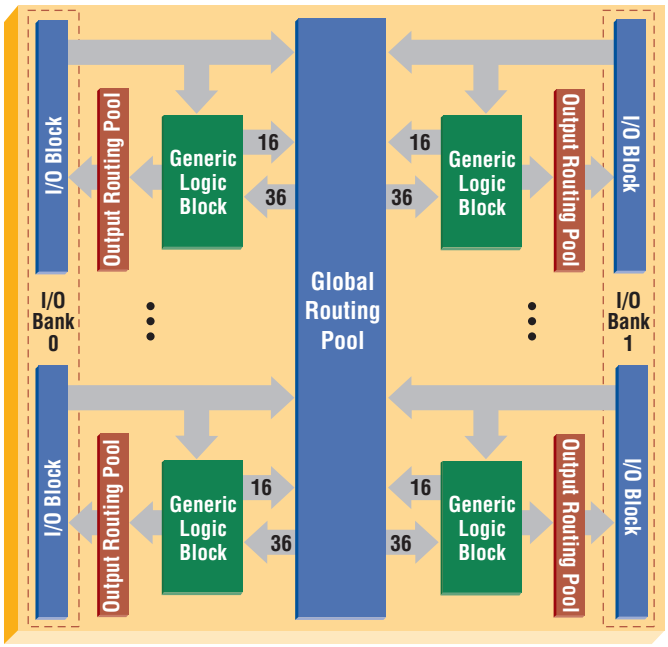
The new ispMACH 4000 Family is fully supported by Lattice's easy-to-use and powerful ispLEVER® design software, plus a wide range of popular third-party tools. Designing with ispMACH 4000 devices is quick and easy using leading synthesis and simulation tools from Exemplar Logic, Synplicity and Model Technology.



Key Features and Benefits

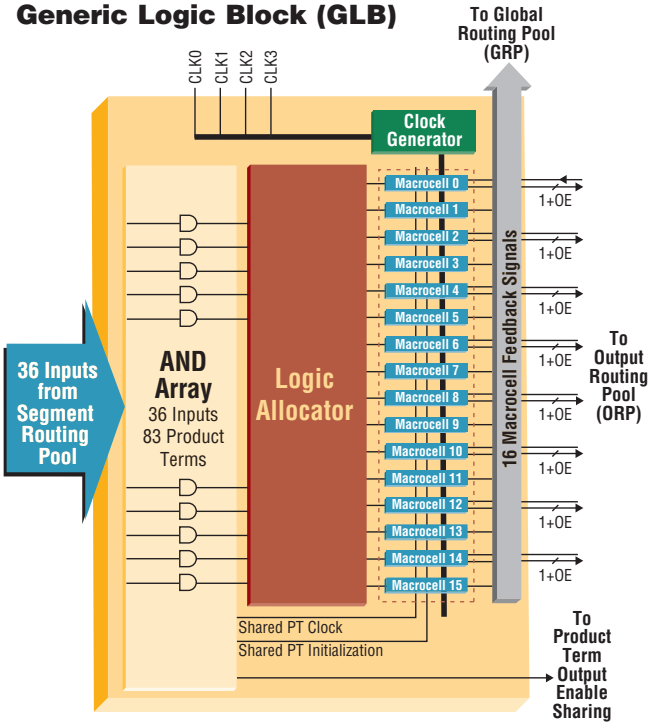
- **SuperFAST Performance**
  - 2.5 ns t_{PD} Pin-to-Pin Delay
  - 400 MHz System Performance
- **Industry's Lowest Power Consumption**
  - 1.8V Core for Low Dynamic Power
  - Low Static Current
    - 1.3-3 mA (1.8V Device Family)
    - 11.3-13 mA (2.5V and 3.3V Device Families)
- **Multiple Temperature Range Options**
  - Commercial: 0 to 70° C T_A (Ambient)
  - Industrial: -40 to 85° C T_A (Ambient)
  - Automotive: -40 to 125° C T_A (Ambient)
- **Ease of Design**
  - Excellent First-Time Fit and Refit Capability
  - 4 Global Clocks
  - 36 Inputs per Logic Block
  - Up to 80 Product Terms (PT) per Output
  - ORP for Pin Locking
  - Density Migration
  - Flexible Control, Clocking and OE
  - Fast, SpeedLocking™, and Wide PT Paths
  - 5V Tolerant Inputs and I/O
- **Easy System Integration**
  - Operation with 1.8V, 2.5V and 3.3V Supplies
  - 1.8V, 2.5V, 3.3V I/O Support
  - IEEE 1532 In-System Programmable (ISP™)
  - IEEE 1149.1 Boundary Scan Test
  - Open Drain Output for Flexible Bus Interface Capability
  - Programmable Pull-Up or Bus-Keeper Inputs
  - Hot Socketing Capability
  - 3.3V PCI Compatible
  - Programmable Output Slew Rate
  - Lead-free Package Options

ispMACH 4000 Block Diagram

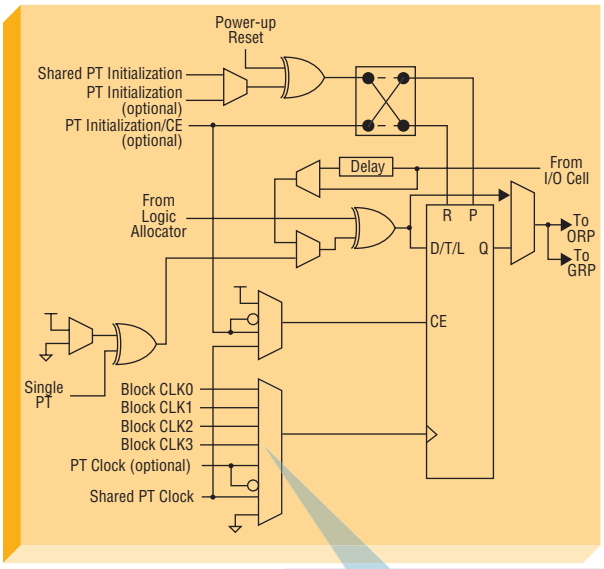


ispMACH 4000 Architecture

Generic Logic Block (GLB)



Macrocell

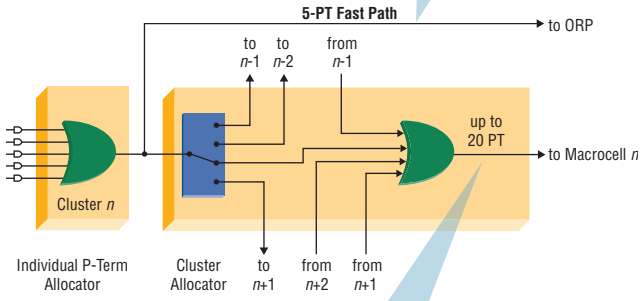


Flexible and efficient clock and control scheme ensures easy implementation with a variety of HDL coding styles.

Flexible Product Term Allocation

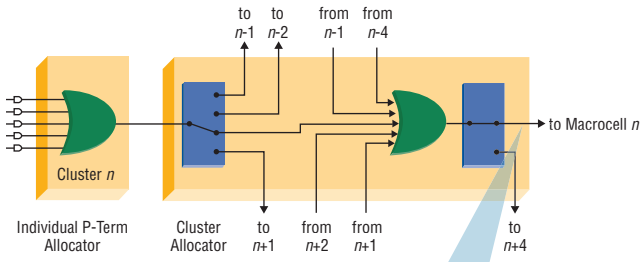
Fast Path and Speed Locked Path

SuperFAST **5 Product Term Fast Path** for high performance functions



SpeedLocked™ Path - up to 20 Product Terms

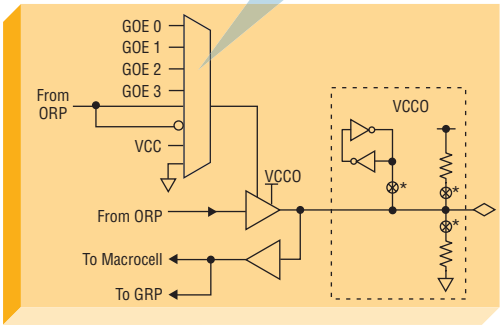
Wide Path



Wide Product Term Path - up to 80 Product Terms

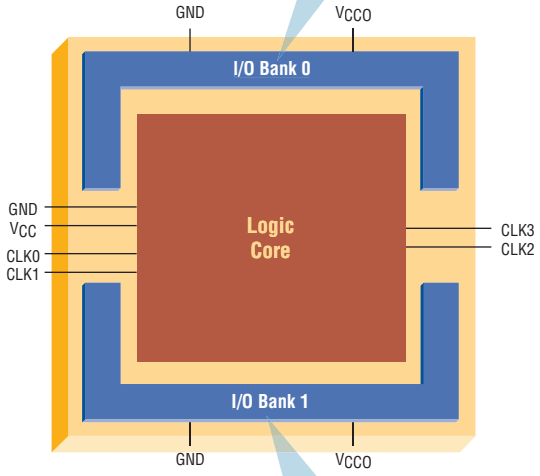
I/O Cell

Enhanced Output Enable control selections for each I/O pin



1.8V/2.5V/3.3V Mixed Voltage Support

I/O Bank power supply can be 1.8V, 2.5V or 3.3V. Input standard supported is independent of V_{CCO}.



Each I/O Bank has its own V_{CCO} and GND

ispMACH 4000 Applications

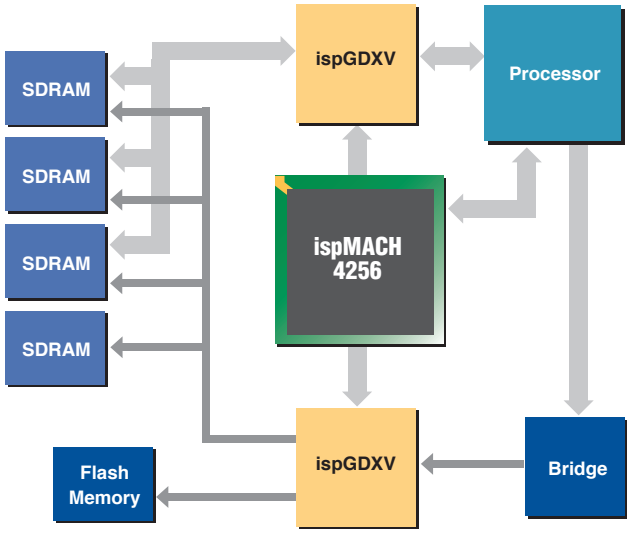
Network Core Router

The SuperFAST performance of the ispMACH 4000 is perfect for implementing high speed data path and control applications. In this application, the ispMACH 4256 implements:

- MPC765 to SDRAM Data Pathway and Controller
- Finite State Machine
- JTAG Control
- MUX/DEMUX

ispMACH 4000 Strengths

- High Density of I/Os
- Cost Effective
- Boundary Scan Improves Testability
- Design Simplicity



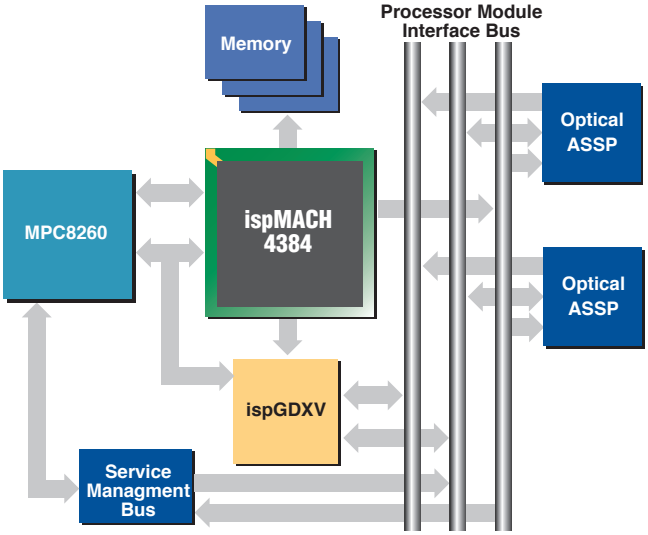
Optical Transmission Processor Module

The ispMACH 4000 is an excellent solution for multi-voltage systems and high-speed bus applications. In this optical transmission application, the ispMACH 4384 performs:

- Complex Data Path Control
- Dedicated Interrupts
- Watchdog Timer
- LED/Alarm Controls
- Bus Arbitration Signals and Chip Selects for ASICs

ispMACH 4000 Strengths

- Bus Speed
- Hot Socketing Capability
- Multi-Voltage Support
- Output Enable Control for Each Pin



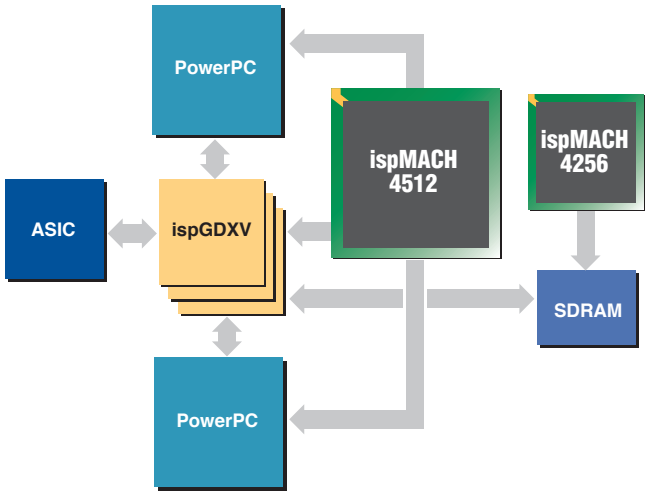
OC12 Edge Router

The in-system programmability, non-volatility and very high speed of ispMACH 4000 devices make them a superior choice for interface applications. In this OC12 edge router application, the ispMACH 4512 performs the following functions:

- PowerPC™, ASIC and SDRAM Interface
- ispGDXV™ Data Flow Control
- CPU Control Registers
- SDRAM Controller
- Multiple Interface Options: DS3, OC-3, OC-12, Ethernet and Gigabit Ethernet

ispMACH 4000 Strengths

- High Speed
- Package Migration
- In-System Programmable for Different Interface Options



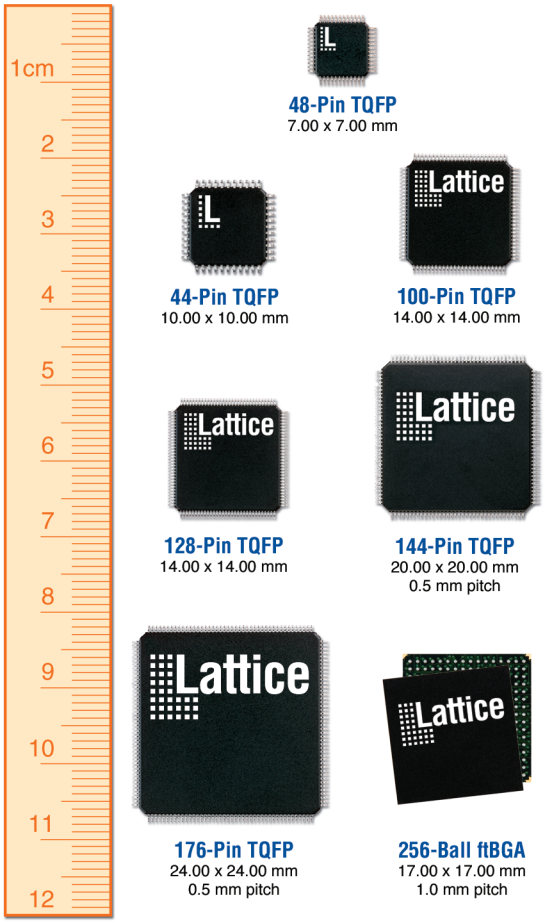
ispMACH 4000V/B/C Family Attributes

V = 3.3V, B = 2.5V, C = 1.8V core supply

Family Member	Macrocells	User I/O + Inputs	t_{PD} (ns)	t_{CO} (ns)	t_S (ns)	f_{MAX} (MHz)	V_{CC} (Volts)	Standby Current at 1.8V (mA)	Package
ispMACH 4032V/B/C	32	30+2 32+4	2.5	2.2	1.8	400	3.3/2.5/1.8	1.3	44-pin TQFP 48-pin TQFP
ispMACH 4064V/B/C	64	30+2 32+4 64+10	2.5	2.2	1.8	400	3.3/2.5/1.8	1.5	44-pin TQFP 48-pin TQFP 100-pin TQFP
ispMACH 4128V/B/C	128	64+10 92+4 96+4	2.7	2.7	1.8	333	3.3/2.5/1.8	1.5	100-pin TQFP 128-pin TQFP 144-pin TQFP**
ispMACH 4256V/B/C	256	64+10 96+4 128+4 128+4/160+4	3.0	2.7	2.0	322	3.3/2.5/1.8	2.0	100-pin TQFP 144-pin TQFP** 176-pin TQFP 256-ball ftBGA*
ispMACH 4384V/B/C	384	128+4 192+4	3.5	2.7	2.0	322	3.3/2.5/1.8	2.5	176-pin TQFP 256-ball ftBGA
ispMACH 4512V/B/C	512	128+4 208+4	3.5	2.7	2.0	322	3.3/2.5/1.8	3.0	176-pin TQFP 256-ball ftBGA

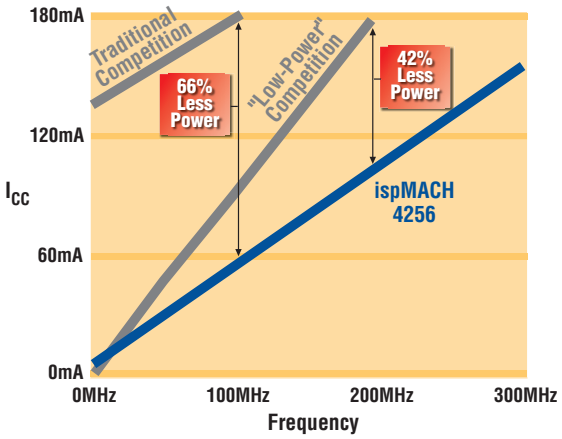
*128 and 160 I/O options **3.3V only

ispMACH 4000 Advanced Packaging

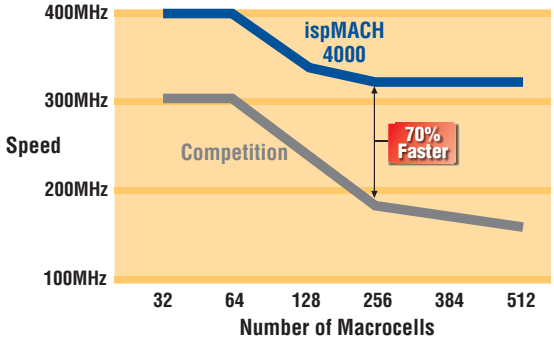


Packages are shown actual size. Dimensions refer to package body size.

Industry's Lowest Power Consumption



Superior Performance



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