Evaluation Board for the AD8333 I/Q Demodulator

AD8333-EVALZ

FEATURES

Factory tested and ready to use
SMA input and output connectors (7)
Configurable jumpers for user options
Phase select
Provision for external reset
Includes LNA input amplifier
Internal clock buffer
Summing amplifier to view sum of both channels or single Channel I and Channel Q outputs
Compact surface-mount layout can be applied to user application

APPLICATIONS

Hands-on testing of the AD8333

GENERAL DESCRIPTION

The AD8333-EVAL evaluation board enables the user to quickly become familiar with the operating characteristics and features of the AD8333 dual I/Q demodulator and phase shifter. Jumpers provide a convenient means for exercising the user-selectable features of the AD8333.

The board is tested prior to shipment and shipped with the phase-encoding bits set to 0000 (no phase shift) for both channels. The LNA is set up for a 50 Ω source, and the VGA sections of the AD8332 are disabled. Test points are provided along the signal path to facilitate signal tracing.

EVALUATION BOARD

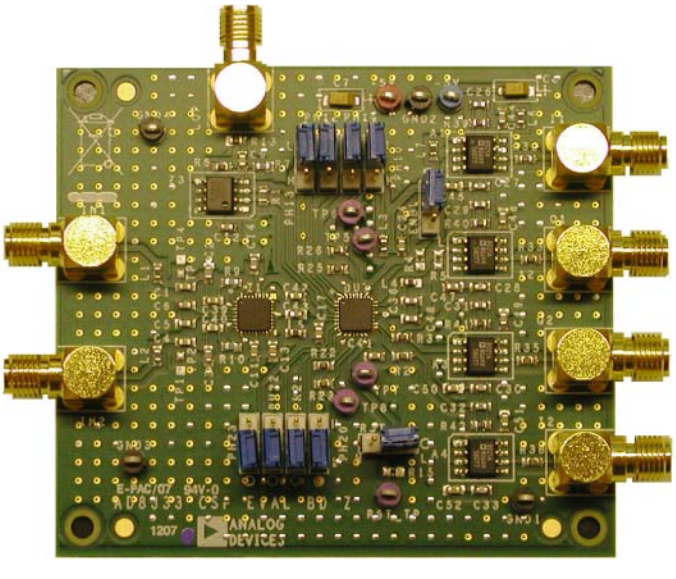

Figure 1. Evaluation Board—Actual Size

Rev. B

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1/06—Revision 0: Initial Version

INTRODUCTION

The AD8333-EVAL evaluation board provides a platform for test and evaluation of the AD8333 I/Q demodulator and phase shifter. The board is shipped fully assembled and tested, and the user need only connect appropriate signals to the RF input and f_{4LO} SMA connectors. An AD8332 is included with the board and acts as a buffer and bias supply for the AD8333, converting single-ended signals to differential, centered at half the supply. A photograph of the board is shown in Figure 1 and a schematic diagram is shown in Figure 3. The board requires dual 5 V supplies capable of supplying 300 mA or greater. Except for the components shown in grayscale, the board is built and tested using all the components illustrated in Figure 3.

FEATURES AND OPTIONS

The evaluation board has several features and options that are configurable according to the specific needs of the user. Table 1 lists the jumpers and their functions.

Table 1. Jumper Functions

Jumper	Function	Position
ENBL	Enable the AD8333	Bottom = disable; top = enable
PH10	Ch 1 Phase 0 bit	Top = 0; bottom = 1
PH11	Ch 1 Phase 1 bit	Top = 0; bottom = 1
PH12	Ch 1 Phase 2 bit	Top = 0; bottom = 1
PH13	Ch 1 Phase 3 bit	Top = 0; bottom = 1
PH20	Ch 2 Phase 0 bit	Top = 1; bottom = 0
PH21	Ch 2 Phase 1 bit	Top = 1; bottom = 0
PH22	Ch 2 Phase 2 bit	Top = 1; bottom = 0
PH23	Ch 2 Phase 3 bit	Top = 1; bottom = 0
RST	Reset pin	Left = reset; right = normal

The Phase Bits

The phase bits configure the channel for one of sixteen 22.5° increments from 0° to 337.5°. The increments increase according to a simple binary code from 0000 to 1111 embodied in the phase bits from 0° (0x0) to 337.5° (0xF). Table 2 lists the phase shift and corresponding code for each bit. The bits labeled 0 and 1 correspond to low and high, respectively, on the silkscreen. Jumpers are provided to select the desired state.

Enable and Reset Jumpers

For normal operation, place a jumper in the upper position of ENBL. To disable the AD8333, move the jumper to the lower position. For normal operation, the jumper for RST is in its right position. When the jumper is in the left position, the device counter is held in reset and no mixing occurs.

Table 2. Phase Shift Select Codes

Φ Shift	PHx3	PHx2	PHx1	PHx0
0°	0	0	0	0
22.5°	0	0	0	1
45°	0	0	1	0
67.5°	0	0	1	1
90°	0	1	0	0
112.5°	0	1	0	1
135°	0	1	1	0
157.5°	0	1	1	1
180°	1	0	0	0
202.5°	1	0	0	1
225°	1	0	1	0
247.5°	1	0	1	1
270°	1	1	0	0
292.5°	1	1	0	1
315°	1	1	1	0
337.5°	1	1	1	1

Fixed Options

Several options can be realized by adding or changing resistors.

LNA Input Impedance

The shipping configuration of the input impedance of the LNA is 50 Ω to match the output impedance of most signal generators. Input impedances of up to 14.7 kΩ are obtained by selection of the values of R9 and R10. Details concerning this circuit feature are found in the AD8332 data sheet. For reference, Table 3 lists common values of input impedance and corresponding feedback resistor values.

Table 3. LNA External Component Values for Common Source Impedances

R_{IN} (Ω)	R_{FB}, Nearest STD 1% Value (Ω)	C_{SH} (pF)
50	280	22
75	412	12
100	562	8
200	1.13 k	1.2
500	3.01 k	None
6 k	∞	None

Current Summing

The output transimpedance amplifiers, A1 through A4, are configured as I-to-V converters to convert the output current of the AD8333 to a voltage. The low-pass filters formed by the feedback components are designed for single-channel operation with ±5 V supplies.

Optional R4 and R5 resistors are provided to sum the two channels. When R4 and R5 are installed, R2 and R3 are removed and the sum of the outputs is seen at the I1 and Q1 output SMA connectors. If large signal levels are expected, the feedback resistor and capacitor values, 787 Ω and 2.2 nF, can be halved and doubled, respectively, to optimize the output swing. The filter capacitor values can be changed if other frequencies are desired.

Reset Input

For normal operation, the reset input is high (no reset). To drive the reset with a dynamic signal, provision is made to connect a signal generator at the RST input. A 49.9 Ω, 0603 surface-mount resistor can be installed at R15 to terminate the reset input for pulsed experiments. In this configuration, the jumper at RST is not used and must be removed to avoid loading the power supply.

MEASUREMENT SETUP

Figure 2 displays the connector and user-selectable jumper locations. A typical board and test equipment setup is shown in Figure 4. Two signal generators, a power splitter, and a ±5 V, 300 mA (minimum) power supply are required. Synchronize the signal generators for optimum results. Remember that the f_{4LO} signal generator frequency is four times that of the nominal frequency of the RF source. For example, to detect signals with a nominal center frequency of 5 MHz, an f_{4LO} frequency of 20 MHz is applied to the oscillator input. For an applied RF signal of 5.01 MHz, the mix frequencies are 10 kHz and 10.01 MHz. Because of the low-pass active filter of the transconductance amplifiers (A1 through A4), 10 kHz is observed at the output.

Take care to avoid over driving the LNA input of the AD8332. The LNA gain is 19 dB (9.5×) and the maximum output swing must not be exceeded; −10 dBm suffices for many experiments. The f_{4LO} input is ac-coupled to a 5 V LVDS buffer to provide an ideal interface to the AD8333.

The f_{4LO} level is frequency dependent; consult the AD8333 data sheet for minimum signal levels, then adjust the signal generator output level accordingly.

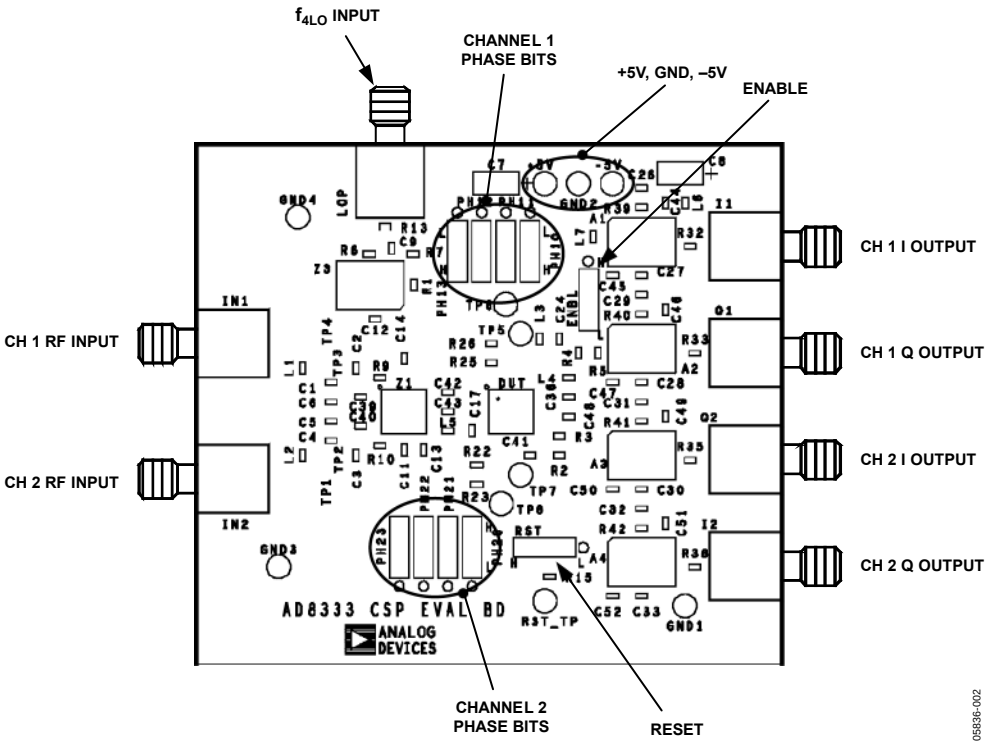

Figure 2. Evaluation Board Layout

EVALUATION BOARD SCHEMATIC AND ARTWORK

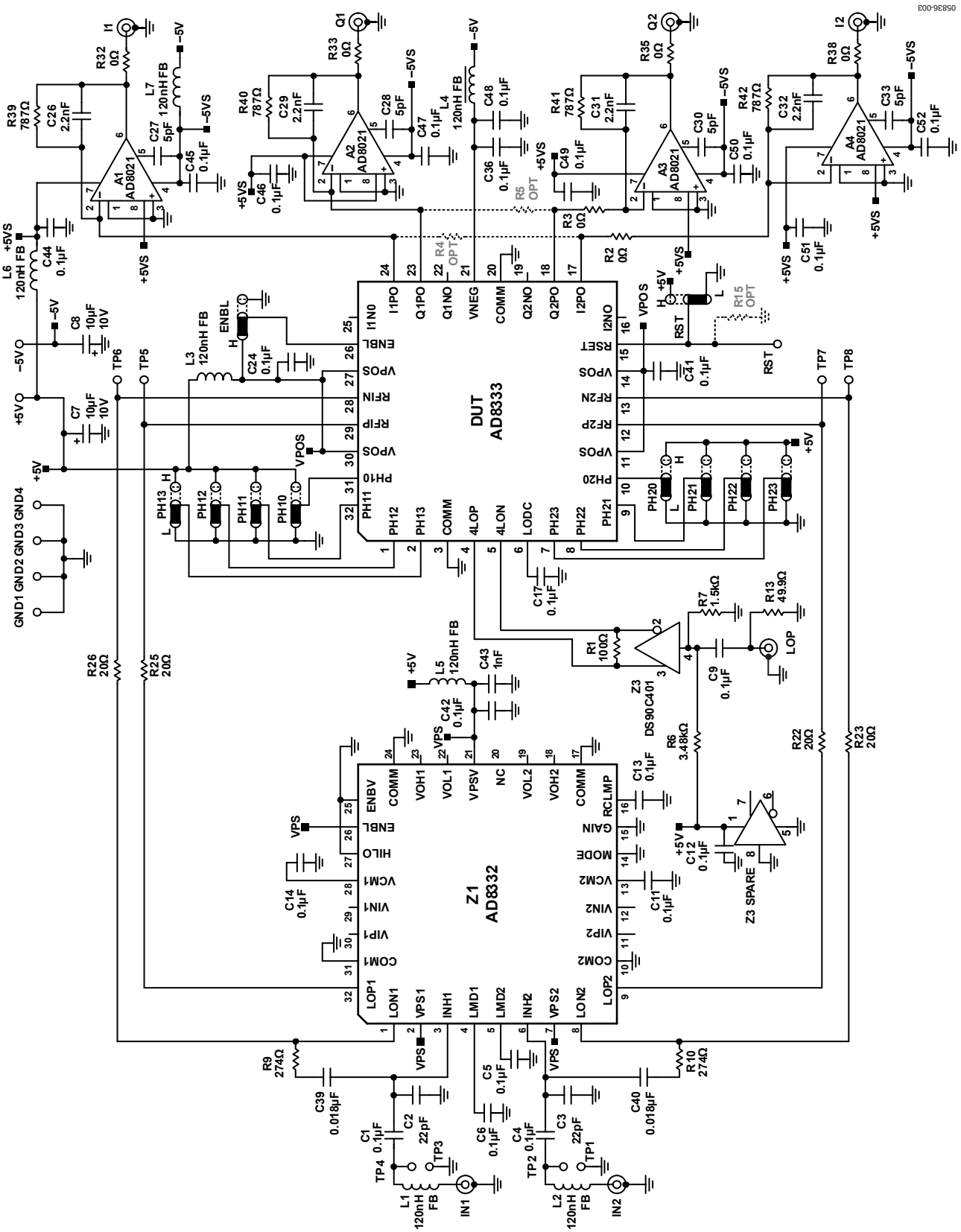

Figure 3. Evaluation Board Schematic

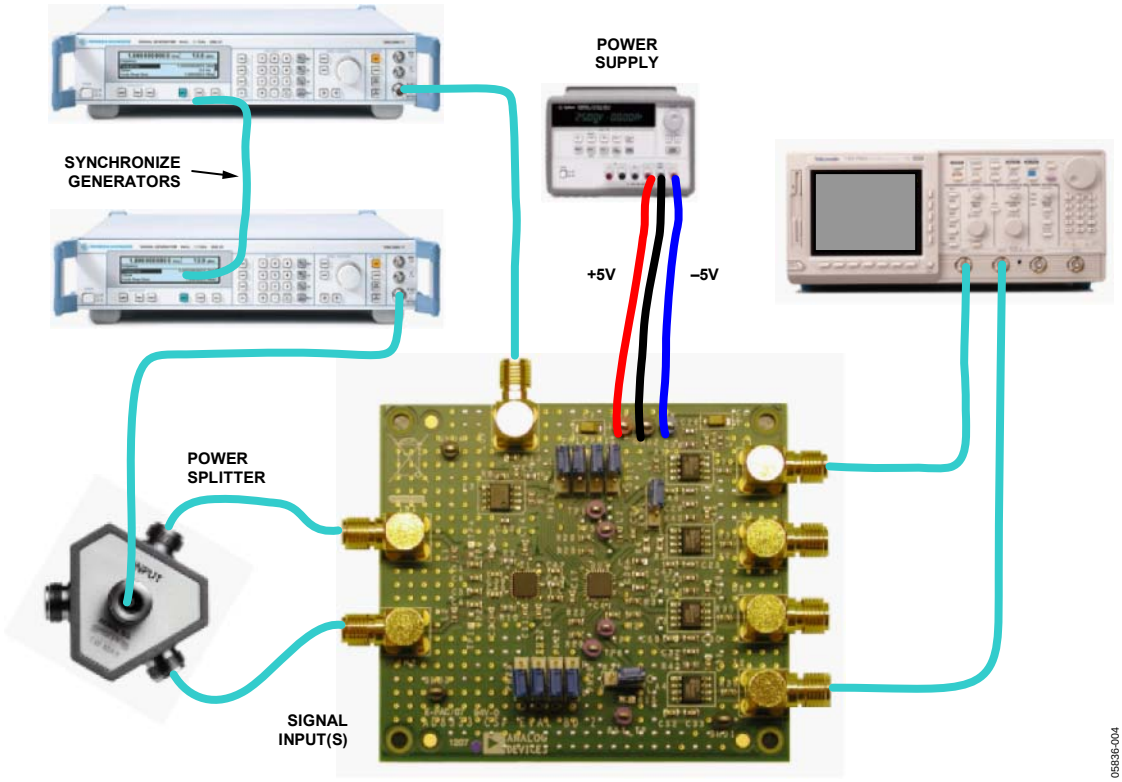

Figure 4. Typical Board Test Connections (One Channel Shown)

BOARD LAYOUT

The AD8333 evaluation board has four layers. The interconnecting circuitry is located on the outer layers with the inner layers dedicated as power and ground planes. Figure 5 through Figure 9 illustrate the copper patterns.

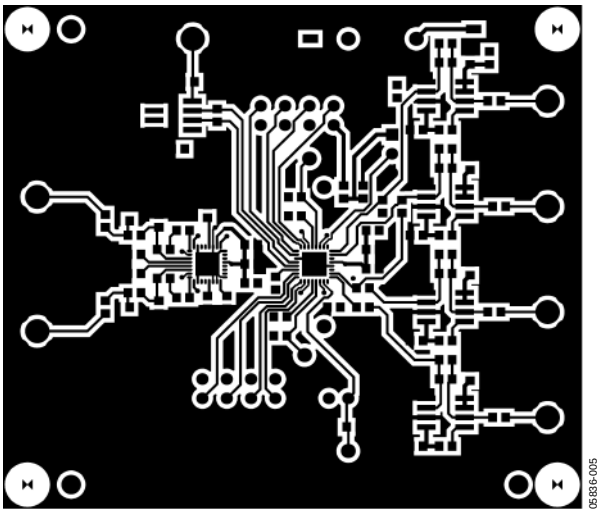

Figure 5. Component Side Copper

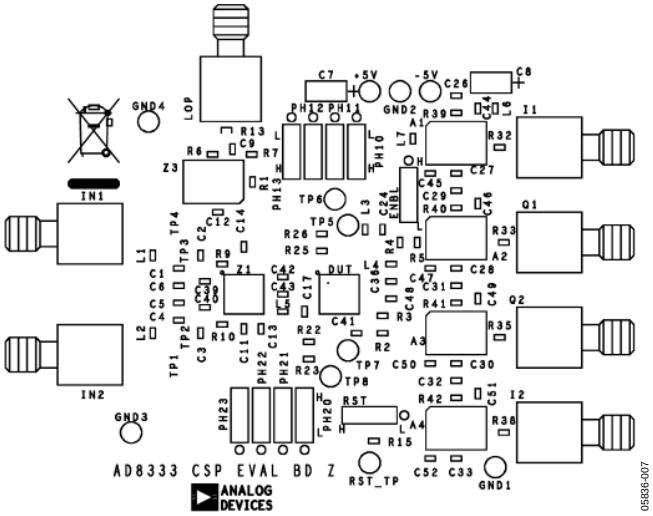

Figure 7. Component Side Silkscreen

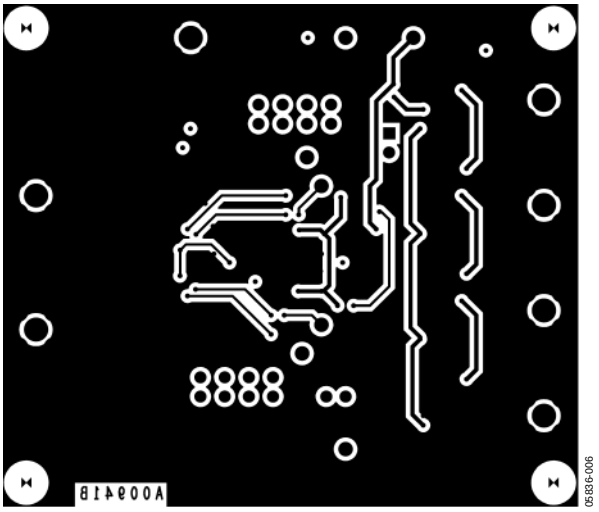

Figure 6. Wiring Side Copper

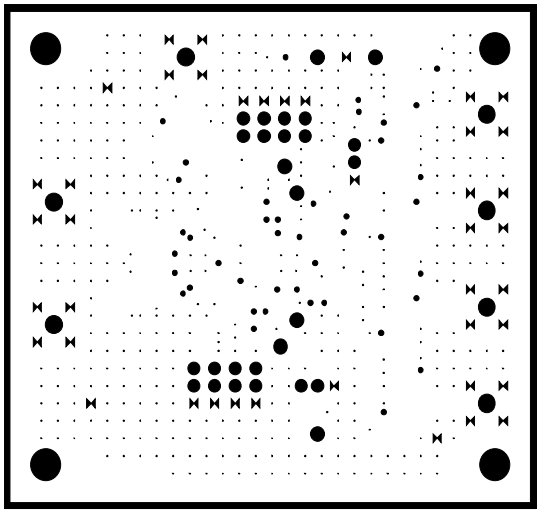

Figure 8. Ground Plane

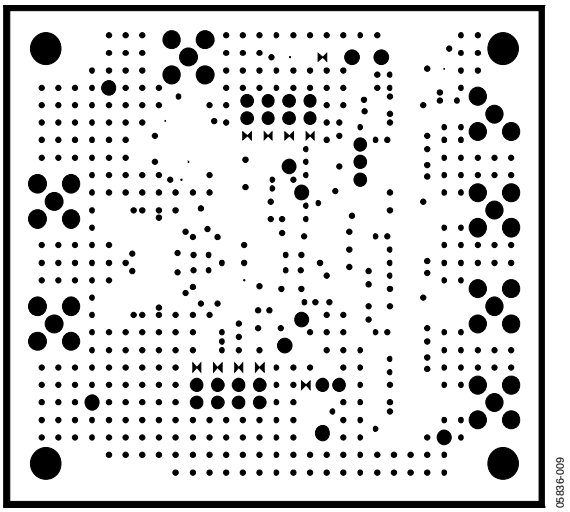

Figure 9. Power Plane

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty	Name	Description	Reference Designator	Mfg. Part Number	Manufacturer
4	IC	AD8021ARZ	A1 to A4	AD8021ARZ	Analog Devices, Inc.
23	Capacitor	0.1 µF, 16 V, 0603, X7R	C1, C4, C5, C6, C9, C11, C12, C13, C14, C17, C24, C36, C41, C42, C44, C45, C46, C47, C48, C49, C50, C51, C52	C0603C104K4RACTU	KEMET Corporation
2	Capacitor	22 pF, 50 V, 5%, 0603	C2, C3	ECJ-1VC1H220J	Panasonic
2	Capacitor	10 µF, 10 V, A size tantalum	C7, C8	T491A106M010AS	KEMET Corporation
4	Capacitor	2.2 nF, 50 V, X7R, 10%, 0603	C26, C29, C31, C32	ECJ-1VB1H222K	Panasonic
4	Capacitor	5 pF, 50 V, 0603	C27, C28, C30, C33	ECJ-1VC1H050C	Panasonic
2	Capacitor	0.018 µF, 10%, 50 V, X7R, 0603	C39, C40	06035C183KAT2A	AVX Corp.
1	Capacitor	1 nF, 100 V, 10%, 0603, X7R	C43	ECJ-1VB2A102K	Panasonic
1	IC	AD8333 I/Q demodulator	DUT	AD8333ACPZ-WP	Analog Devices, Inc.
7	Connector	SMA female PC mount, RA	I1, I2, IN1, IN2, LOP, Q1, Q2	901-143-6RFX	Amphenol
7	Ferrite Bead	120 nH, 0603	L1, L2, L3, L4, L5, L6, L7	BLM18BA750SN1D	Murata Manufacturing Co.
1	Resistor	100 Ω, 1%, 1/16 W, 0603	R1	ERJ-3EKF1000V	Panasonic
6	Resistor	0 Ω, 5%, 1/10 W, 0603	R2, R3, R32, R33, R35, R38	ERJ-2GE0R00X	Panasonic
1	Resistor	3.48 kΩ, 1%, 1/10 W, 0603	R6	ERJ-3EKF3.48KV	Panasonic
1	Resistor	1.5 kΩ, 1%, 1/10 W, 0603	R7	ERJ3EKF1501V	Panasonic
2	Resistor	274 Ω, 1/16 W, 1%, 0603	R9, R10	ERJ-3EKF2740V	Panasonic
1	Resistor	49.9 Ω, 1%, 1/16 W, 0603	R13	ERJ-3EKF49R9V	Panasonic
4	Resistor	20 Ω, 1%, 1/10 W, 0603	R22, R23, R25, R26	ERJ3EKF20R0V	Panasonic
4	Resistor	787 Ω, 1/16 W, 1%, 0603	R39 to R42	ERJ-3EKF7870V	Panasonic
10	Header	3-pin 0.025" sq., 0.1" spacing	ENBL, PH10, PH11, PH12, PH13, PH20, PH21, PH22, PH23, RST	22-11-2032	Molex, Inc.
1	Test Loop	0.125″ diameter, red	+5 V	TP-104-01-02	Components Corp.
4	Test Loop	0.125″ diameter, black	GND1 to GND4	TP-104-01-00	Components Corp.
1	Test Loop	0.125″ diameter, blue	−5 V	TP-104-01-06P	Components Corp.
5	Test Loop	0.125″ diameter, purple	TP5 to TP8, RST	TP-104-01-07	Components Corp.
1	IC	VGA AD8332	Z1	AD8332ACPZ	Analog Devices, Inc.
1	IC	DRV LVDS dual differential signal 8-lead SOIC	Z3	DS90C401M	National Semiconductor
1	PC Board			09-A00941C	
4	Bumper		Mount to wiring side of board	SJ-67A11 (black)	3M
10	Jumper		Install at ENBL: top, PH10: top, PH11: top, PH12: top, PH13: top, PH20: bottom, PH21: bottom, PH22: bottom, PH23: bottom, RST: right; orient when board is in normal viewing position with IN1 and IN2 SMA connectors at left	65474-001	FCI

ORDERING GUIDE

Model	Description
AD8333-EVALZ[1]	Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

NOTES

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