N- and P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
N-Channel	40	0.0355 at V_{GS} = 10 V	6.8	5.3
		0.0425 at V_{GS} = 4.5 V	6.2	
P-Channel	- 40	0.035 at V_{GS} = - 10 V	- 7.2	17
		0.047 at V_{GS} = - 4.5 V	- 6.2	

FEATURES

- **Halogen-free According to IEC 61249-2-21 Available**
- TrenchFET® Power MOSFET

Pb-free

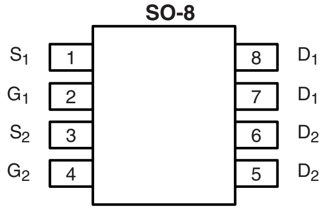
RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

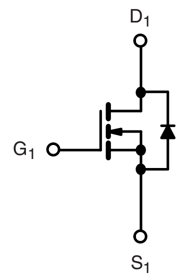
- Backlight Inverter for LCD Display

SO-8

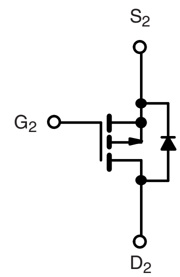


Top View

Ordering Information: Si4561DY-T1-E3 (Lead (Pb)-free)
Si4561DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	40	- 40	V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	6.8	- 7.2	A
	T_C = 70 °C		5.4	- 5.7	
	T_A = 25 °C		5.6[b, c]	- 5.6[b, c]	
	T_A = 70 °C		4.4[b, c]	- 4.4[b, c]	
Pulsed Drain Current		I_{DM}	20	- 20	
Source-Drain Current Diode Current	T_C = 25 °C	I_S	2.5	- 2.5	
	T_A = 25 °C		1.6[b, c]	- 1.6[b, c]	
Pulsed Source-Drain Current		I_{SM}	20	- 20	
Single Pulse Avalanche Current	L = 0 1 mH	I_{AS}	7	15	
Single Pulse Avalanche Energy		E_{AS}	2.45	11.25	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	3.0	3.3	W
	T_C = 70 °C		1.9	2.10	
	T_A = 25 °C		2.0[b, c]	2.0[b, c]	
	T_A = 70 °C		1.25[b, c]	1.25[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	54	64	50	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	33	42	31	37	

Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under Steady State conditions is 120 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

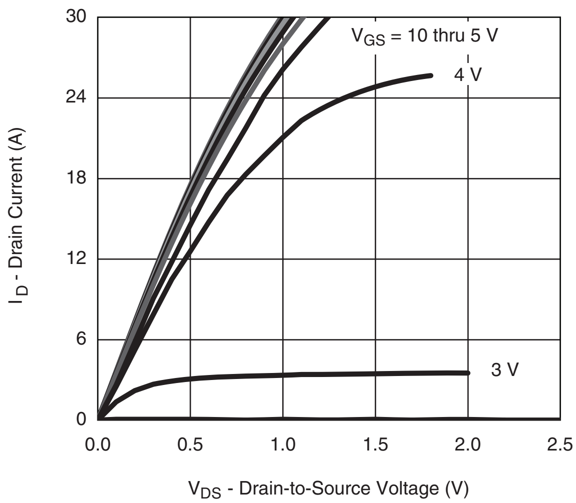
Parameter	Symbol	Test Conditions		Min.	Typ.[a]	Max.	Unit
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	40			V
		V_{GS} = 0 V, I_D = - 250 µA	P-Ch	- 40			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch		44		mV/°C
		I_D = - 250 µA	P-Ch		- 41		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch		- 5.5		
		II_D = - 250 µA	P-Ch		4.3		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	1.4		3.0	V
		$V_{DS} = V_{GS}$, I_D = - 250 µA	P-Ch	- 1.4		- 3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	N-Ch			100	nA
			P-Ch			- 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = - 40 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch			10	
		V_{DS} = - 40 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch			- 10	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	N-Ch	10			A
		V_{DS} = - 5 V, V_{GS} = - 10 V	P-Ch	- 10			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	N-Ch		0.0295	0.0355	Ω
		V_{GS} = - 10 V, I_D = - 5 A	P-Ch		0.0285	0.035	
		V_{GS} = 4.5 V, I_D = 4 A	N-Ch		0.0355	0.0425	
		V_{GS} = - 4.5 V, I_D = - 4 A	P-Ch		0.037	0.047	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 5 A	N-Ch		22		S
		V_{DS} = - 15 V, I_D = - 5 A	P-Ch		20		
Dynamic[a]							
Input Capacitance	C_{iss}	N-Channel V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 20 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		640		pF
			P-Ch		1555		
Output Capacitance	C_{oss}		N-Ch		73		
			P-Ch		176		
Reverse Transfer Capacitance	C_{rss}		N-Ch		41		
			P-Ch		142		
Total Gate Charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 5 A	N-Ch		11.7	20	nC
		V_{DS} = - 20 V, V_{GS} = - 10 V, I_D = - 5 A	P-Ch		38.5	60	
		N-Channel V_{DS} = 20 V, V_{GS} = 4.5 V I_D = 5 A P-Channel V_{DS} = - 20 V, V_{GS} = - 4.5 V, I_D = - 5 A	N-Ch		5.3	9	
			P-Ch		17	27	
Gate-Source Charge	Q_{gs}		N-Ch		1.9		
			P-Ch		4.2		
Gate-Drain Charge	Q_{gd}		N-Ch		1.7		
			P-Ch		7.0		
Gate Resistance	R_g	f = 1 MHz	N-Ch		2.2		Ω
			P-Ch		3		

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**[a]	**Max.**	**Unit**
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 20 V, R_L = 4 Ω I_D ≅ 5 A, V_{GEN} = 10 V, R_g = 1 Ω P-Channel V_{DD} = - 20 V, R_L = 4 Ω I_D ≅ - 5 A, V_{GEN} = - 10 V, R_g = 1 Ω	N-Ch		7	14	ns
			P-Ch		11	20	
Rise Time	t_r		N-Ch		10	20	
			P-Ch		15	30	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		15	30	
			P-Ch		36	60	
Fall Time	t_f		N-Ch		9	18	
			P-Ch		9	18	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 20 V, R_L = 4 Ω I_D ≅ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-Channel V_{DD} = - 20 V, R_L = 4 Ω I_D ≅ - 5 A, V_{GEN} = - 4.5 V, R_g = 16 Ω	N-Ch		16	30	
			P-Ch		49	80	
Rise Time	t_r		N-Ch		17	30	
			P-Ch		79	120	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		16	30	
			P-Ch		35	60	
Fall Time	t_f		N-Ch		10	20	
			P-Ch		14	25	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	N-Ch			2.5	A
			P-Ch			- 2.5	
Pulse Diode Forward Current[a]	I_{SM}		N-Ch			20	
			P-Ch			- 20	
Body Diode Voltage	V_{SD}	I_S = 1.6 A	N-Ch		0.78	1.2	V
		I_S = - 1.6 A	P-Ch		- 0.74	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel I_F = 2 A, dI/dt = 100 A/µs, T_J = 25 °C P-Channel I_F = - 2 A, dI/dt = - 100 A/µs, T_J = 25 °C	N-Ch		19	30	ns
			P-Ch		22	40	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		14	25	nC
			P-Ch		22	35	
Reverse Recovery Fall Time	t_a		N-Ch		13		ns
			P-Ch		15		
Reverse Recovery Rise Time	t_b		N-Ch		6		
			P-Ch		7		

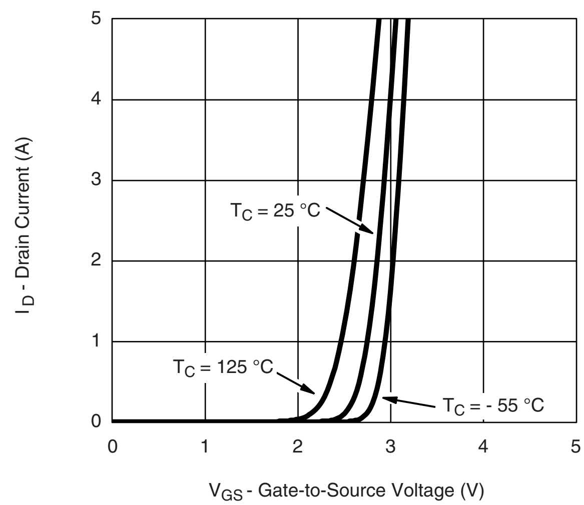
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

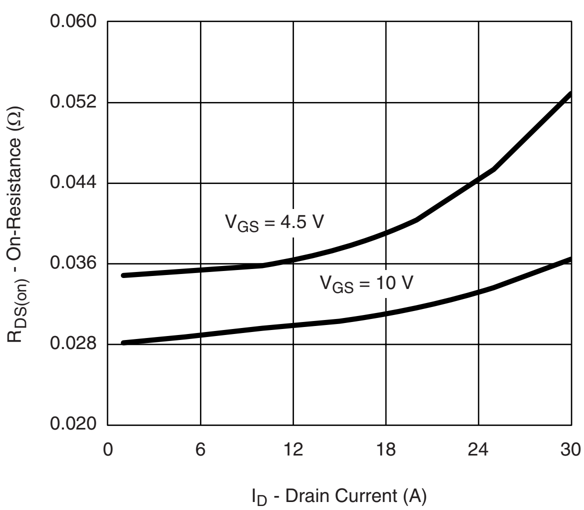
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



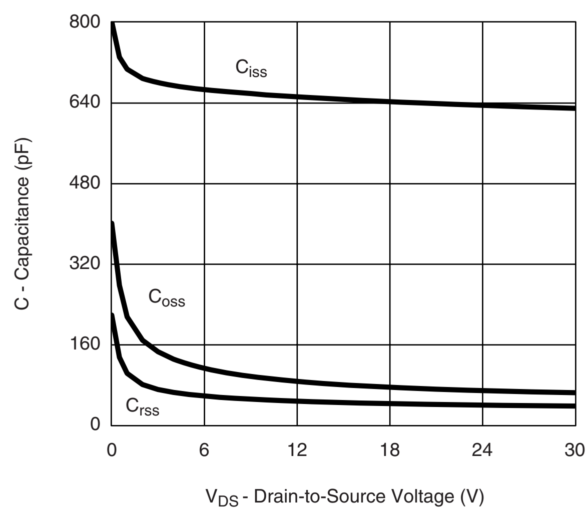
Output Characteristics



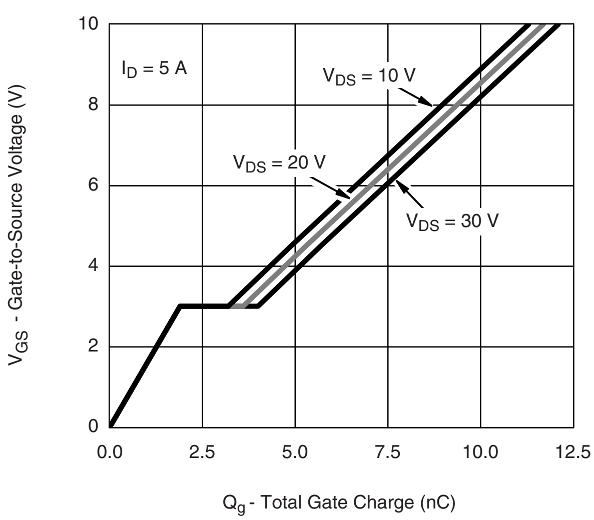
Transfer Characteristics



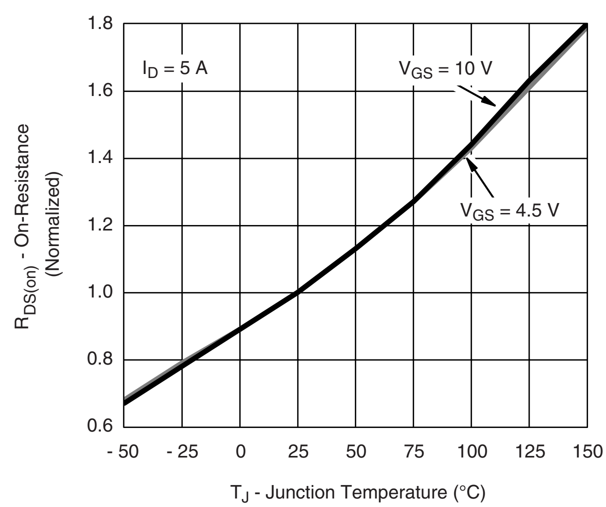
On-Resistance vs. Drain Current



Capacitance

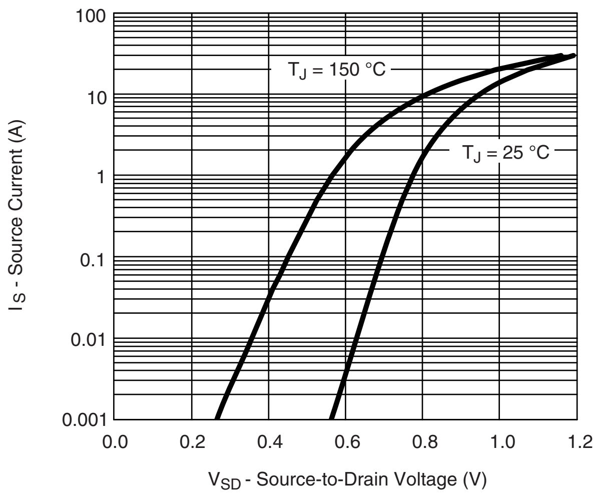


Gate Charge

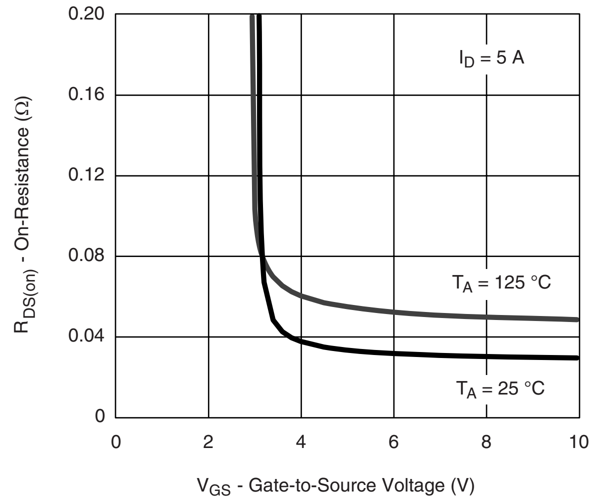


On-Resistance vs. Junction Temperature

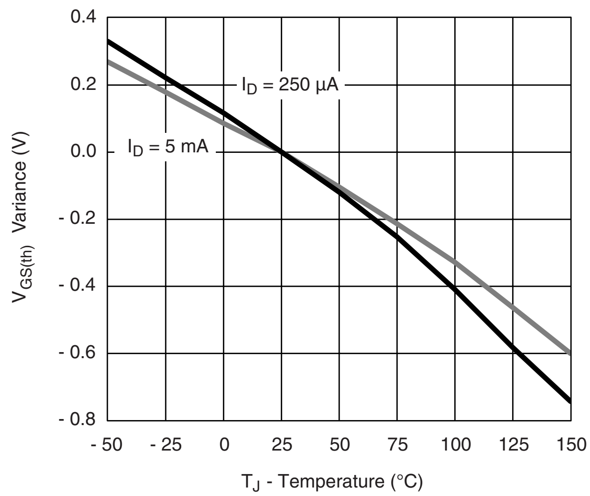
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



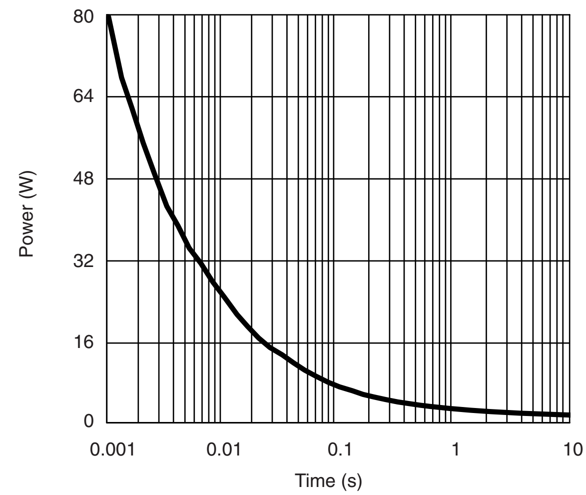
Source-Drain Diode Forward Voltage



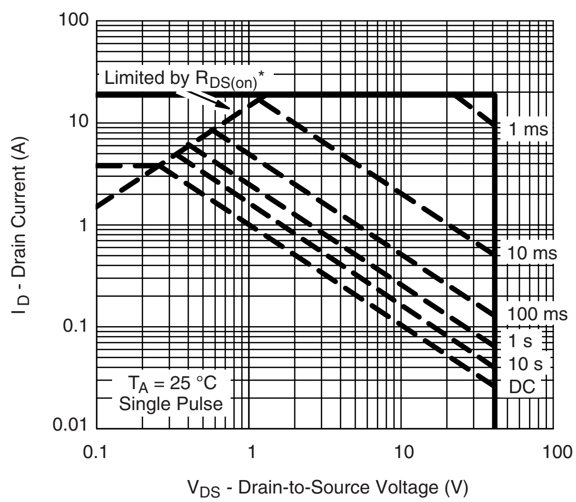
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



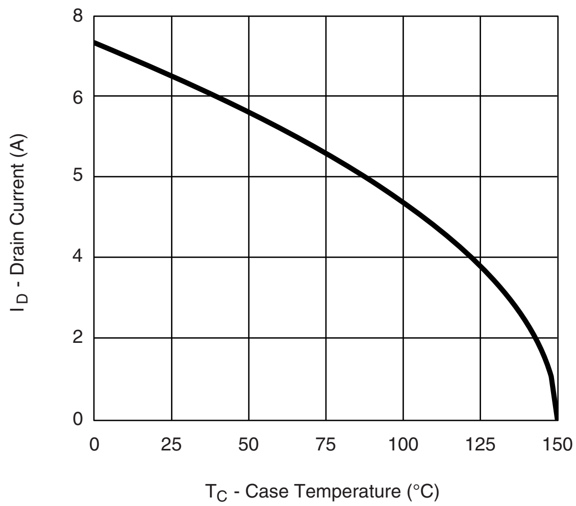
Single Pulse Power, Junction-to-Ambient



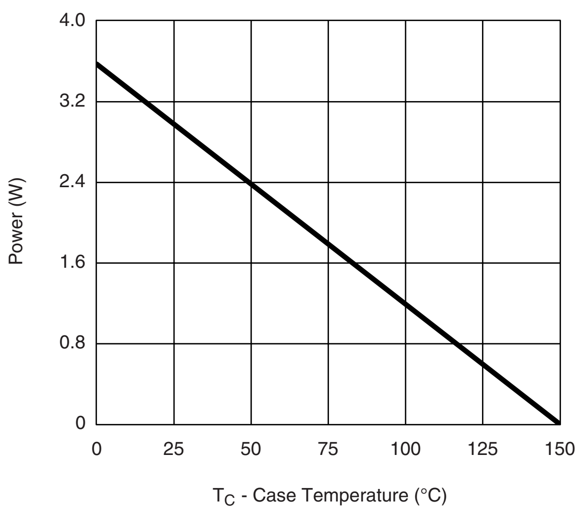
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

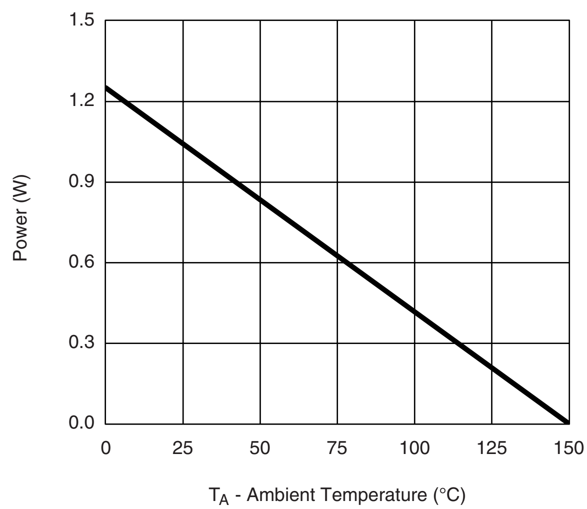
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



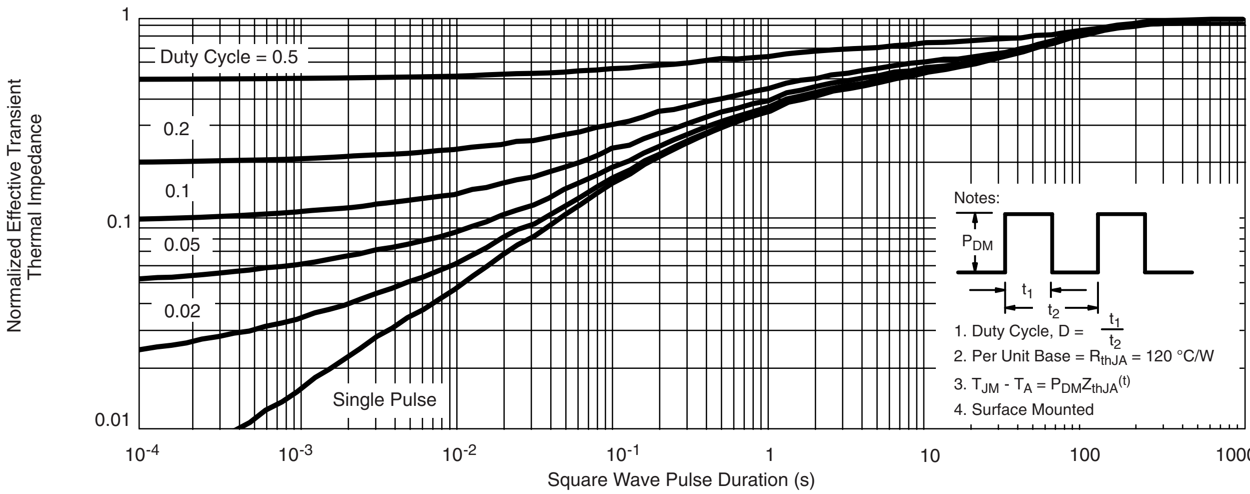
Power Derating, Junction-to-Foot



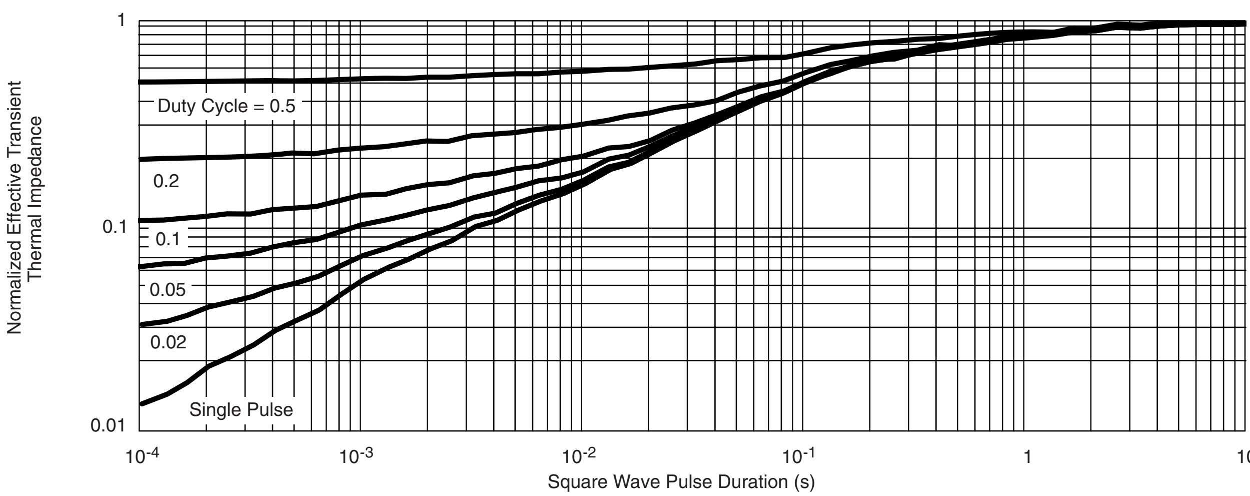
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

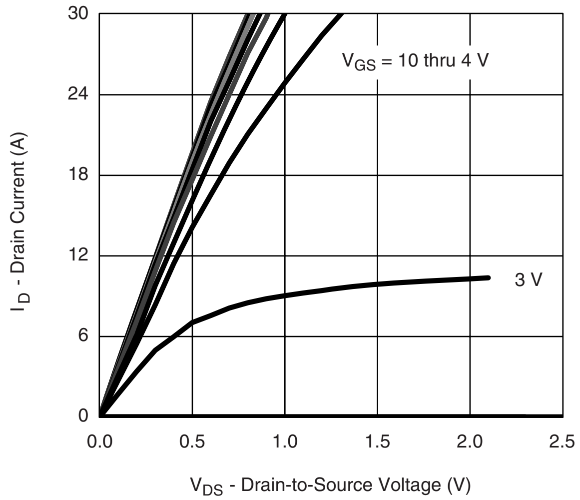


Normalized Thermal Transient Impedance, Junction-to-Ambient

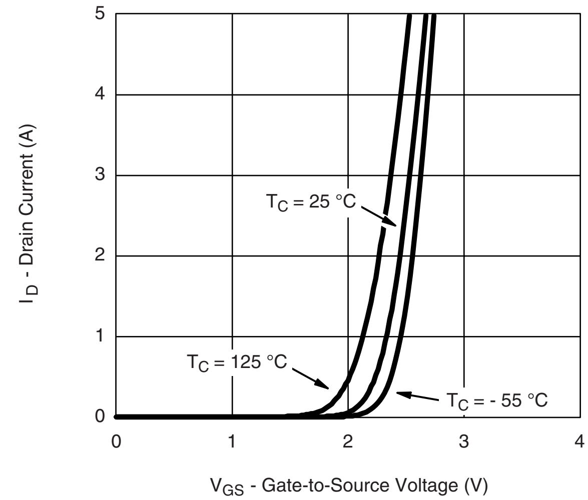


Normalized Thermal Transient Impedance, Junction-to-Foot

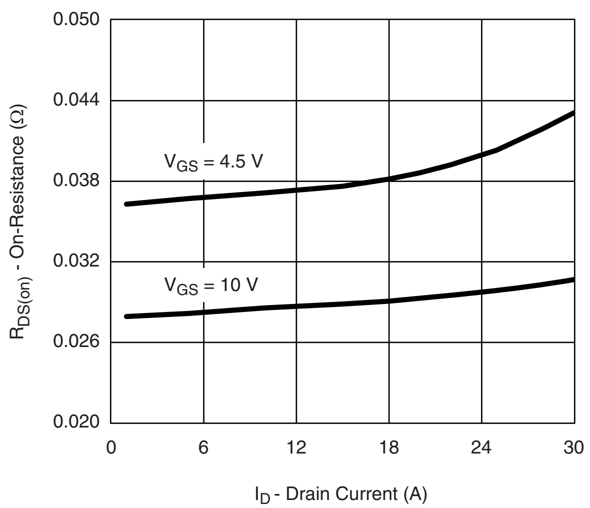
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



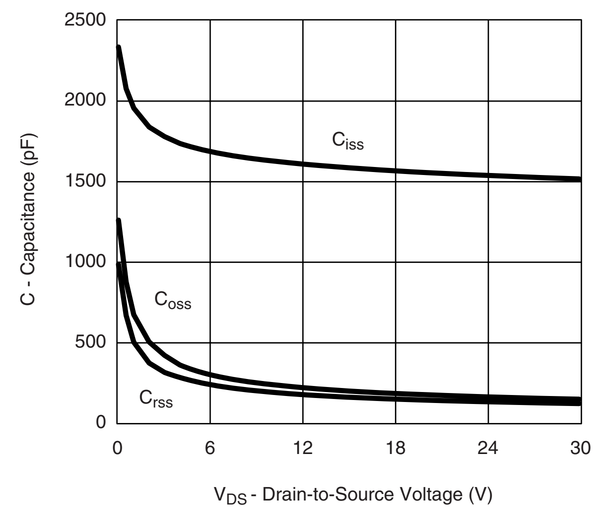
Output Characteristics



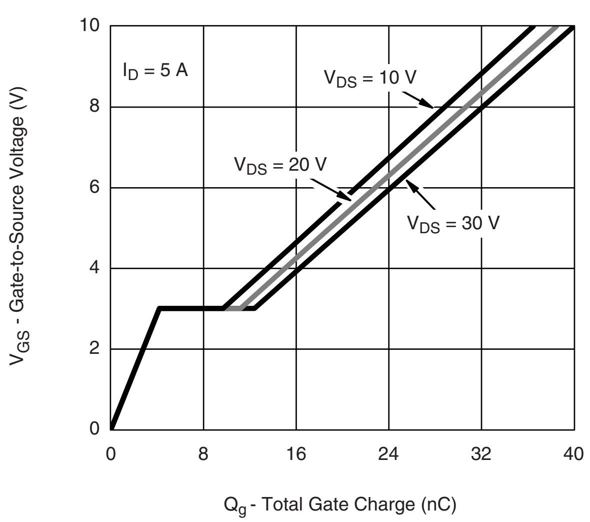
Transfer Characteristics



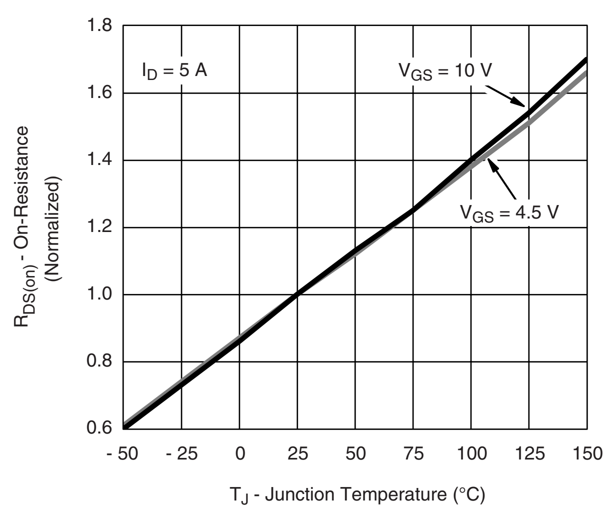
On-Resistance vs. Drain Current



Capacitance

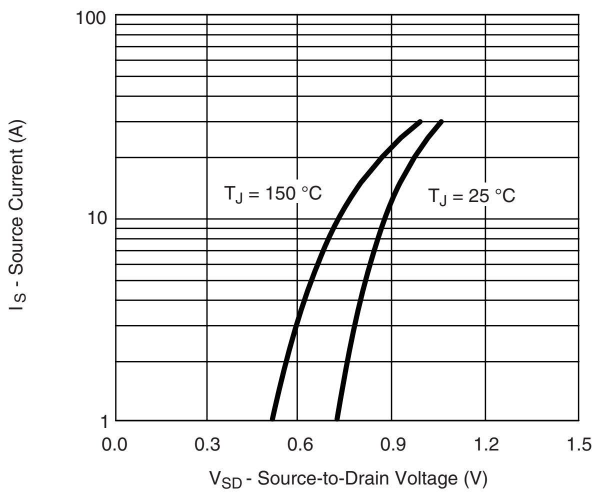


Gate Charge

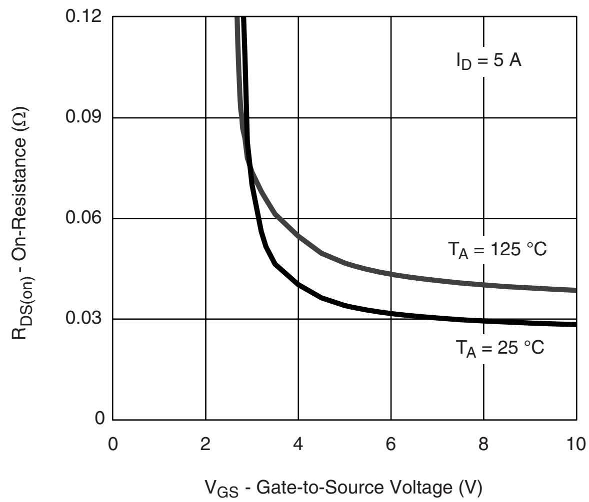


On-Resistance vs. Junction Temperature

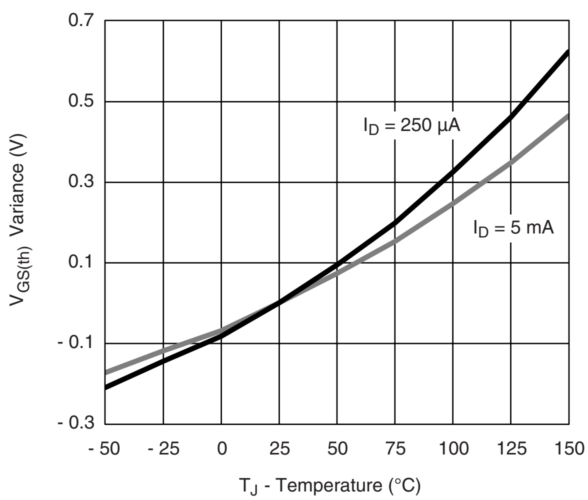
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



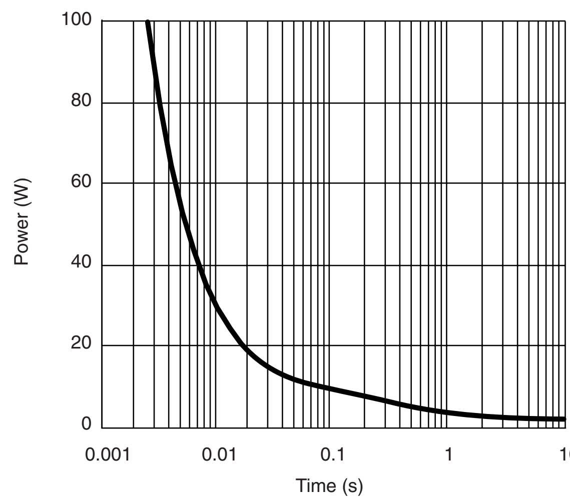
Source-Drain Diode Forward Voltage



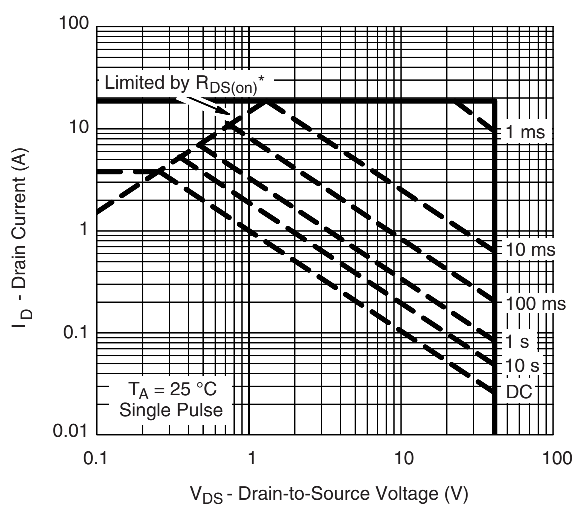
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



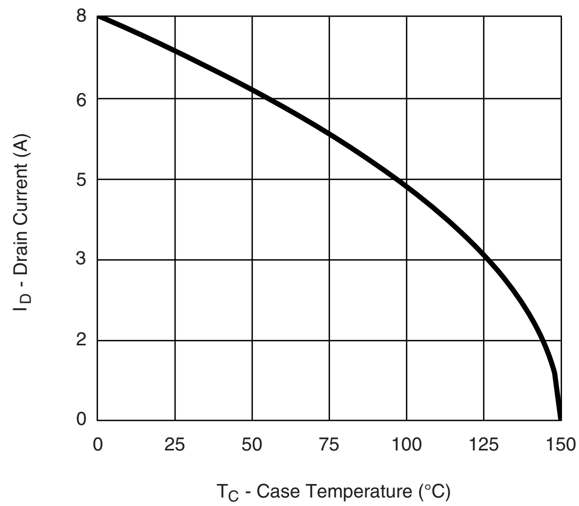
Single Pulse Power, Junction-to-Ambient



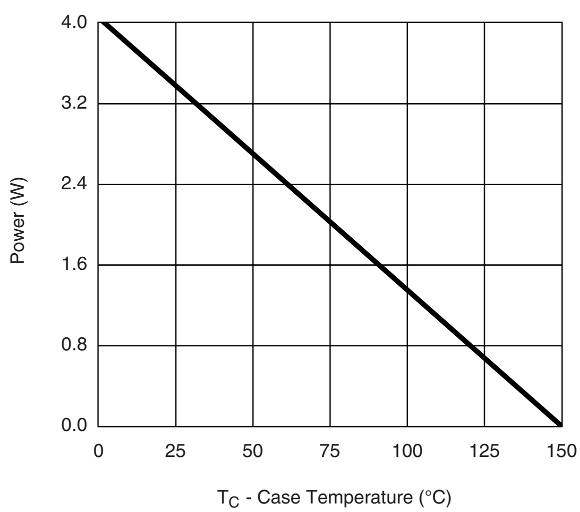
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

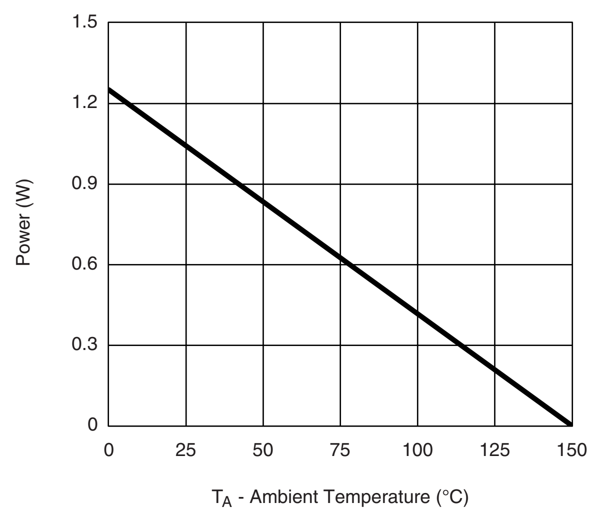
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



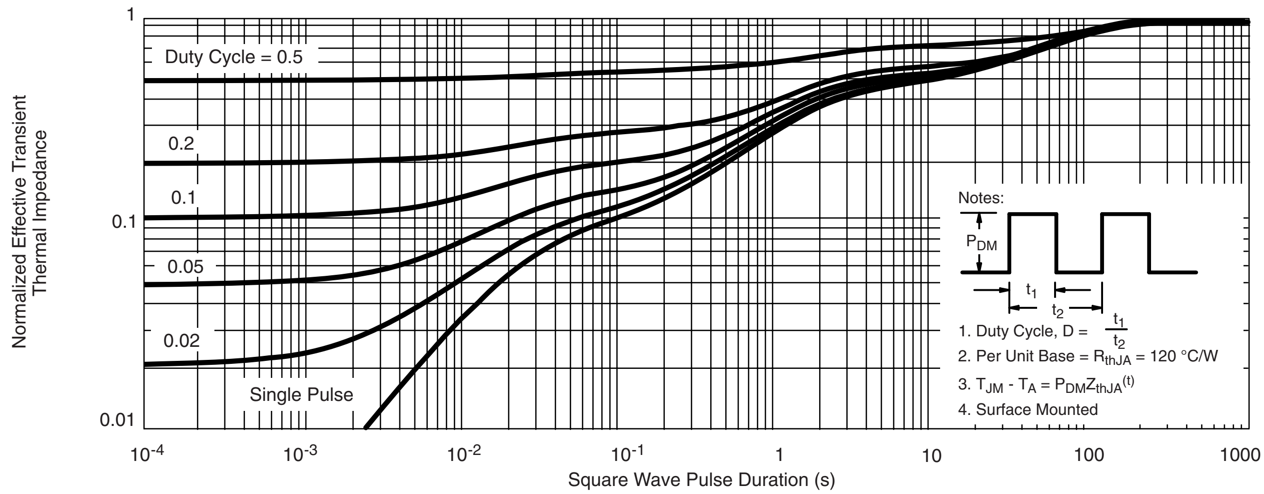
Power Derating, Junction-to-Foot



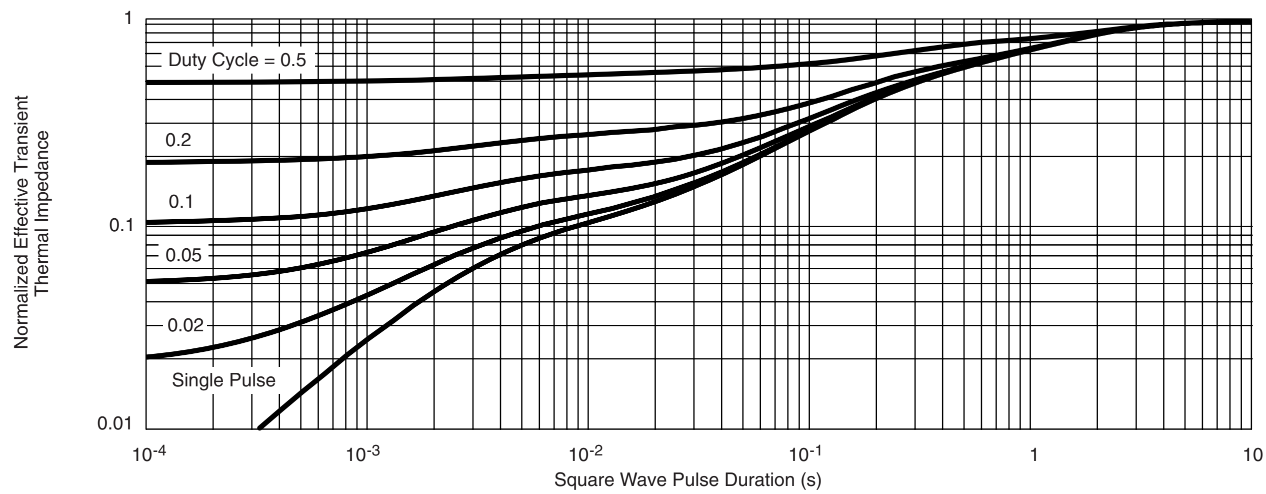
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



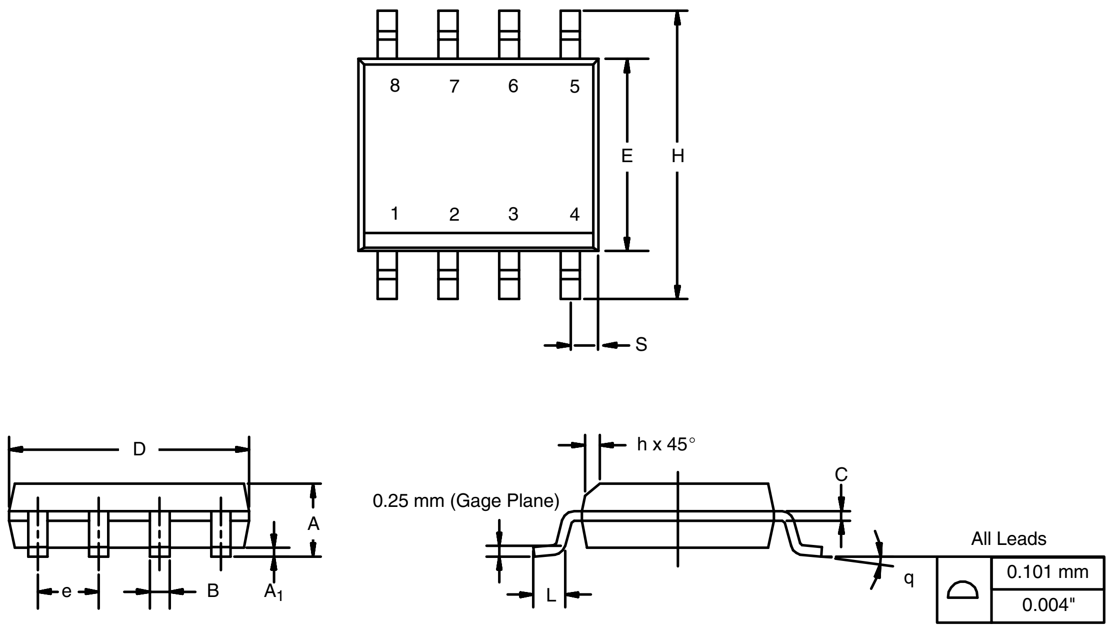
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69730.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

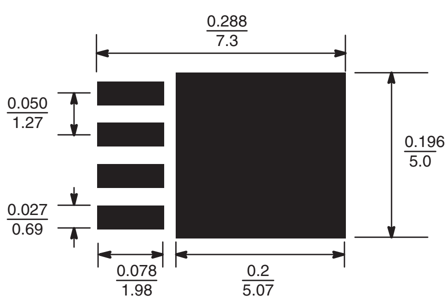


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

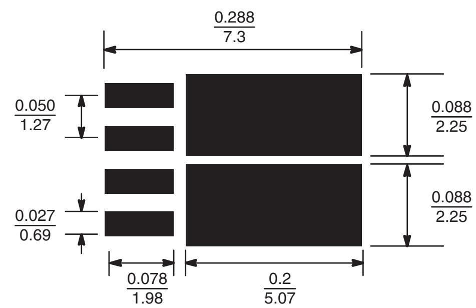


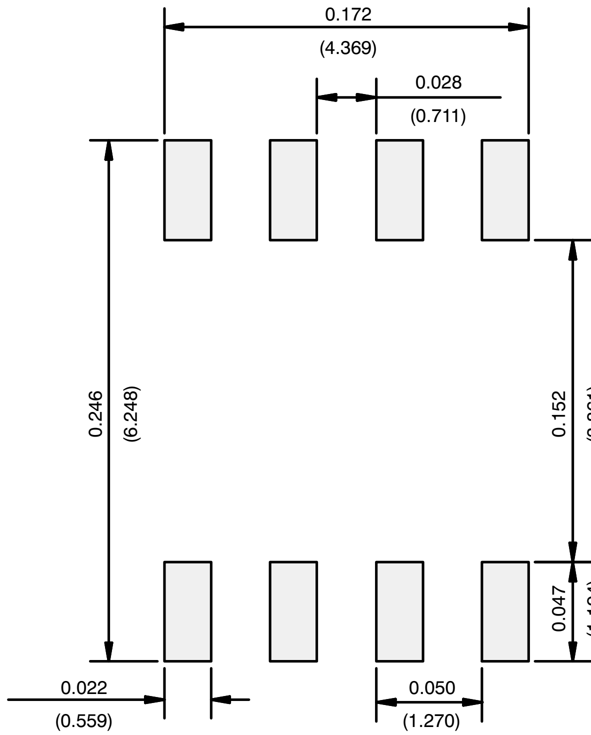
Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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