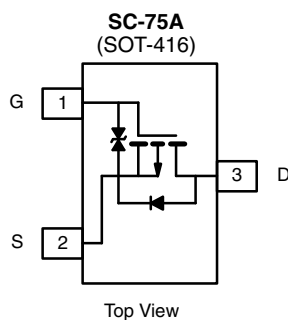


P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

$V_{DS(min.)}$ (V)	$R_{DS(on)}$ (Ω)	$V_{GS(th)}$ (V)	I_D (mA)
- 60	4.0 at $V_{GS} = - 10$ V	- 1 to 3.0	- 190



Marking Code: F

Ordering Information: Si1021R-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- High-Side Switching
- Low On-Resistance: 4 Ω
- Low Threshold: - 2 V (typ.)
- Fast Switching Speed: 20 ns (typ.)
- Low Input Capacitance: 20 pF (typ.)
- Miniature Package
- ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Power Supply Converter Circuits
- Solid-State Relays

BENEFITS

- Ease in Driving Switches
- Low Offset Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Easily Driven without Buffer
- Small Board Area

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C) ^a	$T_A = 25$ °C	I_D - 190	mA
	$T_A = 85$ °C	- 135	
Pulsed Drain Current ^b	I_{DM}	- 650	
Power Dissipation ^a	$T_A = 25$ °C	P_D 250	mW
	$T_A = 85$ °C	130	
Maximum Junction-to-Ambient ^a	R_{thJA}	500	°C/W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 10 μA	- 60			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 0.25 mA	- 1		- 3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 10	μA
		V _{DS} = 0 V, V _{GS} = ± 10 V			± 200	
		V _{DS} = 0 V, V _{GS} = ± 10 V, T _J = 85 °C			± 500	
		V _{DS} = 0 V, V _{GS} = ± 5 V			± 100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 50 V, V _{GS} = 0 V			- 25	nA
		V _{DS} = - 50 V, V _{GS} = 0 V, T _J = 85 °C			- 250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -10 V, V _{GS} = - 4.5 V	- 50			mA
		V _{DS} = -10 V, V _{GS} = - 10 V	- 600			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 25 mA			8	Ω
		V _{GS} = - 10 V, I _D = - 500 mA			4	
		V _{GS} = - 10 V, I _D = - 500 mA, T _J = 125 °C			6	
Forward Transconductance	g _{fs}	V _{DS} = - 10 V, I _D = - 100 mA	80			mS
Diode Forward Voltage ^a	V _{SD}	V _{DS} = - 200 mA, V _{GS} = 0 V	80			V
Dynamic						
Total Gate Charge	Q _g	V _{DS} = - 30 V, V _{GS} = - 15 V, I _D ≅ - 500 mA		1.7		nC
Gate-Source Charge	Q _{gs}			0.26		
Gate-Drain Charge	Q _{gd}			0.46		
Input Capacitance	C _{iss}	V _{DS} = - 25 V, V _{GS} = 0 V, f = 1 MHz		23		pF
Output Capacitance	C _{oss}			10		
Reverse Transfer Capacitance	C _{rss}			5		
Switching ^b						
Turn-On Time	t _{ON}	V _{DD} = - 25 V, R _L = 150 Ω, I _D ≅ - 200 mA, V _{GEN} = - 10 V, R _g = 10 Ω		20		ns
Turn-Off Time	t _{OFF}			35		

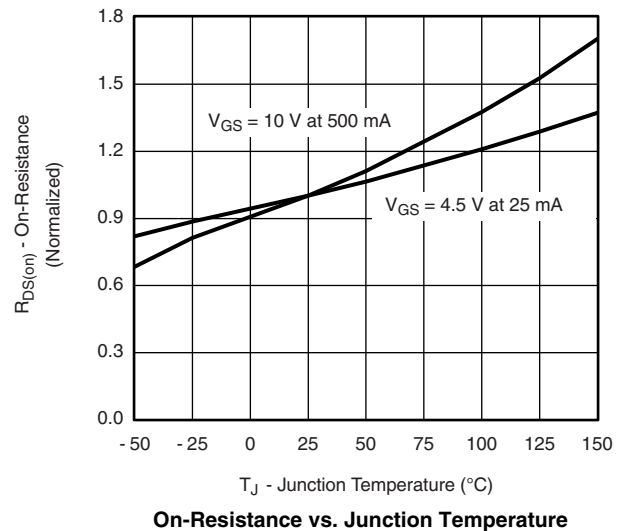
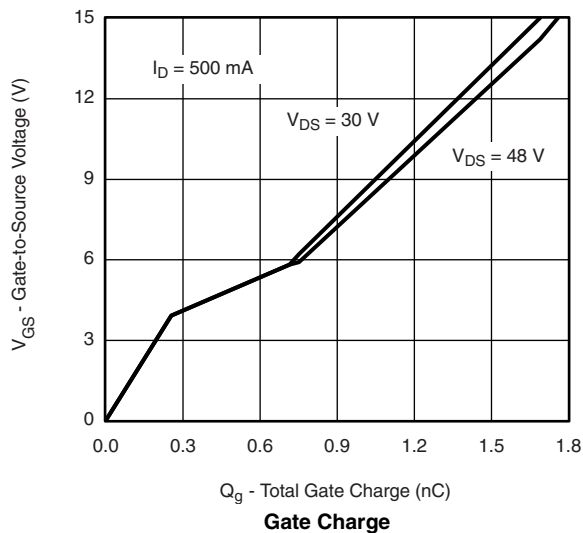
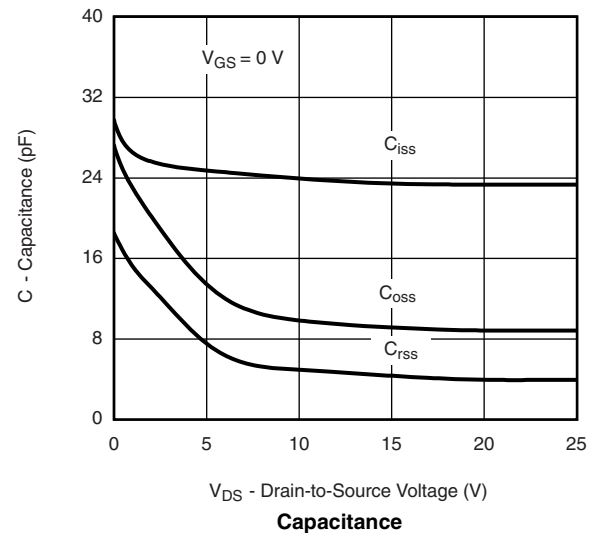
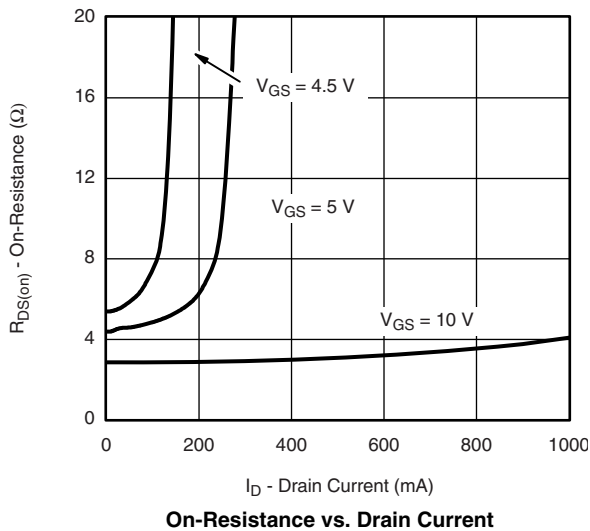
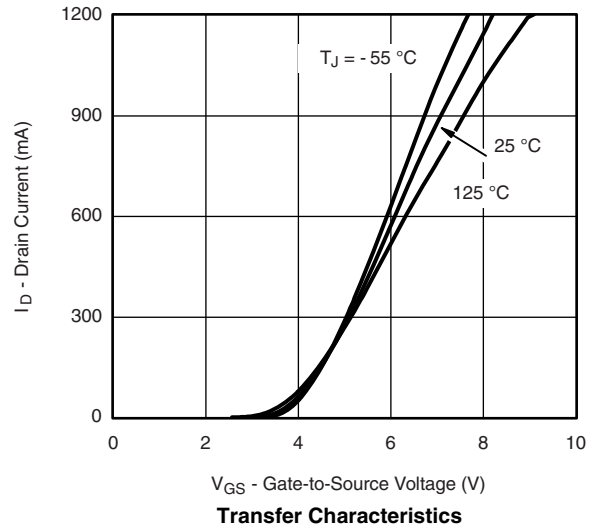
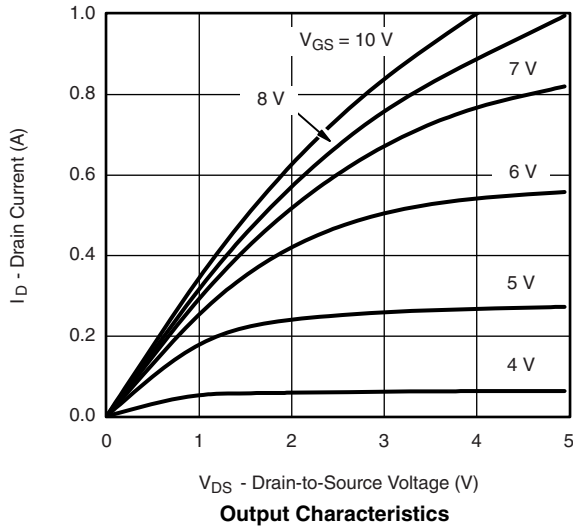
Notes:

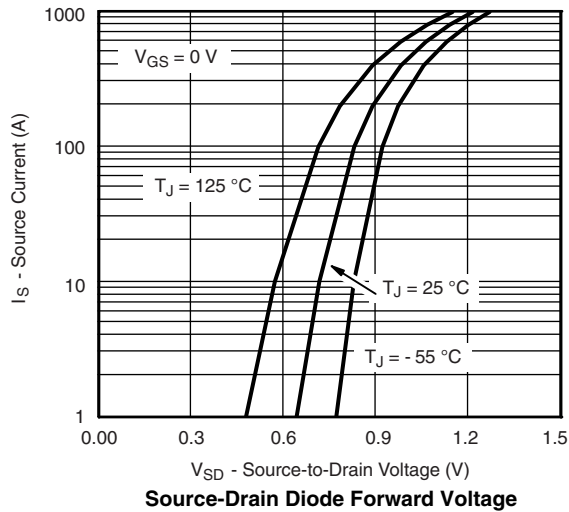
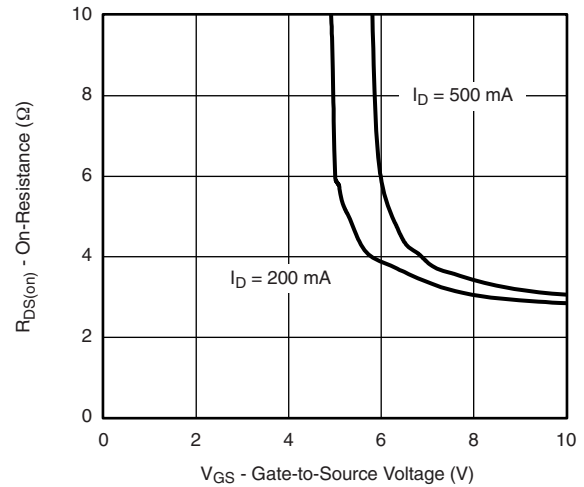
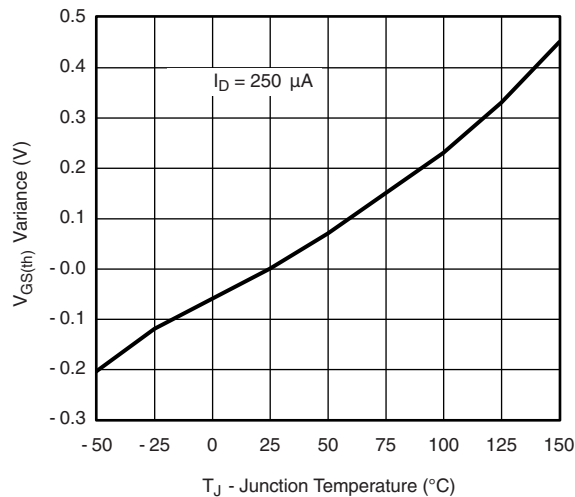
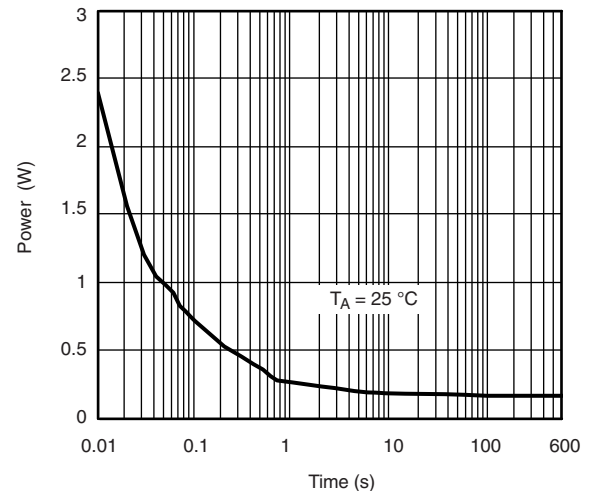
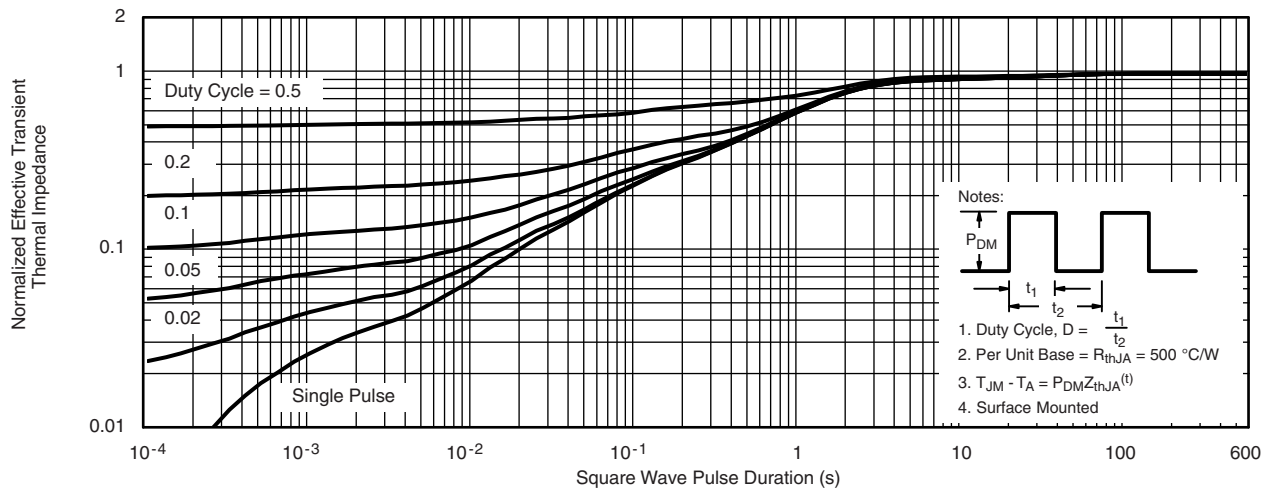
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

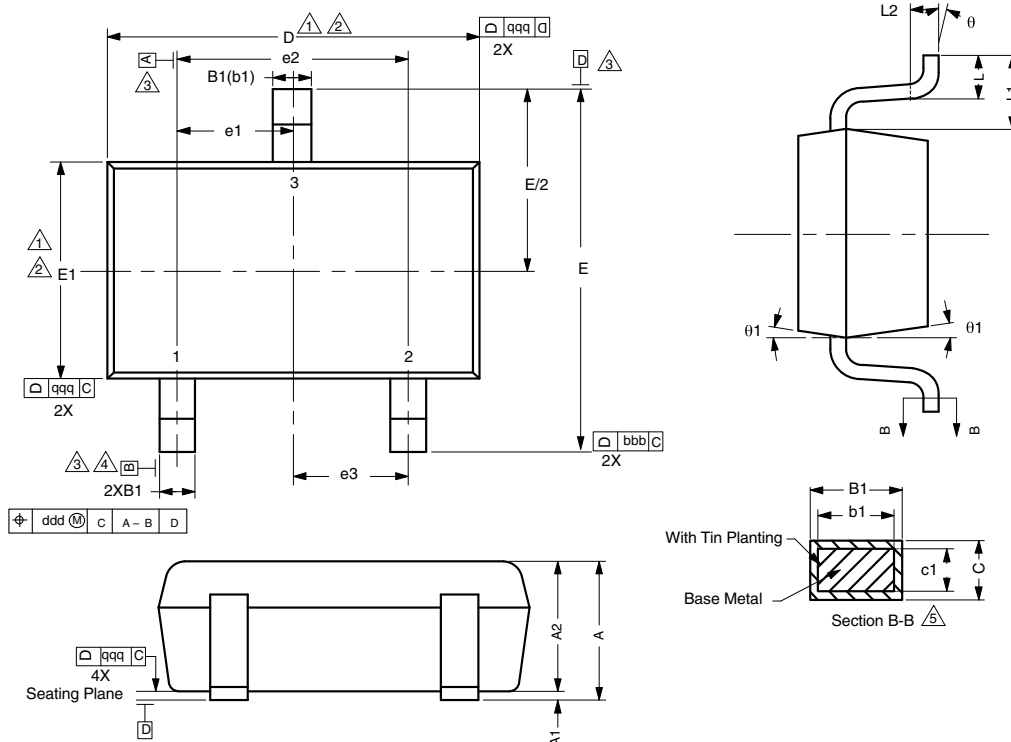


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-Source Voltage****Threshold Voltage Variance Over Temperature****Single Pulse Power, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Ambient**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71410.



SC-75A: 3-LEADS



Notes

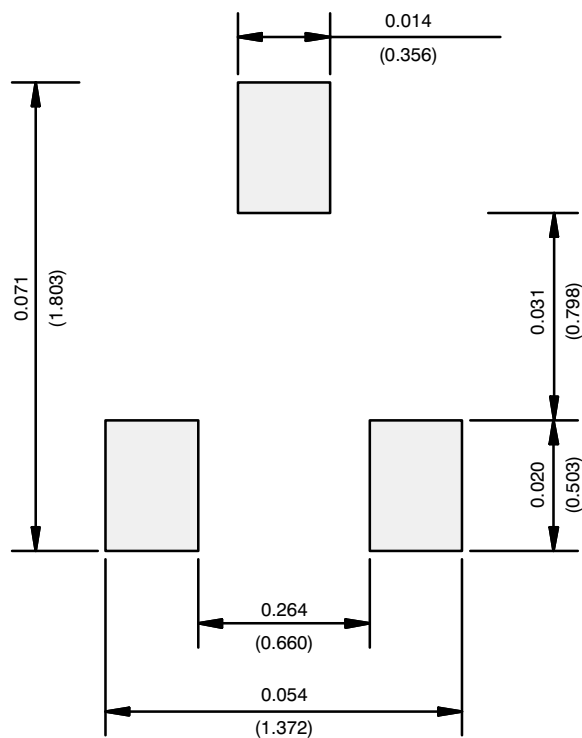
Dimensions in millimeters will govern.

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. Datums A, B and D to be determined 0.10 mm from the lead tip.
4. Terminal positions are shown for reference only.
5. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	-	-	0.80	
A ₁	0.00	-	0.10	
A ₂	0.65	0.70	0.80	
B ₁	0.19	-	0.24	5
b ₁	0.17	-	0.21	
c	0.13	-	0.15	5
c ₁	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E ₁	0.66	0.76	0.86	1, 2
e ₁	0.50 BSC			
e ₂	1.00 BSC			
e ₃	0.50 BSC			
L	0.15	0.205	0.30	
L ₁	0.40 REF			
L ₂	0.15 BSC			
θ	0°	-	8°	
θ_1	4°	-	10°	
ECN: E11-2210-Rev. D, 08-Aug-11				
DWG: 5868				

RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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