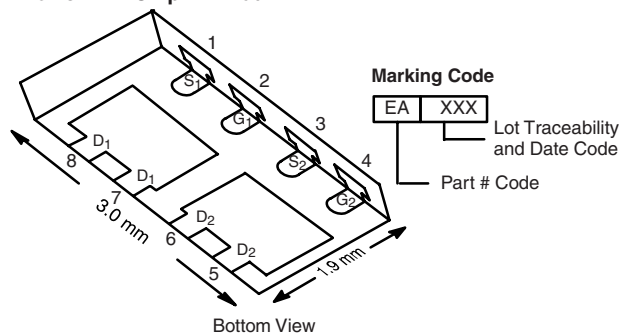


N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS}	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g
N-Channel	20	0.039 at V _{GS} = 4.5 V	6	6 nc
		0.045 at V _{GS} = 2.5 V	6	
		0.055 at V _{GS} = 1.8 V	6	
P-Channel	- 20	0.072 at V _{GS} = - 4.5 V	- 6	5.5 nc
		0.100 at V _{GS} = - 2.5 V	- 6	
		0.131 at V _{GS} = - 18 V	- 6	

PowerPAK ChipFET Dual



Ordering Information: Si5517DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

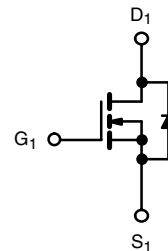
- Halogen-free
- TrenchFET® Power MOSFETs
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile



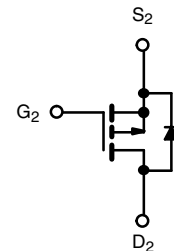
RoHS
COMPLIANT

APPLICATIONS

- Complementary MOSFET for Portable Devices
- Ideal for Buck-Boost Circuits



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	- 20	V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	6 ^a	- 6 ^a	A
	T _C = 70 °C		6 ^a	- 6 ^a	
	T _A = 25 °C		7.2 ^{b, c}	- 4.6 ^{b, c}	
	T _A = 70 °C		5.8 ^{b, c}	- 3.7 ^{b, c}	
Pulsed Drain Current		I _{DM}	20	- 15	W
Source-Drain Current Diode Current	T _C = 25 °C	I _S	6.9	- 6.9	
	T _A = 25 °C		1.9 ^{b, c}	- 1.9 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	8.3	8.3	W
	T _C = 70 °C		5.3	5.3	
	T _A = 25 °C		2.3 ^{b, c}	2.3 ^{b, c}	
	T _A = 70 °C		1.5 ^{b, c}	1.5 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	45	55	45	55	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	12	15	12	15	

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 105 °C/W for both channels.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	N-Ch	20			V	
		V _{GS} = 0 V, I _D = - 1 mA	P-Ch	- 20				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		17		mV/°C	
		I _D = - 250 μA	P-Ch		- 20			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 2.6			
		I _D = - 250 μA	P-Ch		2.4			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.4		1	V	
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 0.4		- 1		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	N-Ch P-Ch	 		100 - 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = - 20 V, V _{GS} = 0 V	P-Ch			- 1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10		
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 10		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ 5 V, V _{GS} = 4.5 V	N-Ch	20			A	
		V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	P-Ch	- 15				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.4 A	N-Ch		0.032	0.039	Ω	
		V _{GS} = - 4.5 V, I _D = - 3.3 A	P-Ch		0.060	0.072		
		V _{GS} = 2.5 V, I _D = 4.1 A	N-Ch		0.037	0.045		
		V _{GS} = - 2.5 V, I _D = - 2.8 A	P-Ch		0.083	0.100		
		V _{GS} = 1.8 V, I _D = 1.8 A	N-Ch		0.0455	0.055		
		V _{GS} = - 1.8 V, I _D = - 0.76 A	P-Ch		0.108	0.131		
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 4.4 A	N-Ch		22		S	
		V _{DS} = - 10 V, I _D = - 3.3 A	P-Ch		9			
Dynamic ^a								
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch P-Ch	 	520 455		pF	
Output Capacitance	C _{oss}		N-Ch P-Ch	 	100 105			
Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch P-Ch	 	60 65			
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 8 V, I _D = 4.4 A	N-Ch		10.5	16	nC	
		V _{DS} = - 10 V, V _{GS} = - 8 V, I _D = - 4.6 A	P-Ch		9.1	14		
		N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.4 A	N-Ch P-Ch	 	6 5.5	9 8.5		
			Gate-Source Charge	Q _{gs}	N-Ch P-Ch	 		0.91 0.75
Gate-Drain Charge	Q _{gd}	P-Channel V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 1.8 A	N-Ch P-Ch	 	0.7 1.5			
Gate Resistance	R _g	f = 1 MHz	N-Ch P-Ch	 	1.9 8			Ω

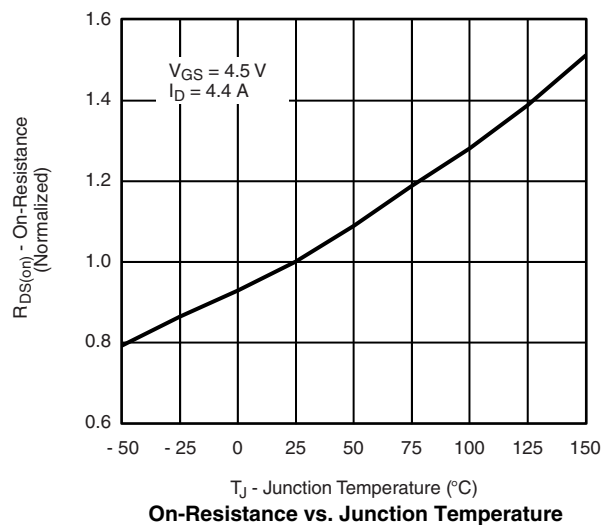
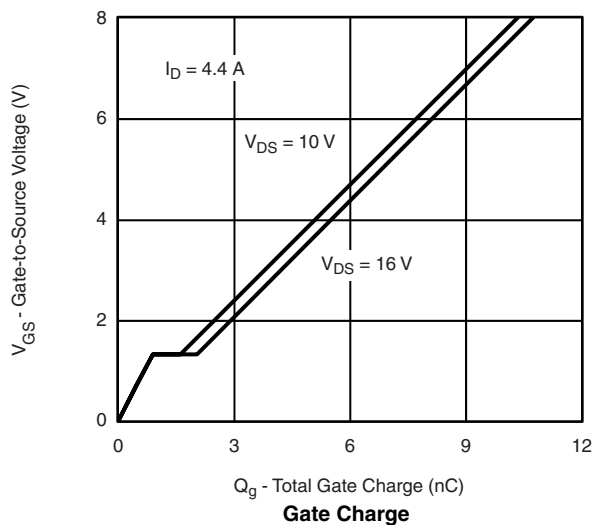
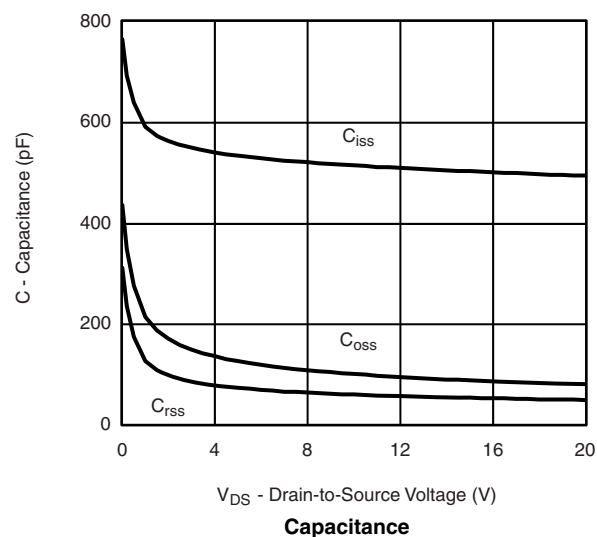
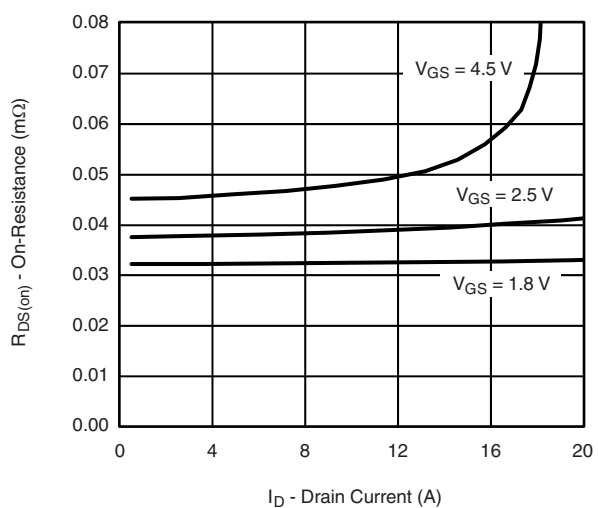
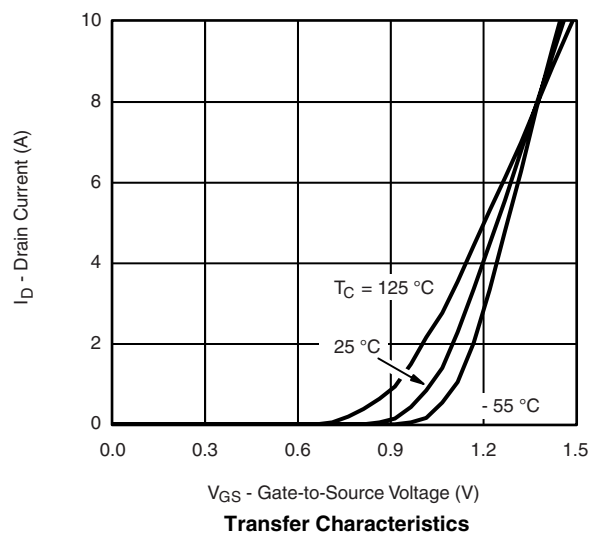
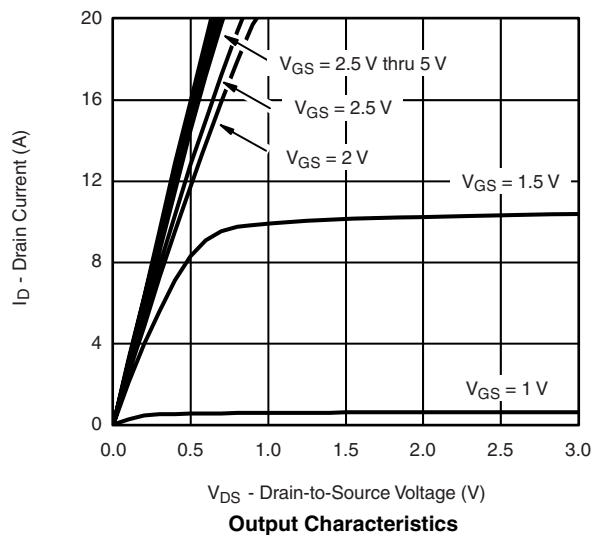


SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit	
Dynamic ^a								
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 2.8 Ω I _D ≅ 3.6 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch		20	30	ns	
			P-Ch		8	15		
Rise Time	t _r		N-Ch		65	100		
			P-Ch		35	55		
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 10 V, R _L = 2.7 Ω I _D ≅ - 3.7 A, V _{GEN} = - 4.5 V, R _g = 1 Ω	N-Ch		40	60		
			P-Ch		40	60		
Fall Time	t _f		N-Ch		10	15		
			P-Ch		55	85		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 2.8 Ω I _D ≅ 3.6 A, V _{GEN} = 8 V, R _g = 1 Ω	N-Ch		5	10		
			P-Ch		5	10		
Rise Time	t _r		N-Ch		12	20		
			P-Ch		15	25		
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 10 V, R _L = 2.7 Ω I _D ≅ - 3.7 A, V _{GEN} = - 8 V, R _g = 1 Ω	N-Ch		26	40		
			P-Ch		30	45		
Fall Time	t _f		N-Ch		8	15		
			P-Ch		45	70		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch			6.9	A	
			P-Ch			- 6.9		
Pulse Diode Forward Current ^a	I _{SM}		N-Ch			20		
			P-Ch			- 15		
Body Diode Voltage	V _{SD}	I _S = 1.2 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V	
		I _S = - 1.0 A, V _{GS} = 0 V	P-Ch		- 0.8	- 1.2		
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 1.2 A, dI/dt = 100 A/μs, T _J = 25 °C	N-Ch		45	70	ns	
			P-Ch		30	60		
Body Diode Reverse Recovery Charge	Q _{rr}			N-Ch		21	32	nC
				P-Ch		15	30	
Reverse Recovery Fall Time	t _a	P-Channel I _F = - 1 A, dI/dt = 100 A/μs, T _J = 25 °C	N-Ch		29		ns	
			P-Ch		11			
Reverse Recovery Rise Time	t _b			N-Ch		16		
				P-Ch		19		

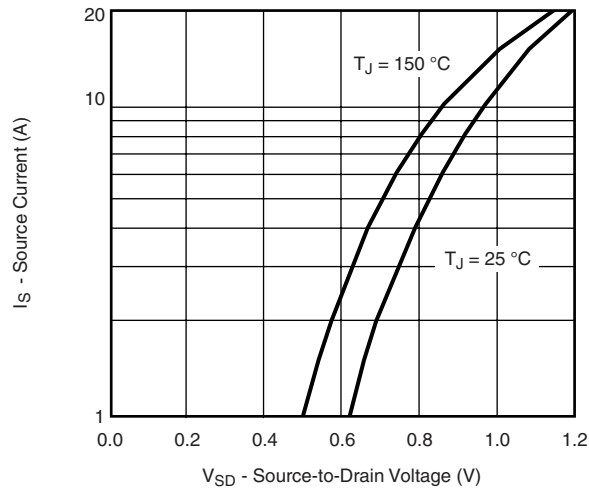
Notes:

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\text{ }\%$.

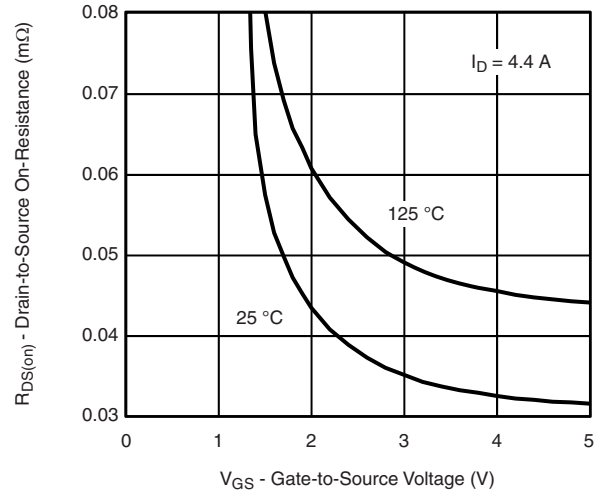
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

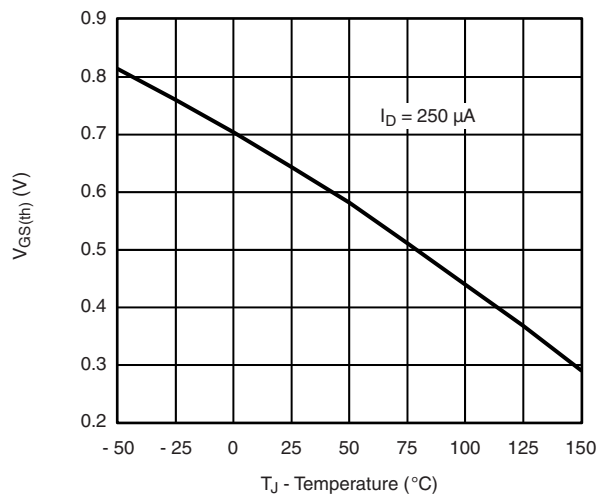
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



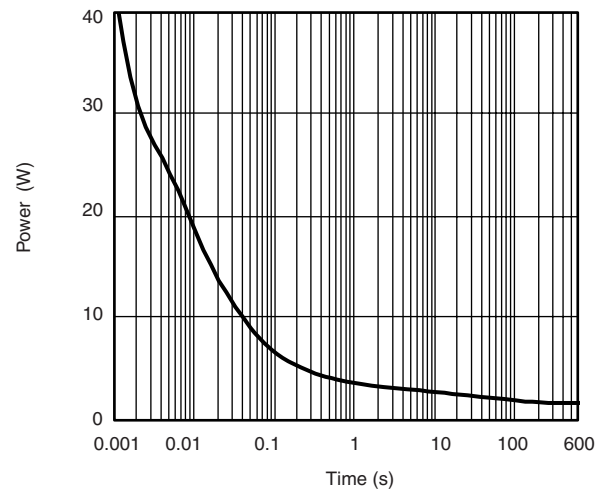
Source-Drain Diode Forward Voltage



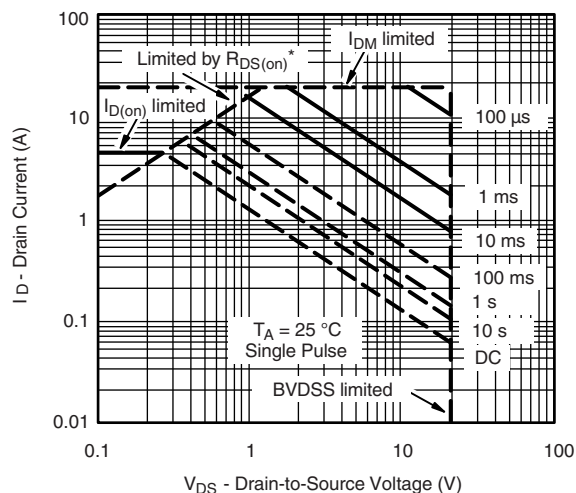
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

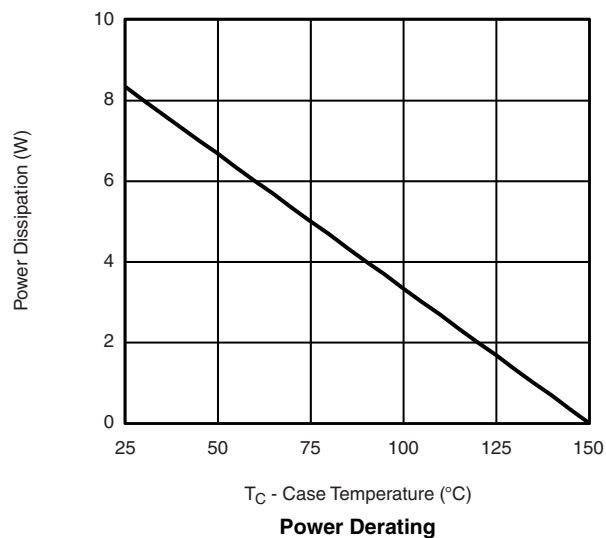
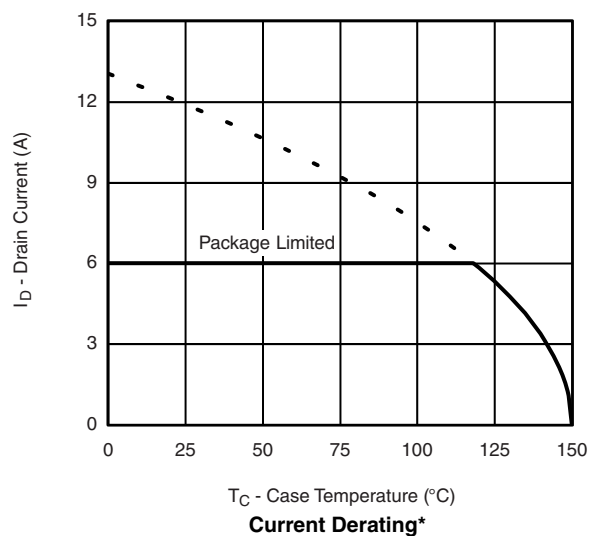


Single Pulse Power, Junction-to-Ambient



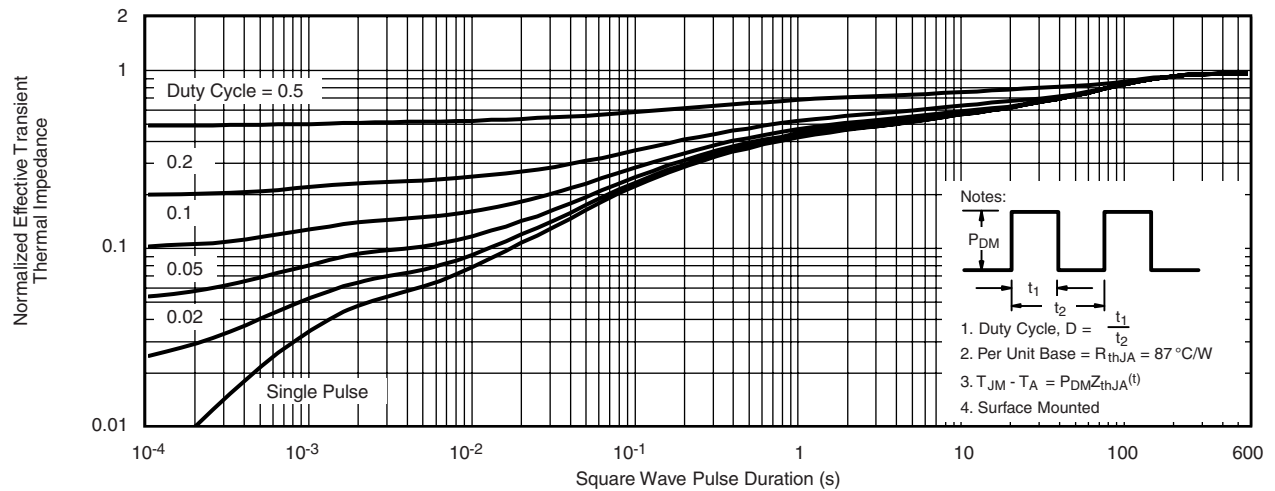
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

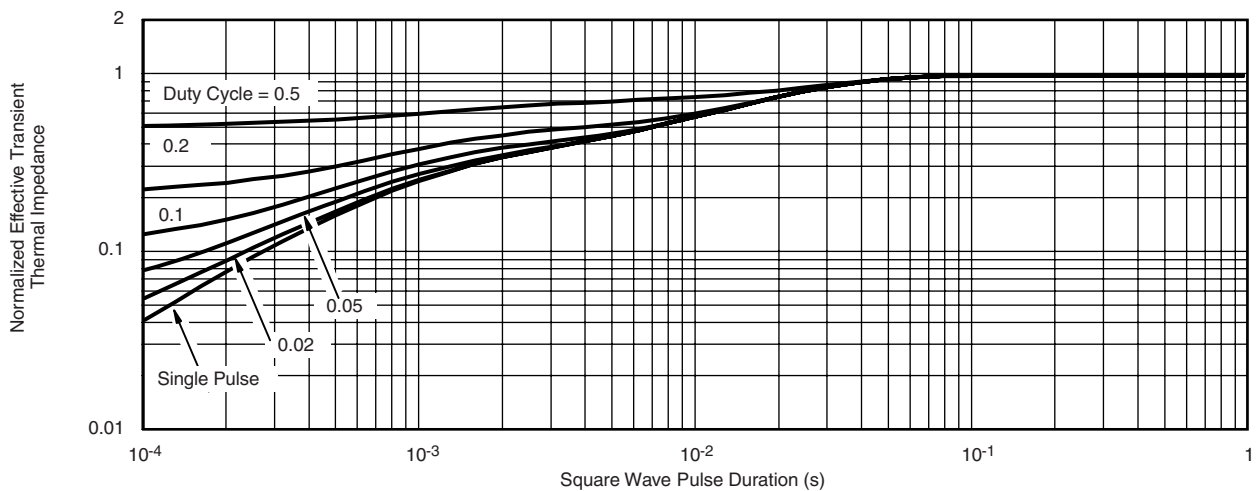
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

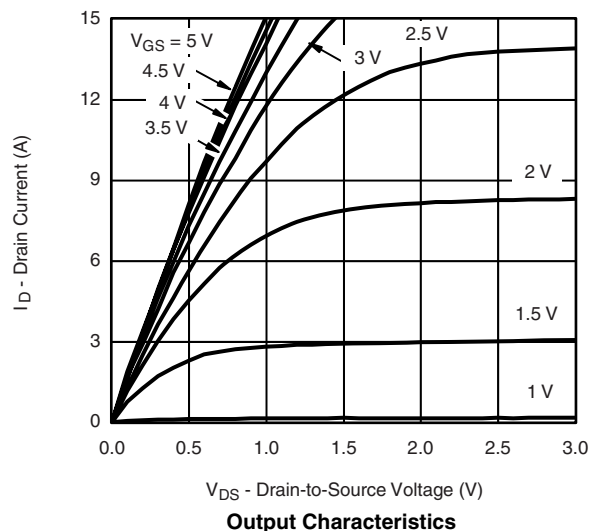
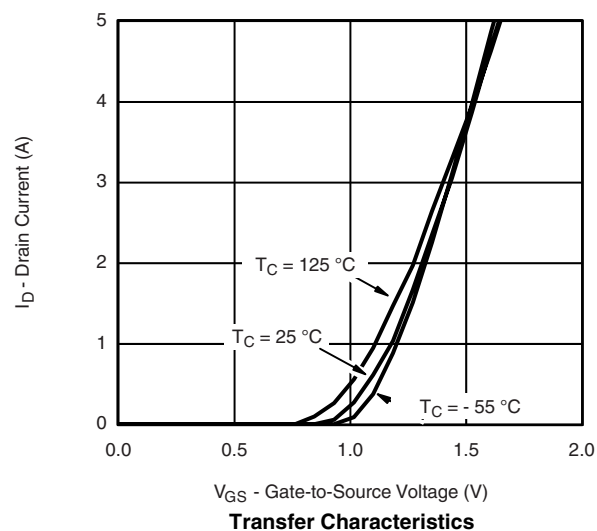
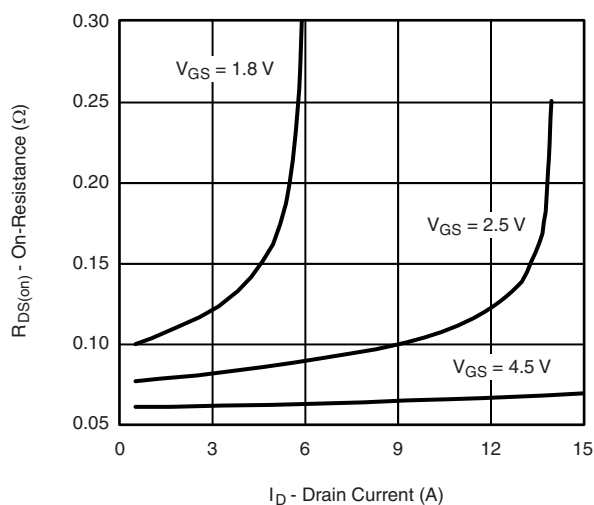
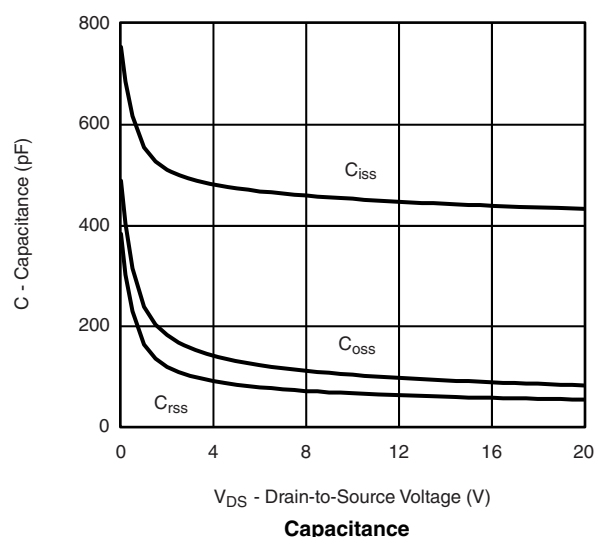
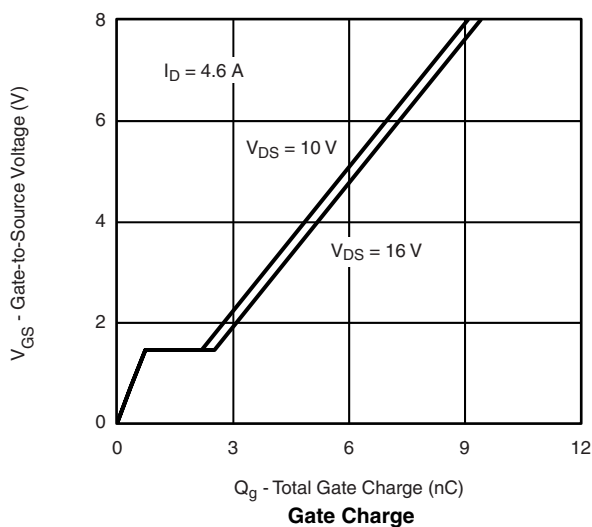
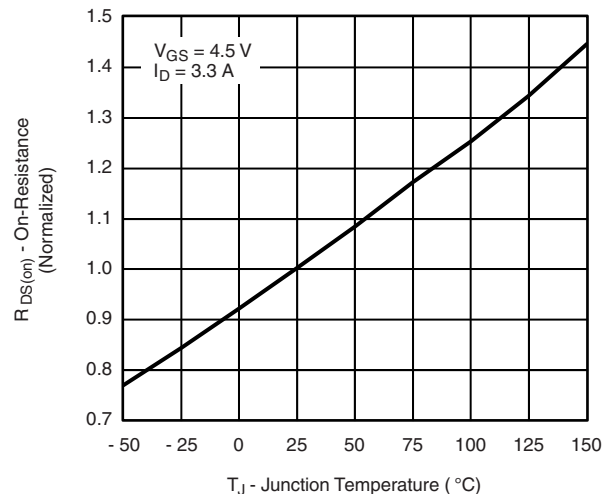
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



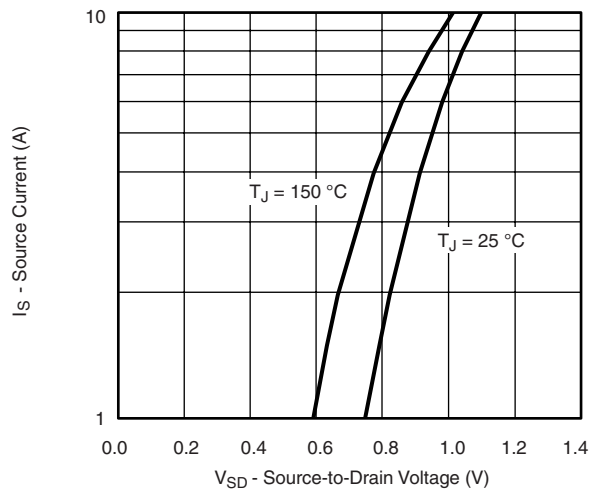
Normalized Thermal Transient Impedance, Junction-to-Ambient



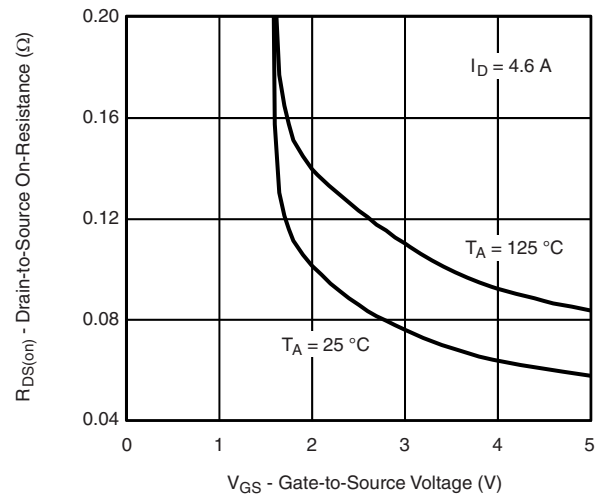
Normalized Thermal Transient Impedance, Junction-to-Case

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

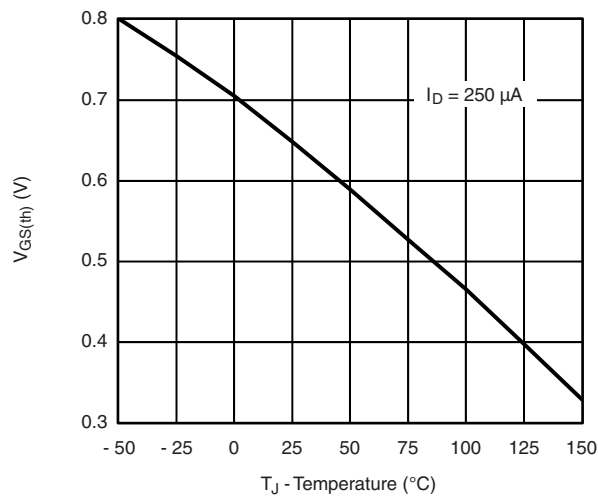
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



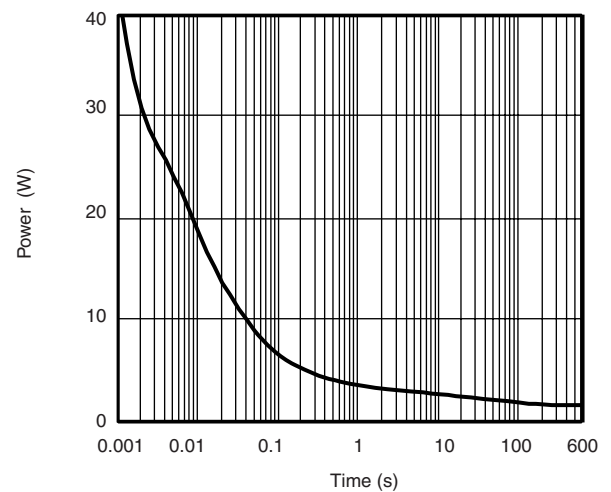
Source-Drain Diode Forward Voltage



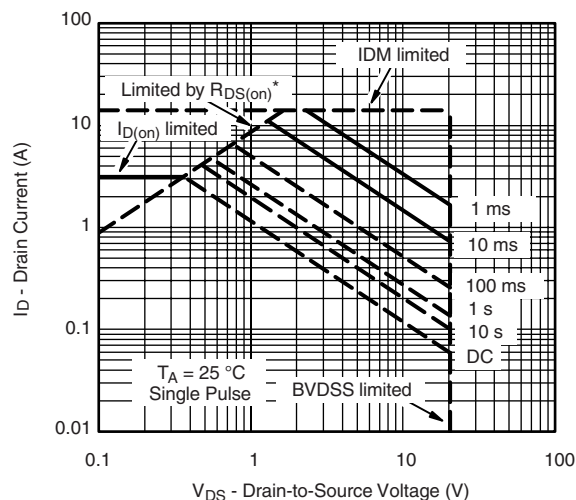
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

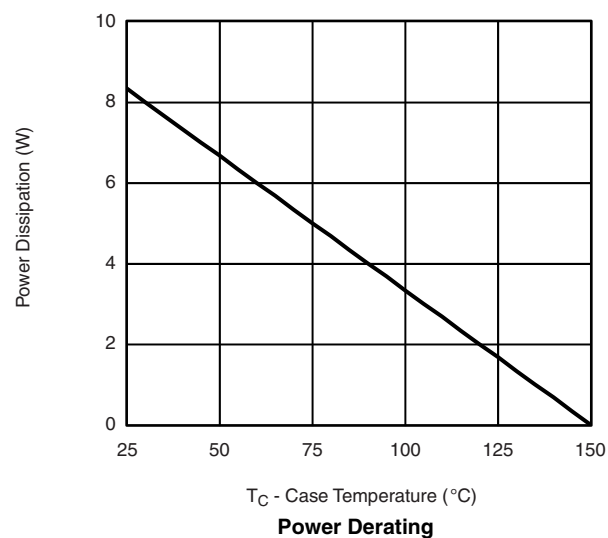
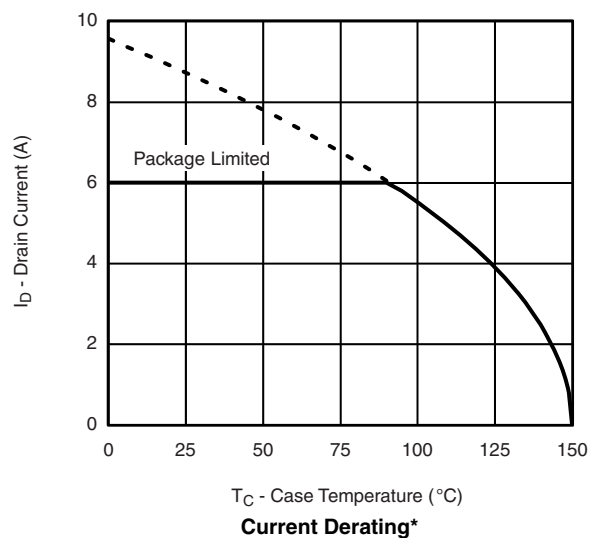


Single Pulse Power, Junction-to-Ambient



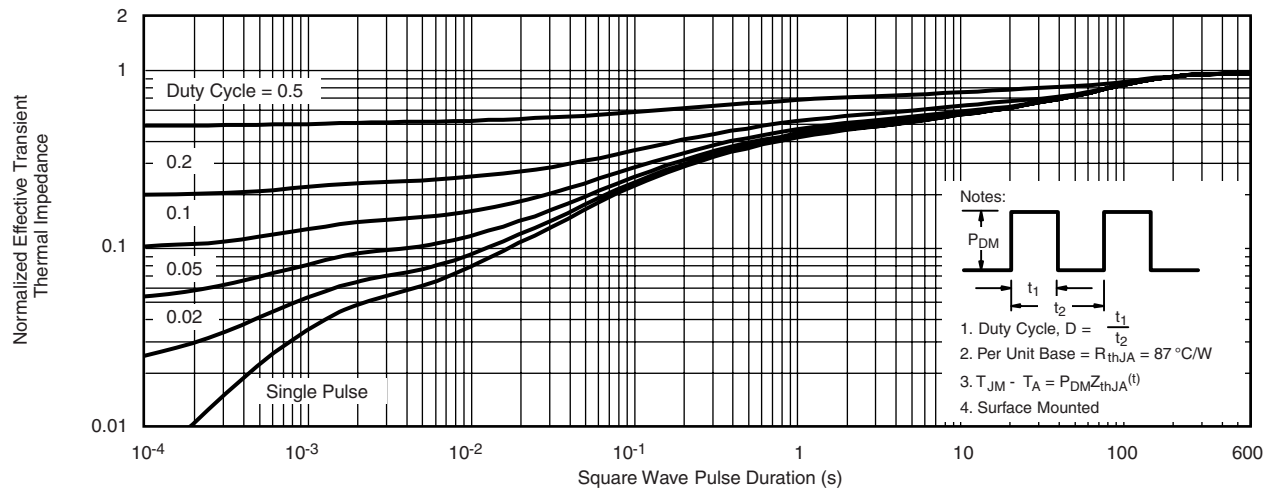
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

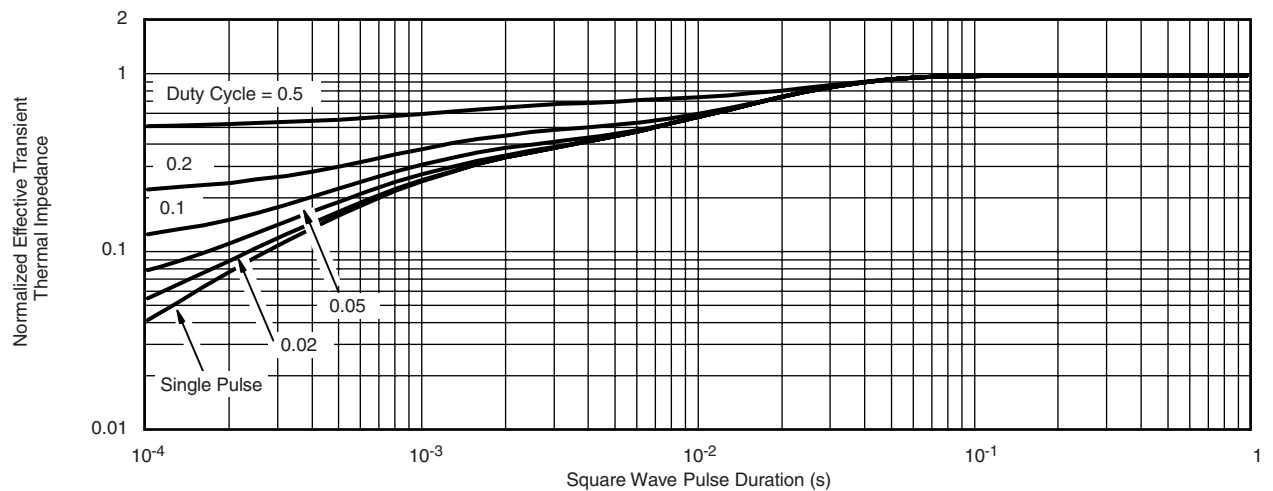
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

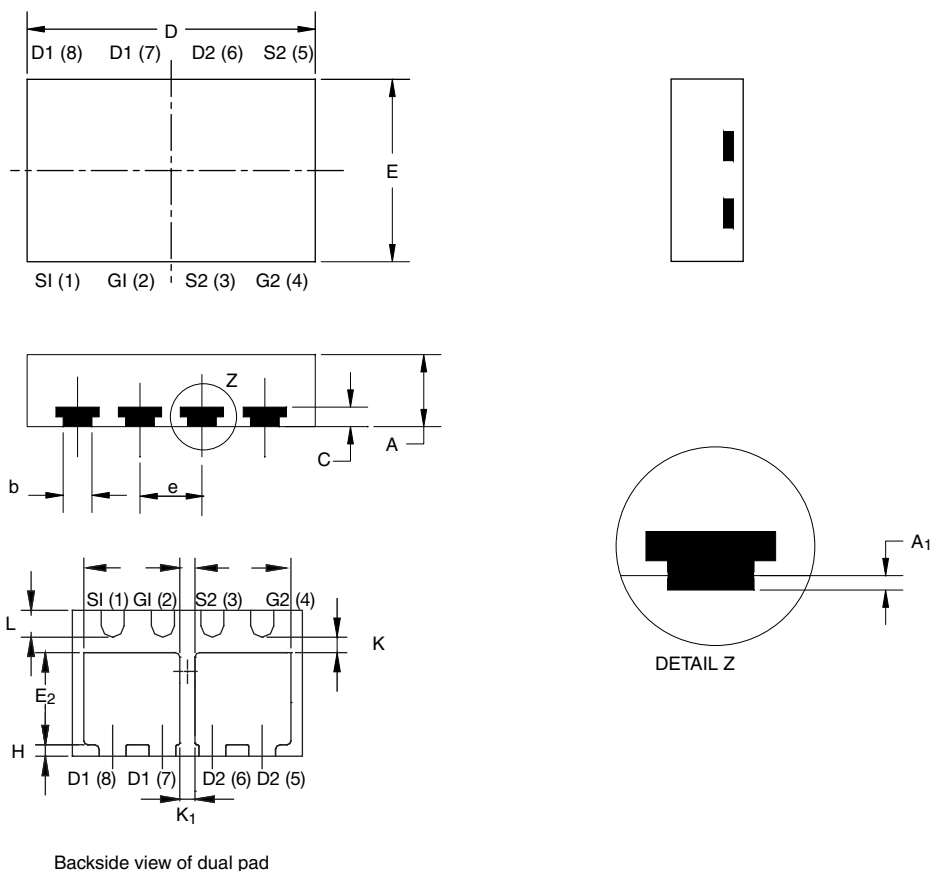


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73529>.



PowerPAK® ChipFET® DUAL PAD

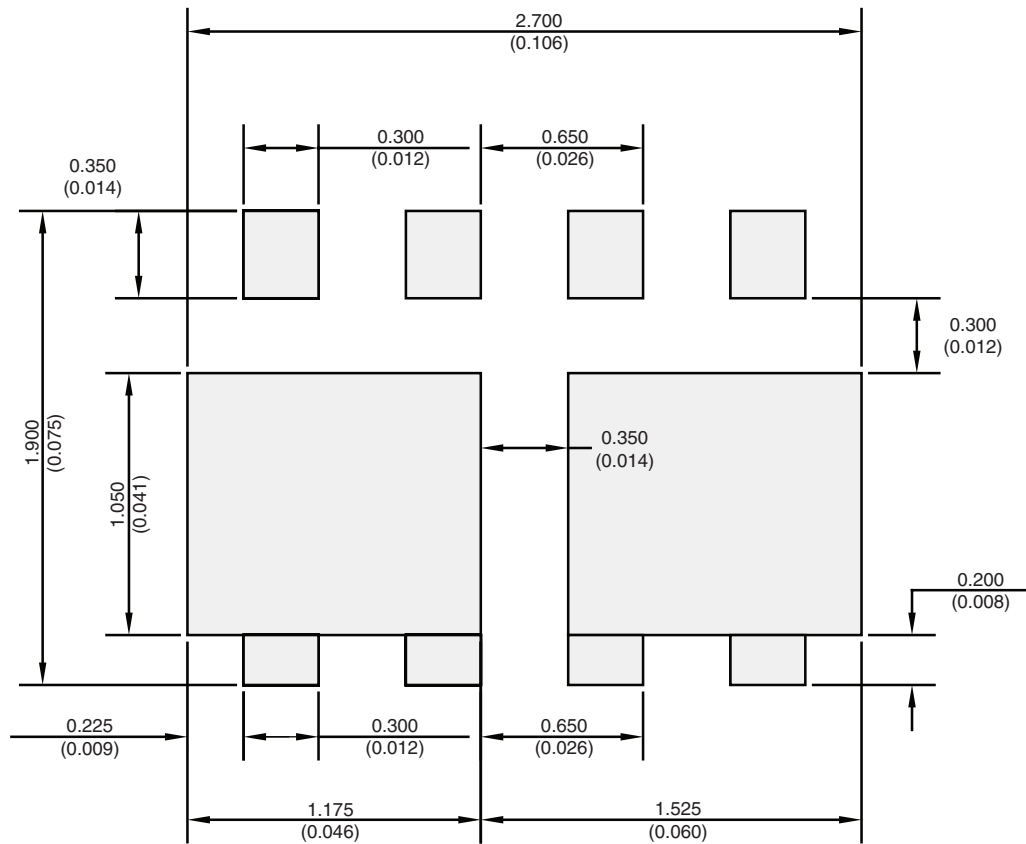


Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.07	1.20	1.32	0.042	0.047	0.052
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K ₁	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

ECN: C10-0618-Rev. C, 19-Jul-10
DWG: 5940

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner



Disclaimer

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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.