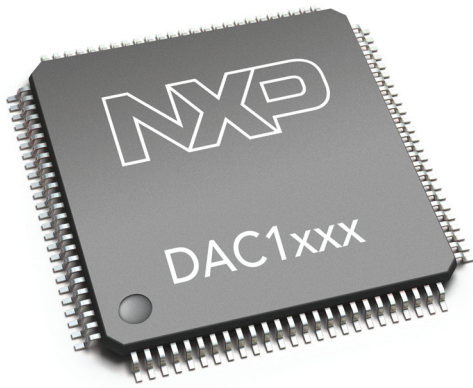




NXP dual-channel 10/12/14-bit, 650 Msps DAC family DAC1x05D650

Reach the exact frequency placement in your signal bandwidth

Designed for signal-synthesis applications, these dual-channel DACs operate with update rates as high as 650 Msps. They're available in 10-, 12, and 14-bit formats, and are functionally compatible with industry equivalents.

Key benefits

- ▶ Exact frequency placement via 32-bit NCO
- ▶ Enhanced application performance with best-in-class ACLR
- ▶ Reduced BoM and simpler PCB layout with integrated, high-performance PLL
- ▶ Easier implementation of interface timings with interleaved input data bus
- ▶ Easy design-in with functional compatibility

Key features

- ▶ 10/12/14-bit resolution with up to 650 Msps update rate
- ▶ Input rate up to 320 Msps
- ▶ Interpolation filter: 2x, 4x, 8x
- ▶ Low-power, fine-frequency mixer with 32-bit NCO
- ▶ CMOS input data bus: dual port or interleaved
- ▶ Differential and scalable output current up to 20 mA
- ▶ 10 bits of auxiliary DAC for gain matching and offset control
- ▶ Integrated, cap-free PLL with very low noise
- ▶ Excellent IMD3
- ▶ Inverse sinc filter
- ▶ Serial Peripheral Interface (SPI)
- ▶ 100-lead TQFP (14 x 14 x 1 mm) with exposed die pad

Applications

- ▶ Wireless infrastructure (CDMA, W-CDMA, TD-SCDMA, GSM, WiMAX)
- ▶ Communication (LMDS/MMDS, point-to-point)
- ▶ Direct Digital Synthesis (DDS)
- ▶ Instrumentation
- ▶ Automated Test Equipment (ATE)

The NXP DAC1x05D650 family delivers exceptional dynamic performance, low noise, low crosstalk, and superior PLL phase noise.

The DAC1405D650 has 14-bit resolution, an SFDR of 84 dBc ($F_{out} = 35$ MHz), and is functionally compatible with AD9788, AD9779A, DAC5688, and DAC5687 devices.

The DAC1205D650 has 12-bit resolution, an SFDR of 83 dBc ($F_{out} = 35$ MHz), and is functionally compatible with AD9787 and AD9778A devices.

The DAC1005D650 has 10-bit resolution, an SFDR of 81 dBc ($F_{out} = 35$ MHz), and is functionally compatible with AD9785 and AD9776A devices.

All can operate with their own digital inputs or can be used as interleaved DACs, with data alternatively written from a single digital input path to either of the two DACs.

Input data can be interpolated 2x, 4x, or 8x with a maximum update rate of 650 Msps. The inverse SinX function compensates for natural DAC SinX/X frequency roll-off, and there are on-chip features for gain and offset compensation.

Housed in a 100-lead TQFP package that measures 14 x 14 x 1 mm and has an exposed die pad, they are specified over the extended industrial temperature range (-40 to +85 °C) and are pin-to-pin compatible with each other.

Selection guide

Part no.	Resolution	SFDR (Fout = 35 MHz)	IMD3	Functional compatibility	Package
DAC1405D650	14-bit	84 dBc	81 dBc	AD9788 AD9779A DAC5688 DAC5687	HTQFP100
DAC1205D650	12-bit	83 dBc	80 dBc	AD9787 AD9778A	HTQFP100
DAC1005D650	10-bit	81 dBc	78 dBc	AD9785 AD9776A	HTQFP100

DAC1405 Demo Board

