NXP dual 11, 12, 14, 16 bits ADC
ADC1113D series
ADC1213D series
ADC1413D series
ADC1613D series

Dual-channel ADCs with JESD204A-compliant outputs for wireless and industrial

NXP advanced dual channel ADC integrates a two-lane CGV™ serial interface, JEDEC JESD204A-compliant, optimized for high-speed applications.

Key features

- SNR: 71.6 dB typical, SFDR: 89 dBc typical
- Maximum sample rate: up to 65, 80, 105, or 125 Msps
- Dual-channel - 11, 12, 14 and 16-bit resolution - pipelined ADC core with dual-stage linearity calibration
- Two highly configurable JEDEC JESD204A-compliant CGV™ serial output lanes
- SPI control/status interface
- HVQFN56 package

Applications

- Wireless and wired broadband communications, especially multicarrier standards
- Wideband spectral analysis
- Industrial imaging systems
- Medical equipment
- Instrumentation

The NXP ADC1413D series comprises dual-channel analog-to-digital converters (ADCs) that support serial digital transmission in compliance with the new JEDEC JESD204A interface standard. Only one CGV™ transmitter per channel is necessary to support sample rates of 125 Msps and to carry out 16-bit resolution.

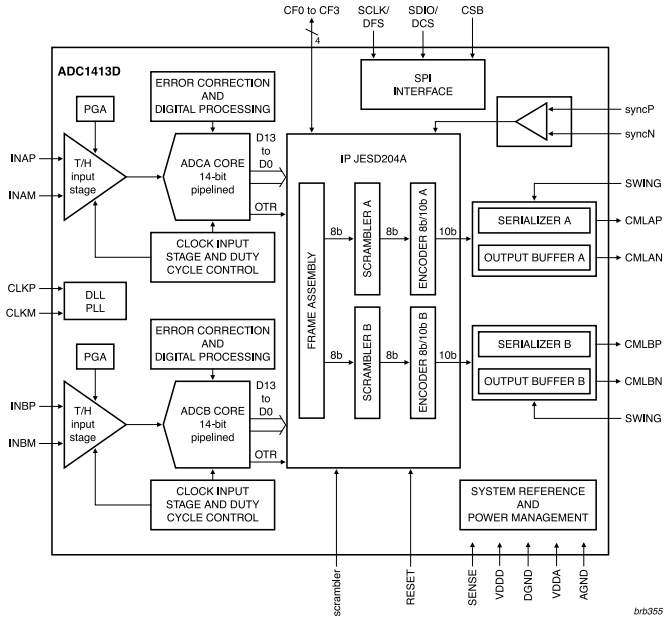
CGV™ (Convertisseur Grande Vitesse) designates NXP's compliant, superset implementation of the JEDEC JESD204A interface standard, with enhanced rate (4.0 Gbps typical), enhanced reach (100 cm typical), enhanced features (multiple DAC synchronization) and assured FPGA interoperability. Specifically, NXP offers enhancements in terms of transceiver rate (up to 4.0 Gbps versus the standard rate of 3.125 Gbps, a 28% increase), and transmitter reach (up to 100 cm versus the standard reach of 20 cm, a 400% increase).

The ADCs maintain excellent dynamic performances from baseband to input frequency up to 600 MHz, making them ideal for applications in communications, industrial imaging, and medical equipment.

The ADCs operate from a single 3-V supply for the analog circuitry and a 1.8-V supply for the digital output drivers.

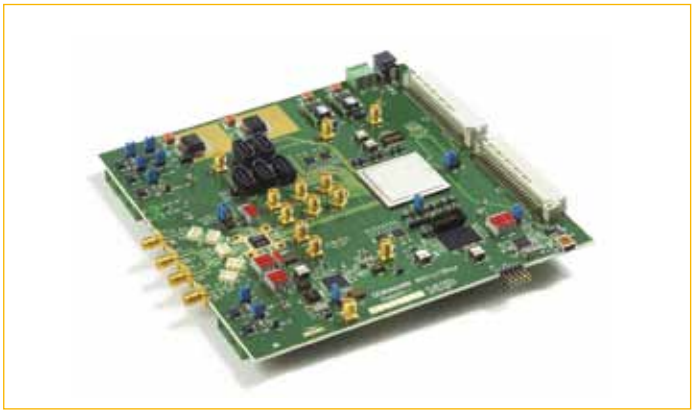
The addition of a Serial Peripheral Interface (SPI) makes the ADCs and their JEDEC serial output modes easy to configure and monitor.
All these products and versions are pin to pin compatible which allows easy upgrade in end application.

ADC1413D block diagram



ADC1413D125 demonstration board, for easy connection to Altera, Xilinx or Lattice evaluation kits.

Example of Reference design with ADC and FPGA



ADC1X13D selection table

Family	Type	Description	Imput Buffer	TTL/ CMOS	LVCMOS	LVDS/ DDR	CGV™	Supply Voltage (V)	Power Dissipation per channel (mW)	SFDR (dBc)	SNR (dBFS)	Package
ADC1613D series	ADC1613D125	Dual 16-bit ADC up to 125Msps					●	1.8 / 3.0	635	89	71.6	HVQFN56 8x8
ADC1413D series	ADC1413D125	Dual 14-bit ADC up to 125Msps					●	1.8 / 3.0	635	87	71.4	HVQFN56 8x8
ADC1213D series	ADC1213D125	Dual 12-bit ADC up to 125Msps					●	1.8 / 3.0	635	87	69.6	HVQFN56 8x8
ADC1113D125	ADC1113D125	Dual 11-bit ADC up to 125Msps					●	1.8 / 3.0	635	87	66.2	HVQFN56 8x8

Other maximum samples rates (105, 080, 065 Msps) are also available for ADC1613D, ADC1413D and ADC1213D

ADC Demo Boards

Family	Type	Description
ADC1413D series	ADC1413D065W1/DB	ADC1413D065 demo board; VIRTEX 5 FPGA on board
	ADC1413D065WO/DB	ADC1413D065 demo board; compliant with Lattice, Altera, Xilinx FPGA boards through specific connectors

Demo boards are also available for all resolutions (11, 12, 14 and 16-bit) and all speeds (125, 105, 080, 065 Msps)

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Date of release: June 2010
Document order number: 9397 750 16875
Printed in the Netherlands