PIC18F26K20/46K20

PIC18F26K20/46K20 Rev. B2/B3/B5/B6 Silicon Errata and Data Sheet Clarification

The PIC18F26K20/46K20 family devices that you have received conform functionally to the current Device Data Sheet (DS41303**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F26K20/46K20 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B6**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F26K20/46K20 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1) (11-bit)	Revision ID for Silicon Revision(2) (5-bit)			
		B2	B3	B5	B6
PIC18F26K20	100h	0x09	0x0A	0x0C	0x0D
PIC18F46K20	101h	0x09	0x0A	0x0C	0x0D

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:DEVREV".

2: Refer to the *"PIC18F2XK20/4XK20 Flash Programming Specification"* (DS41297) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				B2	B3	B5	B6
ECCP	Full-Bridge	1.	Dead-band time is 4/FOSC instead of 1/FOSC.	X	X	X	X
ECCP	Full-Bridge	2.	Compromised dead band.	X	X	X	X
MSSP SPI	SPI Clock	3.	Improper start in Timer2/2 Clock mode.	X	X	X	X
MSSP SPI	SPI Master	4.	Improper sampling of last bit.	X	X	X	X
MSSP (Master I2C™ Mode)	I2C™ Master	5.	Improper handling of Stop event.	X	X	X	X
EUSART	OERR Flag	6.	Clearing SPEN bit does not clear OERR flag.	X	X	X	X
EUSART	BAUDCON	7.	RCIDL may improperly stay low.	X	X	X	X
System Clocks	HFINTOSC	8.	Frequency instability.	X			
Data EEPROM Memory	Endurance	9.	Endurance limited to 10K cycles.	X	X	X	X
Program Flash Memory	Endurance	10.	Endurance limited to 1K cycles.	X	X	X	X
PORTB Interrupt-on-Change	Interrupt-on-change	11.	False interrupt when setting interrupt enable.	X	X	X	X
ADC	ADC Conversion	12.	ADC conversion may be limited to half scale.	X	X		
Interrupt-on-Change	Interrupt-on-change interrupt when in Sleep	13.	False interrupt when waking from Sleep.	X	X	X	X
Capture/Compare/PWM	Capture mode	14.	Weak pull-up disabled in Capture mode on CCP2	X	X	X	X
Low-Voltage Detect	LVD in Sleep	15.	LVD erroneously triggers upon wake-up from Sleep if band gap is disabled in Sleep mode.	X	X	X	X
Resets (BOR)	Brown-out Reset	16.	An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B6**).

1. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead-band time of 4/FOSC * TMR2 prescale instead of 1/FOSC * TMR2 prescale as specified in the data sheet.

Work around

None.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

2. Module: ECCP

ECCP – In Full-Bridge mode when PR2 = CCPR1L and DC1B[1:0] <>'00' and the direction is changed, then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for TOSC * TMR2Presale * DC1B[1:0].

Work around

Avoid changing direction when the duty cycle is within three least significant steps of 100% duty cycle. Instead, clear the DC1B[1:0] bits before the direction change and then set them to the desired value after the direction change is complete.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

3. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011) and the CKE bit of the SSPSTAT register is '1', then the first SDO data bit and SCK non-idle edge occur simultaneously. Also, the first SCK non-idle level may be short.

Work around

Use clock mode other than Timer2/2.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

4. Module: MSSP SPI

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

5. Module: MSSP (Master I²C™ Mode)

In Master I²C Receive mode, if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. When a Start condition occurs after the improper Stop condition, then 9 additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches, which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear stuck RCEN bit by clearing SSPEN bit of SSPCON1.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

6. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

7. Module: EUSART

In Asynchronous Receive mode when the RX input goes low after an Idle period and stays low for less than 1/16th bit period, then that event will be correctly detected as an invalid Start bit. If the RX input goes low a second time, less than one full bit time after the leading edge of the first invalid Start time, then the low transition of the RCIDL Status bit will be improperly delayed by one full bit time following that second edge. If the second pulse is also an invalid Start bit then the RCIDL will remain low indefinitely until either a valid Start bit occurs or the EUSART is reset.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART receiver. The EUSART receiver is reset when either the SPEN bit or CREN bit of the RCSTA register is cleared.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

8. Module: System Clocks

HFINTOSC output frequency may have up to 1% short term frequency instability beyond the maximum and minimum limits shown in the data sheet.

Work around

Use the HS, XT or EC clock modes.

Affected Silicon Revisions

B2	B3	B5	B6				
X							

9. Module: Data EEPROM Memory

The write/erase endurance of data EEPROM memory is limited to 10K cycles.

Work around

Use the error correction method that stores data in multiple locations.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

10. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when V_{DD} is above 3V. Endurance degrades when V_{DD} is below 3V.

Work around

For data tables in program Flash memory use the error correction method that stores data in multiple locations.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

11. Module: PORTB Interrupt-on-Change

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

Work around

Set the IOCB bits to the desired configuration then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

12. Module: ADC

After extended stress the Most Significant bit (MSb) of the ADC conversion result can become stuck at '0'. Conversions resulting in code 511 or less are still accurate, but conversions that should result in codes greater than 511 are instead pinned at 511.

The potential for failures is a function of several factors:

- The potential for failures increases over the life of the part. No failures have ever been seen for accelerated stress estimated to be equivalent to 34 years at room temperature. The failure rate after accelerated stress estimated to be equivalent to 146 years at room temperature can be as high as 10% for VDD = 1.8V. The time to failure will decrease as the operating temperature increases.
- The potential for failures is highest at low VDD and decreases as VDD increases.

Work around

1. Restrict the input voltage to less than 1/2 of the ADC voltage reference so that the expected result is always a code less than or equal to 511.
2. Use manual acquisition time (ACQT<2:0> = 000) and put the part to Sleep after each conversion.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X						

13. Module: Interrupt-on-Change

When any interrupt-on-change is enabled and the corresponding input is high, then waking from Sleep by a source other than interrupt-on-change may cause the RBIF interrupt flag bit to become set improperly.

Work around

1. Use the INTx interrupts in lieu of interrupt-on-change.

   Or

2. Store the state of the PORTB inputs before entering Sleep. Upon waking, if an RBIF is detected, then compare the PORTB levels with those stored. If they are the same, then clear and ignore the RBIF interrupt.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

14. Module: Capture/Compare/PWM

14.1 CCP2

The weak pull-up (if enabled) on the selected CCP2 pin will be disabled when CCP2 is set up for Capture mode.

Work around

Use an external resistor as the pull-up.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

15. Module: Low-Voltage Detect

If Low-Voltage Detect is enabled, the band gap is disabled in Sleep, and the part is put to Sleep for a short period of time, the LVD will trigger immediately upon waking-up from Sleep.

Work around

Do not disable the band gap in Sleep when using the LVD.

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

16. Module: Resets (BOR)

An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled when the Fixed Voltage Reference is not enabled (CVRCON2<7> = 0). This issue affects BOR modes: BOREN<1:0> = 10 and BOREN<1:0> = 01. In both of these modes, if the BOR module is re-enabled while the device is active, unexpected Resets may be generated.

Work around

If BOR is required, and power consumption is not an issue, use BOREN<1:0> = 11. For BOREN<1:0> = 10 mode, either switch to BOREN<1:0> = 11 mode or enable the FVR (CVRCON2<7> = 1) and verify that the FVR is stable (CVRCON2<6> = 1) prior to entering Sleep. If power consumption is an issue and low power is desired, do not use BOREN<1:0> = 10 mode. Instead, use BOREN<1:0> = 01 and follow the steps below when entering and exiting Sleep.

1. Disable BOR by clearing SBOREN(RCON<6> = 0) and the FVR (CVRCON2<7> = 0).
2. Enter Sleep mode (if desired). `Sleep();`
3. After exiting Sleep mode (if entered) enable the FVR (CVRCON2<7> = 1).
4. Wait for the Fixed Voltage Reference to stabilize (typically 25 us).

   `while(!CVRCON2bits.FVRST);`
5. Re-enable BOR by setting SBOREN (RCON<6> = 1).

Affected Silicon Revisions

B2	B3	B5	B6				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303**G**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

Parameter D026 in Table 26-8 on page 376 of the data sheet lists the maximum ADC delta current at 1.8V as 290 µA. The correct value should be 360 µA.

TABLE 26-8: DC CHARACTERISTICS: PERIPHERAL SUPPLY CURRENT, PIC18F2XK20/4XK20

PIC18F2XK20/4XK20		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	**Device Characteristics**	**Typ**	**Max**	**Units**	**Conditions**		
	Module Differential Currents						
D024 (ΔIWDT)	**Watchdog Timer**	0.7	2.0	µA	-40°C to +125°C	VDD = 1.8V	
		1.1	3.0	µA	-40°C to +125°C	VDD = 3.0V	
D024A (ΔIBOR)	**Brown-out Reset(2)**	21	50	µA	-40°C to +125°C	VDD = 2.0V	
		25	60	µA	-40°C to +125°C	VDD = 3.3V	
		0	—	µA	-40°C to +125°C	VDD = 3.3V	Sleep mode, BOREN<1:0> = 10
D024B (ΔIHLVD)	**High/Low-Voltage Detect(2)**	13	30	µA	-40°C to +125°C	VDD = 1.8-3.0V	
D025 (ΔIOSCB) LP	**Timer1 Oscillator**	0.5	2.0	µA	-40°C	VDD = 1.8V	32 kHz on Timer1(1)
		0.5	2.0	µA	+25°C		
		0.7	2.0	µA	+85°C		
		0.7	3.0	µA	-40°C	VDD = 3.0V	32 kHz on Timer1(1)
		0.7	3.0	µA	+25°C		
		0.9	3.0	µA	+85°C		
D025A (ΔIOSCB) HP	**Timer1 Oscillator**	11	30	µA	-40°C	VDD = 1.8V	32 kHz on Timer1(3)
		13	33	µA	+25°C		
		15	35	µA	+85°C		
		14	33	µA	-40°C	VDD = 3.0V	32 kHz on Timer1(3)
		17	37	µA	+25°C		
		19	40	µA	+85°C		
D026 (ΔIAD)	**A/D Converter(4)**	200	**360**	µA	-40°C to +125°C	VDD = 1.8V	A/D on, not converting
		260	425	µA	-40°C to +125°C	VDD = 3.0V	
ΔIFRC		2	5	µA	-40°C to +125°C	VDD = 1.8V	Adder for FRC
		11	18	µA	-40°C to +125°C	VDD = 3.0V	

Note 1: Low-Power mode on T1 osc. Low-Power mode is limited to 85°C.

2: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

3: High-Power mode in T1 osc.

4: A/D converter differential currents apply only in RUN mode. In SLEEP or IDLE mode both the ADC and the FRC turn off as soon as conversion (if any) is complete.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (9/2008)

Initial release of this document.

Rev B Document (5/2009)

Updated Errata to new format.

Added Module 5. MSSP Master I^2C Mode; Added Module 6. EUSART; Added Module 12. ADC.

Clarifications/Corrections to the Data Sheet:
Removed Modules 1-3.

Rev C Document (6/2009)

Revised Table 1: Silicon DEVREV Values.

Clarifications/Corrections to the Data Sheet: Added Module 1: Electrical Specifications; Added Module 2: Electrical Specifications; Added Module 3 MSSP: Register 17-3 SSPADD; Added Module 4 MSSP: Section 17.4.2 Operation; Added Module 5 MSSP: Figure 17-16 MSSP Block Diagram; Added Module 6 MSSP: Sections 17.4.7.1, 17.4.8, 17.4.9, 17.4.17.1, 17.4.17.2, 17.4.17.3: SSPADD, changing <6:0> to <7:0>.

Rev D Document (3/2010)

Silicon Errata Issues: Added Module 13; Updated Table 2.

Data Sheet Clarifications:

Removed Modules 1-6.

Rev E Document (7/2010)

Removed ADC Work around #2 and changed #3 to #2 (Module 12).

Rev F Document (2/2012)

Updated errata to new format; Added Module 14, Capture/Compare/PWM.

Rev G Document (4/2012)

Added MPLAB X IDE; Added Silicon Revision B6.

Rev H Document (5/2013)

Added Module 15, Low-Voltage Detect and Module 16, Reset (BOR).

Data Sheet Clarifications: Added Module 1, Electrical Characteristics.

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11/29/12