dsPIC33EPXXXGM3XX/6XX/7XX Family Silicon Errata and Data Sheet Clarification

The dsPIC33EPXXXGM3XX/6XX/7XX family devices that you have received conform functionally to the current Device Data Sheet (DS70000689**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of dsPIC33EPXXXGM3XX/6XX/7XX family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on Page 8, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33EPXXXGM3XX/6XX/7XX family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A0	A1			A0	A1
dsPIC33EP128GM304	0x1B40	0x4000	0x4001	dsPIC33EP256GM706	0x1B8B	0x4000	0x4001
dsPIC33EP128GM604	0x1B48			dsPIC33EP256GM310	0x1B87		
dsPIC33EP128GM306	0x1B43			dsPIC33EP256GM710	0x1B8F		
dsPIC33EP128GM706	0x1B4B			dsPIC33EP512GM304	0x1BC0		
dsPIC33EP128GM310	0x1B47			dsPIC33EP512GM604	0x1BC8		
dsPIC33EP128GM710	0x1B4F			dsPIC33EP512GM306	0x1BC3		
dsPIC33EP256GM304	0x1B80			dsPIC33EP512GM706	0x1BCB		
dsPIC33EP256GM604	0x1B88			dsPIC33EP512GM310	0x1BC7		
dsPIC33EP256GM306	0x1B83			dsPIC33EP512GM710	0x1BCF		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"dsPIC33EPXXXGM3XX/6XX/7XX Flash Programming Specification"* (DS70000685) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A0	A1
Core	CPU	1.	Limited execution speed (44/64-pin and 100/121-pin devices).	X	—
Core	Program Memory	2.	Address error trap may occur while accessing certain program memory locations.	X	X
SPI	Frame Sync Pulse	3.	When in SPI Slave mode, with the Frame Sync pulse set as an input, FRMDLY must be set to '0'.	X	X
SPI	Frame Master Mode	4.	Received data is right-shifted under certain conditions.	X	X
Input Capture	External Sync	5.	Input Capture and Output Compare modules cannot be synchronized.	X	X
PWM	Immediate Update	6.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.	X	X
PWM	Independent Time Base	7.	Under certain circumstances, updates to the OVRENH and OVRENL bits may be ignored by the PWM module.	X	X
PWM	Complementary Mode	8.	With dead time greater than zero, 0% and 100% duty cycle cannot be obtained on PWMxL and PWMxH outputs.	X	X
PWM	Center-Aligned Mode	9.	PHASEx register updates delayed.	X	X
PWM	Current Reset Mode	10.	PWM Resets only occur on alternate cycles in Current Reset mode.	X	X
ADC	DONE bit	11.	DONE does not work when an external interrupt is selected as the ADC trigger source.	X	X
ADC	—	12.	Selecting the same ANx input for CH0 and CH1 results in erroneous readings for CH1.	X	X
ECAN™	DMA	13.	Write collisions on a DMA-enabled ECAN module do not generate DMAC error traps.	X	X
JTAG	I/O	14.	$\overline{\text{MCLR}}$ pin operation may be disabled.	X	X
JTAG	I/O	15.	Active-high logic pulse on the I/O pin with TMS function at POR.	X	X
QEI	Velocity Counter	16.	Under certain circumstances, the Velocity Counter register (VELxCNT) misses count pulses.	X	X
FRC	FRC Accuracy	17.	Change in the FRC accuracy.	X	—

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Core

For 44/64-pin and 100/121-pin devices, code execution may be unreliable under the following conditions:

- From -40°C to +85°C for FOSC above 120 MHz (60 MIPS)
- From +85°C to +125°C for FOSC above 100 MHz (50 MIPS)
- From +125°C to +150°C for FOSC above 60 MHz (30 MIPS)

Work around

Do not use clock speeds above 120 MHz for applications operating in the Industrial temperature range (-40°C to +85°C) or above 100 MHz for temperatures in the Extended range (+85°C to +125°C) or above 60 MHz for high temperature range (+125°C to +150°C).

Affected Silicon Revisions

A0	A1						
X							

2. Module: Core

An unexpected address error trap may occur during accesses to program memory addresses, 001h through 200h. This has been observed when one or more interrupt requests are asserted while reading or writing program memory addresses using TBLRDH/L, TBLWTH/L or PSV-based instructions.

Work around

Before executing instructions that read or write program memory addresses, 001h through 200h, disable interrupts using the DISI instruction.

Affected Silicon Revisions

A0	A1						
X	X						

3. Module: SPI

When in SPI Slave mode (MSTEN bit (SPIxCON1<5>) = 0) and using the Frame Sync pulse output feature (FRMEN bit (SPIxCON2<15>) = 1) in Slave mode (SPIFSD bit (SPIxCON2<14>) = 1), the Frame Sync Pulse Edge Select bit (FRMDLY bit (SPIxCON2<1>) = 0) must be set to '0'.

Work around

None. The Frame Sync Pulse Edge Select bit, FRMDLY, cannot be set to produce a Frame Sync pulse that coincides with the first bit clock.

Affected Silicon Revisions

A0	A1						
X	X						

4. Module: SPI

When SPI is operating in Master mode and Framed SPI is enabled (SPIxCON1<5> = 1 and SPIxCON2<15> = 1), received data may be shifted to the right by one bit when the following conditions are also true:

- The Frame Sync pulse is configured as an output (SPISFD (SPIxCON2<14>) = 0).
- Input data is sampled at the end of data output time (SMP (SPIxCON1<9>) = 1).

Work around

Clear the SMP bit while using SPI Frame Master mode; this changes data sampling to the start of data output time.

Affected Silicon Revisions

A0	A1						
X	X						

5. Module: Input Capture

When an input capture module is selected as the Sync source for either an output compare module or another input capture module, synchronization may fail.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

6. Module: PWM

The PWM generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWM generator is configured to operate in Complementary mode with the independent time base or master time base.
- Immediate update is enabled.
- The value in the PDCx register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

7. Module: PWM

Under certain circumstances, an update to the IOCONx register to turn off the override will be ignored by the PWM module.

Work around

1. Turn off the PWM dead time.
2. Alternatively, turn off the PWM override with the following procedure:
   a) Disable the PWM module (PTEN = 0).
   b) Clear the Override Enable bits (OVRENH = 0 and OVRENL = 0).
   c) Enable the PWM module (PTEN = 1).

Affected Silicon Revisions

A0	A1						
X	X						

8. Module: PWM

This issue is applicable when a PWM generator is configured to operate in Independent Time Base mode with either Center-Aligned Complementary mode or Edge-Aligned Complementary mode. When dead time is non-zero, PWMxL is not asserted for 100% of the time when PDCx is zero. Similarly, when dead time is non-zero, PWMxH is not asserted for 100% of the time when PDCx is equal to PHASEx. This issue also applies to Master Time Base model.

Work around

In Center-Aligned mode:

- To obtain 0% duty cycle, zero out the ALTDTRx register, and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the ALTDTRx register, and then write (PHASEx + 2) to the PDCx register.

In Edge-Aligned mode:

- To obtain 0% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write (PHASEx + 1) to the PDCx register.

Affected Silicon Revisions

A0	A1						
X	X						

9. Module: PWM

In Center-Aligned Complimentary mode with independent time base, updates to the PHASEx register take effect after a delay of two PWM periods.

This occurs only when the Immediate Update Enable (IUE = 0) feature is disabled. If Immediate Update is enabled (IUE = 1), the PHASEx register updates will take effect immediately.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

10. Module: PWM

The PWM Reset may only occur on alternate PWM cycles, when both of the following conditions are met:

- The PWM generator is configured to operate in Current Reset mode (PWMCONx<1> = 1).
- Independent Time Base mode is selected (PWMCONx<9> = 1).

Work around

There are two proposed solutions; others may exist.

1. Software Solution: Generate an interrupt when the comparator state changes. The interrupt can either be a comparator or a PWM Fault interrupt and should be high priority. During this interrupt's service routine, update the Period Value register (PHASEx) with a value less than the programmed duty cycle (PDCx); then, immediately update PHASEx with the PWM period required by the application. Example 1 shows a possible implementation.

EXAMPLE 1:

```
PWMx ISR:
{           PHASEx = PDCx-100;
            PHASEx = PWM_PERIOD;
            PWMxIF = 0;
}
```

2. Hardware Solution: When the current Reset signal is coming from an external comparator selected by FCLCONx<14:10>, limit the pulse width of the external trigger to less than the maximum value specified in Table 3. Note that the maximum pulse width is determined by the PWM resolution, as selected by the PCLKDIV<2:0> bits (PTCON2<2:0>).

TABLE 3: MAXIMUM PULSE WIDTH FOR CURRENT-LIMIT SIGNAL

PCLKDIV<2:0>	Maximum Pulse Width (ns)
000	20
001	40
010	80
011	160
100	320
101	640
110	1280
111	2560

Affected Silicon Revisions

A0	A1						
X	X						

11. Module: ADC

The ADC Conversion Status (DONE) bit (ADxCON1<0>) does not indicate completion of a conversion when an external interrupt is selected as the ADC trigger source (SSRC<2:0> bits (ADxCON1<7:5>) = 0x1).

Work around

Use an ADC interrupt or poll the ADxIF bit in the IFSx registers to determine the completion of the conversion.

Affected Silicon Revisions

A0	A1						
X	X						

12. Module: ADC

Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.

Work around

Bring the analog signal into the device using both AN0 and AN3, connect externally, and then assign one input to CH0 and the other to CH1.

If selecting AN0 on CH1 (CH123Sx = 0), select AN3 on CH0 (CH0Sx = 3). Conversely, if selecting AN3 on CH1 (CH123Sx = 1), select AN0 on CH0 (CH0Sx = 0).

Affected Silicon Revisions

A0	A1						
X	X						

13. Module: ECAN™

When DMA is used with the ECAN module, and the CPU and DMA write to an ECAN Special Function Register (SFR) at the same time, the DMAC error trap does not occur. In addition, neither the PWCOL<3:0> bits of the DMAPWC SFR nor the DMACERR bit of the INTCON1 SFR become set. Since the PWCOLx bits are not set, subsequent DMA requests to that channel are not ignored.

Work around

There is no work around; however, under normal circumstances, this situation should not arise. When DMA is used with the ECAN module, the application should not be writing to the ECAN SFRs.

Affected Silicon Revisions

A0	A1						
X	X						

14. Module: JTAG

The $\overline{\text{MCLR}}$ pin (normally input only) may be set as an output pin through the JTAG interface. If it is set at an output high level, subsequent device Resets are prevented until the device is powered down.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

15. Module: JTAG

At Power-on Reset (POR), when JTAG is disabled in the Configuration bits, the I/O pin with TMS function produces an active-high logic pulse with a pulse width in the order of milliseconds.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

16. Module: QEI

The Velocity Counter (VELxCNT) is a 16-bit wide register that increments or decrements based on the signal from the quadrature decoder logic. Reading this register results in a Counter Reset. Typically, the user application should read the velocity counter at a rate of 1-4 kHz.

As a result of this issue, the velocity counter may miss a count if the user application reads the Velocity Counter register at the same time as a (+1 or -1) count increment occurs.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

17. Module: FRC

Refer Table 4 for change in FRC accuracy at FRC frequency = 7.3728 MHz.

TABLE 4: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended -40°C ≤ TA ≤ +150°C for High Temperature					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz							
F20a	FRC	-2	0.5	2	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0–3.6V
F20b	FRC	-3	1.5	3	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0–3.6V
HF20	FRC	-4	—	4	%	-40°C ≤ TA ≤ +150°C	VDD = 3.0–3.6V

Work around

None.

Affected Silicon Revisions

A0	A1						
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70000689**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2013)

Initial release of this document; issued for silicon revision A0.

Includes silicon issues 1 (Core, CPU), 2 (Core, Program Memory), 3-4 (SPI, Frame modes), 5 (Input Capture), 6-10 (PWM), 11-12 (ADC), 13 (ECAN), 14-15 (JTAG), and 16 (QEI).

Rev B Document (9/2013)

Added **17. Module: "FRC"** and updated Table 2

Added a new bulleted list in **17. Module: "FRC"**

Updated work around section in **17. Module: "FRC"**

Rev C Document (10/2013)

Updated Table 1 with new revision ID "A1".

Updated Table 2.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

Printed on recycled paper.

ISBN: 978-1-62077-525-7

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/20/13