dsPIC30F6011A/6012A/6013A/6014A Rev. A2 Silicon Errata

dsPIC30F6011A, dsPIC30F6012A, dsPIC30F6013A, dsPIC30F6014A (Rev. A2) Silicon Errata

The dsPIC30F6011A/6012A/6013A/6014A (Rev. A2) samples you have received were found to conform to the specifications and functionality described in the following documents:

- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"
- DS70143 – *"dsPIC30F6011A, dsPIC30F6012A, dsPIC30F6013A, dsPIC30F6014A Data Sheet"*
- DS70046 – "*dsPIC30F Family Reference Manual*"

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- dsPIC30F6011A
- dsPIC30F6012A
- dsPIC30F6013A
- dsPIC30F6014A

dsPIC30F601XA Rev. A2 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 within the MPLAB IDE. The following text is then visible under the MPLAB ICD 2 section in the output window within MPLAB IDE:

```
MPLAB ICD 2 Ready
Connecting to MPLAB ICD 2
...Connected
Setting Vdd source to target
Target Device dsPIC30F6014A found,
revision = Rev 0x1002
...Reading ICD Product ID
Running ICD Self Test
...Passed
MPLAB ICD 2 Ready".
```

The errata described in this section will be fixed in future revisions of dsPIC30F6011A, dsPIC30F6012A, dsPIC30F6013A and dsPIC30F6014A silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. MAC Class Instruction with ±4 Address Modification

   Sequential MAC instructions, which prefetch data from Y data space using ±4 address modification will cause an address error trap.

2. Decimal Adjust Instruction

   The Decimal Adjust instruction, `DAW.b`, may improperly clear the Carry bit, C (SR<0>).

3. `DISI` Instruction

   The `DISI` instruction will not disable interrupts if a `DISI` instruction is executed in the same instruction cycle that the `DISI` counter decrements to zero.

4. Output Compare Module in PWM Mode

   Output compare will produce a glitch when loading 0% duty cycle in PWM mode. It will also miss the next compare after the glitch.

5. Output Compare

   The output compare module will produce a glitch on the output when an I/O pin is initially set high and the module is configured to drive the pin low at a specified time.

6. Using OSC2/RC15 as Digital I/O or CLKOUT

   For this revision of silicon, pin OSC2/RC15 is operational for digital I/O and CLKOUT only in specific oscillator modes.

7. LP Oscillator

   For this revision of silicon, the LP Oscillator is not operational.

8. INT0, ADC and Sleep Mode

   ADC event triggers from the INT0 pin will not wake-up the device from Sleep mode if the SMPI bits are non-zero.

9. 4x and 8x PLL Mode

   If 4x or 8x PLL mode is used, the input frequency range is 5 MHz-10 MHz instead of 4 MHz-10 MHz.

The following sections will describe the errata and work around to these errata, where they may apply.

1. Module: MAC Class Instructions with ±4 Address Modifications

Sequential MAC class instructions, which prefetch data from Y data space using ±4 address modification, will cause an address error trap. The trap occurs only when all of the following conditions are true:

1. Two sequential MAC class instructions (or a MAC class instruction executed in a REPEAT or DO loop) that prefetch from Y data space.
2. Both instructions prefetch data from Y data space using the + = 4 or – = 4 address modification.
3. Neither instruction uses an accumulator write-back.

Work around

The problem described above can be avoided by using any of the following methods:

1. Inserting any other instruction between the two MAC class instructions.
2. Adding an accumulator write-back (a dummy write-back if needed) to either of the MAC class instructions.
3. Do not use the + = 4 or – = 4 address modification.
4. Do not prefetch data from Y data space.

2. Module: CPU – DAW.b Instruction

The Decimal Adjust instruction, DAW.b, may improperly clear the Carry bit, C (SR<0>), when executed.

Work around

Check the state of the Carry bit prior to executing the DAW.b instruction. If the Carry bit is set, set the Carry bit again after executing the DAW.b instruction. Example 1 shows how the application should process the Carry bit during a BCD addition operation.

EXAMPLE 1: CHECK CARRY BIT BEFORE DAW.b

```
    .include "p30fxxxx.inc"
    .......
    mov.b   #0x80, w0   ;First BCD number
    mov.b   #0x80, w1   ;Second BCD number
    add.b   w0, w1, w2  ;Perform addition
    bra     NC, L0      ;If C set go to L0
    daw.b   w2          ;If not,do DAW and
    bset.b  SR, #C      ;set the carry bit
    bra     L1          ;and exit
L0:daw.b    w2
L1: ....
```

3. Module: DISI Instruction

When a user executes a DISI #7, for example, this will disable interrupts for 7 + 1 cycles (7 + the DISI instruction itself). In this case, the DISI instruction uses a counter which counts down from 7 to 0. The counter is loaded with 7 at the end of the DISI instruction.

If the user code executes another DISI on the instruction cycle where the DISI counter has become zero, the new DISI count is loaded, but the DISI state machine does not properly re-engage and continue to disable interrupts. At this point, all interrupts are enabled. The next time the suer code executes a DISI instruction, the feature will act normally and block interrupts.

In summary, it is only when a DISI execution is coincident with the current DISI count = 0, that the issue occurs. Executing a DISI instruction before the DISI counter reaches zero will not produce this error. In this case, the DISI counter is loaded with the new value, and interrupts remain disabled until the counter becomes zero.

Work around

When executing multiple DISI instructions within the source code, make sure that subsequent DISI instructions have at least one instruction cycle between the time that the DISI counter decrements to zero and the next DISI instruction. Alternatively, make sure that subsequent DISI instructions are called before the DISI counter decrements to zero.

4. Module: Output Compare in PWM Mode

If the desired duty cycle is '0' (OCxRS = 0), the module will generate a high level glitch of 1 TCY. the second problem is that on the next cycle after the glitch, the OC pin does not go high, or, in other words, it misses the next compare for any value written on OCxRS.

Work around

There are two possible solutions to this problem:

1. Load a value greater than '0' to the OCxRS register when operating in PWM mode. In this case, no 0% duty cycle is achievable.
2. If the application requires 0% duty cycles, the output compare module can be disabled for 0% duty cycles, and re-enabled for non-zero percent duty cycles.

5. Module: Output Compare

A glitch will be produced on an output compare pin under the following conditions:

- The user software initially drives the I/O pin high using the output compare module or a write to the associated PORT register.
- The output compare module is configured and enabled to drive the pin low at some later time (OCxCON = 0x0002 or OCxCON = 0x0003).

When these events occur, the output compare module will drive the pin low for one instruction cycle (T_{CY}) after the module is enabled.

Work around

None. However, the user may use a timer interrupt and write to the associated PORT register to control the pin manually.

6. Module: Using OSC2/RC15 as Digital I/O or CLKOUT

Table 20-2 (see below) from the "dsPIC30F6011A/6012A/6013A/6014A Data Sheet" (DS70143A) lists the device clock operational modes. The data in the table is correct with the following exceptions:

- Digital I/O functionality is not operational in the FRC with PLL (4x, 8x and 16x PLL) Oscillator mode.
- CLKOUT functionality is only supported if the EC or ERC Oscillator mode is actually selected as the device clock source.

TABLE 20-2: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	FOS<2:0>			FPR<4:0>					OSC2 Function
ECIO w/ PLL 4x	PLL	1	1	1	0	1	1	0	1	I/O
ECIO w/ PLL 8x	PLL	1	1	1	0	1	1	1	0	I/O
ECIO w/ PLL 16x	PLL	1	1	1	0	1	1	1	1	I/O
FRC w/ PLL 4x	PLL	1	1	1	0	0	0	0	1	I/O
FRC w/ PLL 8x	PLL	1	1	1	0	1	0	1	0	I/O
FRC w/ PLL 16x	PLL	1	1	1	0	0	0	1	1	I/O
XT w/ PLL 4x	PLL	1	1	1	0	0	1	0	1	OSC2
XT w/ PLL 8x	PLL	1	1	1	0	0	1	1	0	OSC2
XT w/ PLL 16x	PLL	1	1	1	0	0	1	1	1	OSC2
HS2 w/ PLL 4x	PLL	1	1	1	1	0	0	0	1	OSC2
HS2 w/ PLL 8x	PLL	1	1	1	1	0	0	1	0	OSC2
HS2 w/ PLL 16x	PLL	1	1	1	1	0	0	1	1	OSC2
HS3 w/ PLL 4x	PLL	1	1	1	1	0	1	0	1	OSC2
HS3 w/ PLL 8x	PLL	1	1	1	1	0	1	1	0	OSC2
HS3 w/ PLL 16x	PLL	1	1	1	1	0	1	1	1	OSC2
ECIO	External	0	1	1	0	1	1	0	0	I/O
XT	External	0	1	1	0	0	1	0	0	OSC2
HS	External	0	1	1	0	0	0	1	0	OSC2
EC	External	0	1	1	0	1	0	1	1	CLKOUT
ERC	External	0	1	1	0	1	0	0	1	CLKOUT
ERCIO	External	0	1	1	0	1	0	0	0	I/O
XTL	External	0	1	1	0	0	0	0	0	OSC2
LP	Secondary	0	0	0	x	x	x	x	x	**(Note 1, 2)**
FRC	Internal FRC	0	0	1	x	x	x	x	x	**(Note 1, 2)**
LPRC	Internal LPRC	0	1	0	x	x	x	x	x	**(Note 1, 2)**

Note 1: OSC2 pin function is determined by FPR<4:0>.

2: OSC1 pin cannot be used as an I/O pin even if the secondary oscillator or an internal clock source is selected at all times.

Work around

None. In future revisions of silicon, port pin RC15 may also be configured for Digital I/O and CLKOUT for additional oscillator modes.

7. Module: LP Oscillator

The 32 kHz LP Oscillator module is not operational for this version of silicon.

8. Module: INT0, ADC and Sleep Mode

ADC event triggers from the INT0 pin will not wake-up the device from Sleep mode if the SMPI bits are non-zero. This means that if the ADC is configured to generate an interrupt after a certain number of INT0 triggered conversions, the ADC conversions will not be triggered and the device will remain in Sleep. The ADC will perform conversions and wake-up the device only if it is configured to generate an interrupt after each INT0 triggered conversion (SMPI<3:0> = 0000).

Work around

None. If ADC event trigger from the INT0 pin is required, initialize SMPI<3:0> to '0000' (interrupt on every conversion).

9. Module: 4x and 8x PLL Mode

If 4x or 8x PLL mode is used, the input frequency range is 5 MHz-10 MHz instead of 4 MHz-10 MHz.

Work around

None. If 4x or 8x PLL is used, make sure the input crystal or clock frequency is 5 MHz or greater.

APPENDIX A: REVISION HISTORY

Revision A (7/2005)

Original version of the document marked as Confidential.

Revision B (8/2005)

Revision C (9/2006)

Added errata #1, #3, #4, #5, #8, #9.

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