MICROCHIP PIC18F2221/2321/4221/4321

PIC18F2221/2321/4221/4321 Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39689**E**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2221/2321/4221/4321 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

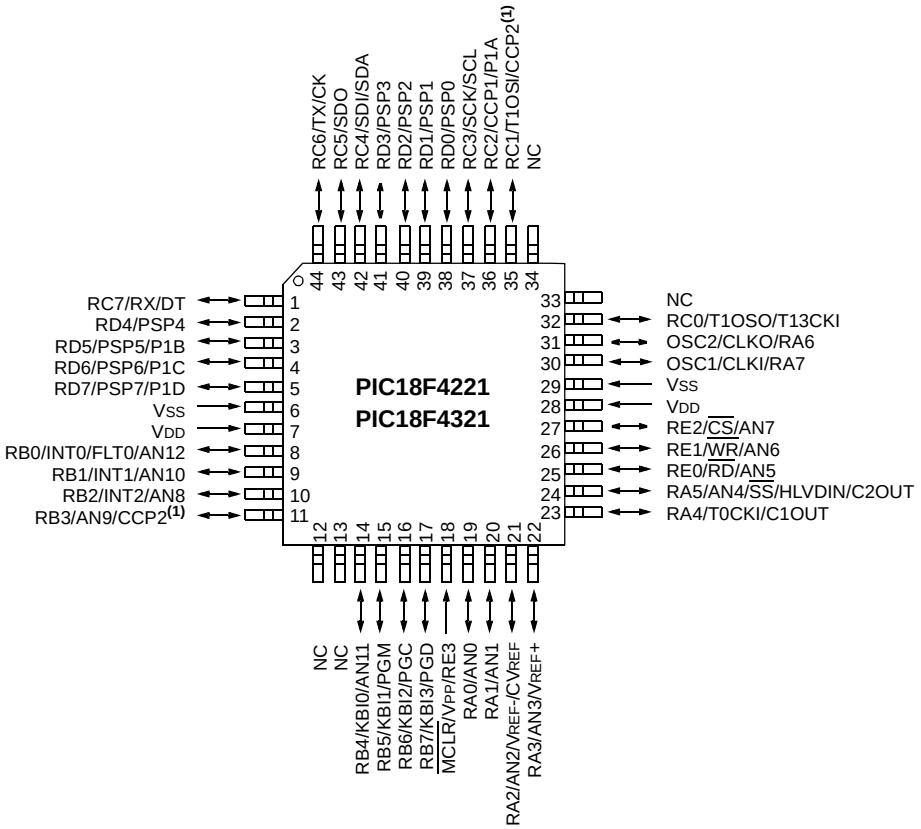
1. Module: Pin Diagrams

The pin diagram for the 44-pin TQFP package, on Page 4, has been modified to change the designation for Pins 12, 13, 33 and 34 to “NC”, No Connect.

Additionally, the diagram’s second note – concerning “Special ICPORT features” – has been removed, such that the diagram appears as shown below.

Pin Diagrams (Continued)

44-Pin TQFP



Note 1: RB3 is the alternate pin for CCP2 multiplexing.

2. Module: PIC18F4221/4321 Pinout I/O Descriptions Table

Table 1-3: PIC18F4221/4321 Pinout I/O Descriptions, beginning on Page 16, has been changed to remove Note 3, concerning “Special ICPORT features.”

3. Module: PIC18F4221/4321 Pinout I/O Descriptions Table

Table 1-3: PIC18F4221/4321 Pinout I/O Descriptions, beginning on Page 16, has been changed to remove four rows.

With Data Sheet Clarifications 2 and 3, the table now appears as shown.

TABLE 1-3: PIC18F4221/4321 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
$\overline{MCLR}$/VPP/RE3	1	18	18			Master Clear (input) or programming voltage (input).
$\overline{MCLR}$				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				P		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI/RA7	13	32	30			Oscillator crystal or external clock input.
OSC1				I	Analog	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; analog otherwise.
CLKI				I	Analog	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7				I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	14	33	31			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC, EC and INTIO modes, OSC2 pin outputs CLKO which has one-fourth the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; I^2C = ST with I^2C™ or SMB levels; O = Output

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4221/4321 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Comparator reference voltage output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RA5/AN4/$\overline{SS}$/HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
$\overline{SS}$				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6						See the OSC2/CLKO/RA6 pin.
RA7						See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; I^2C = ST with I^2C™ or SMB levels; O = Output

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4221/4321 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0/FLT0/AN12	33	9	8			
RB0				I/O	TTL	Digital I/O.
INT0				I	ST	External interrupt 0.
FLT0				I	ST	PWM Fault input for Enhanced CCP1.
AN12				I	Analog	Analog input 12.
RB1/INT1/AN10	34	10	9			
RB1				I/O	TTL	Digital I/O.
INT1				I	ST	External interrupt 1.
AN10				I	Analog	Analog input 10.
RB2/INT2/AN8	35	11	10			
RB2				I/O	TTL	Digital I/O.
INT2				I	ST	External interrupt 2.
AN8				I	Analog	Analog input 8.
RB3/AN9/CCP2	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog input 9.
CCP2(2)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
RB4/KBI0/AN11	37	14	14			
RB4				I/O	TTL	Digital I/O.
KBI0				I	TTL	Interrupt-on-change pin.
AN11				I	Analog	Analog input 11.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; I^2C = ST with I^2C™ or SMB levels; O = Output

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4221/4321 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator analog output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator analog input.
CCP2(1)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
P1A				O	—	Enhanced CCP1 output.
RC3/SCK/SCL	18	37	37			
RC3				I/O	ST	Digital I/O.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	I^2C	Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI/SDA	23	42	42			
RC4				I/O	ST	Digital I/O.
SDI				I	ST	SPI data in.
SDA				I/O	I^2C	I^2C data I/O.
RC5/SDO	24	43	43			
RC5				I/O	ST	Digital I/O.
SDO				O	—	SPI data out.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see related RX/DT).
RC7/RX/DT	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see related TX/CK).

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; I^2C = ST with I^2C™ or SMB levels; O = Output

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4221/4321 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled.
RD0/PSP0	19	38	38			
RD0				I/O	ST	Digital I/O.
PSP0				I/O	TTL	Parallel Slave Port data.
RD1/PSP1	20	39	39			
RD1				I/O	ST	Digital I/O.
PSP1				I/O	TTL	Parallel Slave Port data.
RD2/PSP2	21	40	40			
RD2				I/O	ST	Digital I/O.
PSP2				I/O	TTL	Parallel Slave Port data.
RD3/PSP3	22	41	41			
RD3				I/O	ST	Digital I/O.
PSP3				I/O	TTL	Parallel Slave Port data.
RD4/PSP4	27	2	2			
RD4				I/O	ST	Digital I/O.
PSP4				I/O	TTL	Parallel Slave Port data.
RD5/PSP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
PSP5				I/O	TTL	Parallel Slave Port data.
P1B				O	—	Enhanced CCP1 output.
RD6/PSP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
PSP6				I/O	TTL	Parallel Slave Port data.
P1C				O	—	Enhanced CCP1 output.
RD7/PSP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
PSP7				I/O	TTL	Parallel Slave Port data.
P1D				O	—	Enhanced CCP1 output.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels I = Input P = Power
I^2C = ST with I^2C™ or SMB levels O = Output

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F4221/4321 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/$\overline{RD}$/AN5	8	25	25			
RE0				I/O	ST	Digital I/O.
$\overline{RD}$				I	TTL	Read control for Parallel Slave Port (see also $\overline{WR}$ and $\overline{CS}$ pins).
AN5				I	Analog	Analog input 5.
RE1/$\overline{WR}$/AN6	9	26	26			
RE1				I/O	ST	Digital I/O.
$\overline{WR}$				I	TTL	Write control for Parallel Slave Port (see $\overline{CS}$ and $\overline{RD}$ pins).
AN6				I	Analog	Analog input 6.
RE2/$\overline{CS}$/AN7	10	27	27			
RE2				I/O	ST	Digital I/O.
$\overline{CS}$				I	TTL	Chip Select control for Parallel Slave Port (see related $\overline{RD}$ and $\overline{WR}$).
AN7				I	Analog	Analog input 7.
RE3	—	—	—	—	—	See $\overline{MCLR}$/V_{PP}/RE3 pin.
V_{SS}	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
V_{DD}	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
NC	—	13	12,13, 33, 34	—	—	No Connect.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; I^2C = ST with I^2C™ or SMB levels; O = Output

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

4. Module: Configuration Bits and Device IDs

Table 23-1: Configuration Bits and Device IDs, on Page 253, has been changed to designate Bit 3 of CONFIG4L as unimplemented.

The table is changed as shown.

TABLE 23-1: CONFIGURATION BITS AND DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	00-- 0111
300002h	CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	$\overline{\text{PWRTEN}}$	---1 1111
300003h	CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	---1 1111
300005h	CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX	1--- -011
300006h	CONFIG4L	$\overline{\text{DEBUG}}$	XINST	BBSIZ1	BBSIZ0	—	LVP	—	STVREN	1000 -1-1
300008h	CONFIG5L	—	—	—	—	—	—	CP1	CP0	---- --11
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	—	—	—	—	—	—	WRT1	WRT0	---- --11
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	—	—	—	—	—	—	EBTR1	EBTR0	---- --11
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1(1)	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx(2)
3FFFFFh	DEVID2(1)	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 1100

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition.
Shaded cells are unimplemented, read as '0'.

Note 1: Unimplemented in PIC18F2221/4221 devices; maintain these bits set.

2: See Register 23-14 for DEVID1 values. DEVID registers are read-only and cannot be programmed by the user.

5. Module: CONFIG4L Register

Register 23-5: CONFIG4L: Configuration Register 4 Low (Byte Address 300006h), on Page 258, has been changed to designate Bit 3 of CONFIG4L as unimplemented.

The register is changed as shown.

REGISTER 23-5: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)

R/P-1	R/P-0	U-0	U-0	U-0	R/P-1	U-0	R/P-1
$\overline{\text{DEBUG}}$	XINST	BBSIZ1	BBSIZ0	—	LVP	—	STVREN
bit 7							bit 0

bit 7 **$\overline{\text{DEBUG}}$:** Background Debugger Enable bit
1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins
0 = Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug

bit 6 **XINST:** Extended Instruction Set Enable bit
1 = Instruction set extension and Indexed Addressing mode enabled
0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)

bit 5-4 **BBSIZ1:BBSIZ0:** Boot Block Size Select bits

PIC18F4221/4321 Devices:
1x = 1024 Words
01 = 512 Words
00 = 256 Words

PIC18F2221/2321 Devices:
1x = 512 Words
x1 = 512 Words
00 = 256 Words

bit 3 **Unimplemented:** Read as '0'

bit 2 **LVP:** Single-Supply ICSP™ Enable bit
1 = Single-Supply ICSP enabled
0 = Single-Supply ICSP disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **STVREN:** Stack Full/Underflow Reset Enable bit
1 = Stack full/underflow will cause Reset
0 = Stack full/underflow will not cause Reset

Legend:		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

6. Module: "Special ICPORT Features" Section

Section 23.9 "Special ICPORT Features (44-Pin TQFP Packages Only)" has been removed. That section includes Table 23-5: Equivalent Pins for Legacy and Dedicated ICD/ICSP™ Ports, **Section 23.9.1 "Dedicated ICD/ICSP Port"** and **Section 23.9.2 "28-Pin Emulation**" on Pages 271 and 272.

7. Module: Index Deletions

Because of the content deleted by Data Sheet Clarifications 1 through 6, the following items are removed from the index:

- ICCK
- ICDT
- ICPORTS
- ICVPP
- ICRST
- Special ICPORT Features

8. Module: Product Identification System

The "PIC18F2221/2321/4221/4321 Product Identification System" illustration, on Page 393, is changed to correct the following inaccuracies:

- Tape and reel delivery is available for TQFP, SOIC, SSOP and QFN packages — *not* only for TQFP packages, as stated
- The part number code for QFN packages is "ML" — *not* "MM," as stated.

The illustration is changed, as shown, with bold text indicating the corrected information.

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PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC18F2221/2321(1), PIC18F4221/4321(1), PIC18F2221/2321T(2), PIC18F4221/4321T(2); VDD range 4.2V to 5.5V PIC18LF2221/2321(1), PIC18LF4221/4321(1), PIC18LF2221/2321T(2), PIC18LF4221/4321T(2); VDD range 2.0V to 5.5V
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SS = SSOP SP = Skinny Plastic DIP P = PDIP **ML = QFN**
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18F4321-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.

b) PIC18LF2321-I/SO = Industrial temp., SOIC package, Extended VDD limits.

c) PIC18LF4321-I/P = Industrial temp., PDIP package, normal VDD limits.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range
2: T = In tape and reel for TQFP, **SOIC**, **SSOP and QFN** packages.

9. Module: EUSART

The descriptions of the RXDTP and TXCKP bits (BAUDCON<5:4>) are being revised as shown below (changes in **bold**).

In this document's Revision E change, the Synchronous mode content was removed from the bit 5 (RXDTP) description.

REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER (EXCERPT)

R/W-0	R-1	**R/W-0**	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 5 **RXDTP: Data/Receive Polarity Select bit (Asynchronous mode only)**

Asynchronous mode:
1 = Receive data (RX) is inverted (active-low)
0 = Receive data (RX) is not inverted (active-high)

bit 4 **TXCKP: Clock and Data Polarity Select bit**

Asynchronous mode:
1 = Idle state for transmit (TX) is a low level
0 = Idle state for transmit (TX) is a high level

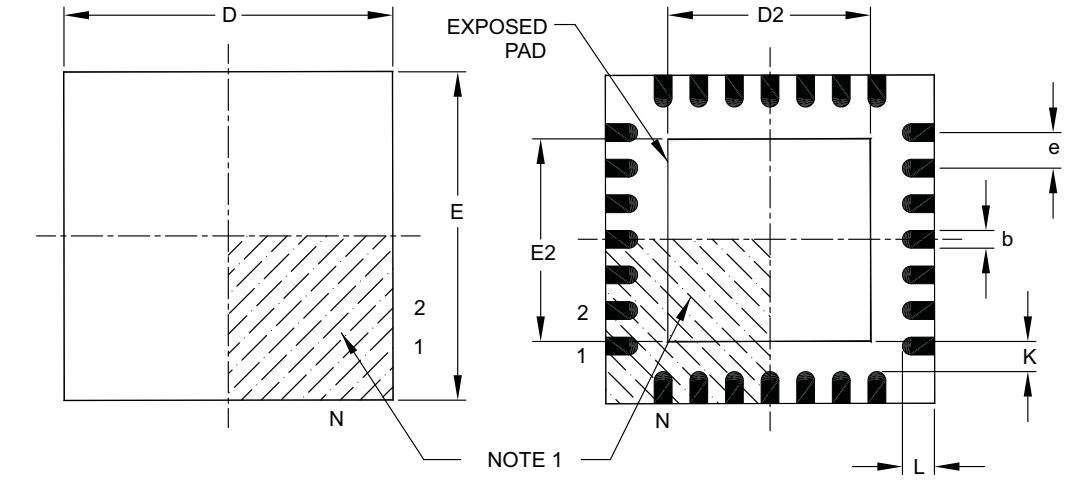
Synchronous mode:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

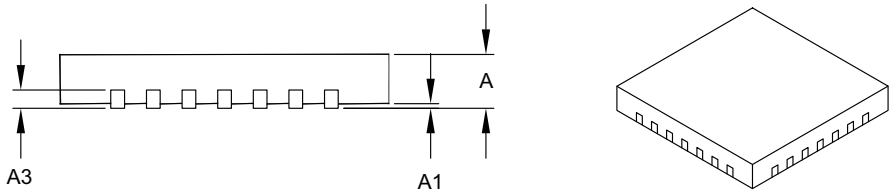
10. Module: Packaging Information

The 28-Lead Plastic Quad Flat, No Lead Package (MM) illustration, on page 371, is replaced by the one shown.

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

11. Module: Electrical Characteristics

The Supply Voltage, Power-Down and Supply Current, and High/Low-Voltage Detect Characteristics tables are updated as shown. The three tables are reprinted in their entirety, with the updated values indicated by bold text.

26.1 DC Characteristics: Supply Voltage PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial)

PIC18LF2221/2321/4221/4321 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2221/2321/4221/4321 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**					
		PIC18LF2X21/4X21	2.0	—	5.5	V	HS, XT, RC and LP Oscillator mode
		PIC18FXXXX	4.2	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	—	0.7	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details
	VBOR	**Brown-out Reset Voltage**					
D005		PIC18LF2X21/4X21					
		BORV1:BORV0 = 11	2.00	**2.11**	**2.22**	V	
		BORV1:BORV0 = 10	2.65	2.79	2.93	V	
D005		All devices					
		BORV1:BORV0 = 01(2)	4.11	4.33	4.55	V	
		BORV1:BORV0 = 00	4.36	4.59	4.82	V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: With BOR enabled, full-speed operation (FOSC = 40 MHz) is supported until a BOR occurs. This is valid although VDD may be below the minimum voltage for this frequency.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**	
	Power-Down Current (IPD)(1)					
	PIC18LF2X21/4X21	0.5	0.7	µA	-40°C	VDD = 2.0V (**Sleep** mode)
		0.5	0.7	µA	+25°C	
		0.5	1.7	µA	+85°C	
	PIC18LF2X21/4X21	0.6	0.9	µA	-40°C	VDD = 3.0V (**Sleep** mode)
		0.6	0.9	µA	+25°C	
		0.6	1.9	µA	+85°C	
	All devices	0.9	2.0	µA	-40°C	VDD = 5.0V (**Sleep** mode)
		0.9	2.0	µA	+25°C	
		0.9	6.5	µA	+85°C	
	Extended devices only	7.5	70	µA	+125°C	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2)						
	PIC18LF2X21/4X21	13	**19**	µA	-40°C	VDD = 2.0V	FOSC = 31 kHz (**RC_RUN** mode, INTRC source)
		13	**19**	µA	+25°C		
		13	**17**	µA	+85°C		
	PIC18LF2X21/4X21	41	45	µA	-40°C	VDD = 3.0V	
		34	**38**	µA	+25°C		
		27	30	µA	+85°C		
	All devices	104	115	µA	-40°C	VDD = 5.0V	
		86	95	µA	+25°C		
		67	75	µA	+85°C		
	Extended devices only	68	**100**	µA	+125°C		
	PIC18LF2X21/4X21	0.31	0.35	mA	-40°C	VDD = 2.0V	FOSC = 1 MHz (**RC_RUN** mode, INTOSC source)
		0.31	0.35	mA	+25°C		
		0.31	0.35	mA	+85°C		
	PIC18LF2X21/4X21	0.55	0.60	mA	-40°C	VDD = 3.0V	
		0.51	0.60	mA	+25°C		
		0.47	0.60	mA	+85°C		
	All devices	1.0	**1.3**	mA	-40°C	VDD = 5.0V	
		0.94	**1.3**	mA	+25°C		
		0.88	**1.2**	mA	+85°C		
	Extended devices only	0.88	**1.2**	mA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2)						
	PIC18LF2X21/4X21	0.69	**0.9**	mA	-40°C	VDD = 2.0V	FOSC = 4 MHz (**RC_RUN** mode, INTOSC source)
		0.70	**0.9**	mA	+25°C		
		0.71	**0.9**	mA	+85°C		
	PIC18LF2X21/4X21	1.17	**1.45**	mA	-40°C	VDD = 3.0V	
		1.15	**1.45**	mA	+25°C		
		1.14	**1.45**	mA	+85°C		
	All devices	2.24	**2.9**	mA	-40°C	VDD = 5.0V	
		2.20	**2.9**	mA	+25°C		
		2.16	**2.8**	mA	+85°C		
	Extended devices only	2.18	**2.8**	mA	+125°C		
	PIC18LF2X21/4X21	3	5	µA	-40°C	VDD = 2.0V	FOSC = 31 kHz (**RC_IDLE** mode, INTRC source)
		3	5	µA	+25°C		
		3	**5.6**	µA	+85°C		
	PIC18LF2X21/4X21	4	**7**	µA	-40°C	VDD = 3.0V	
		5	7	µA	+25°C		
		5	**10**	µA	+85°C		
	All devices	10	12	µA	-40°C	VDD = 5.0V	
		10	12	µA	+25°C		
		10	**16**	µA	+85°C		
	Extended devices only	17	**50**	µA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2)						
	PIC18LF2X21/4X21	**160**	**230**	µA	-40°C	VDD = 2.0V	FOSC = 1 MHz (**RC_IDLE** mode, INTOSC source)
		170	**230**	µA	+25°C		
		170	**230**	µA	+85°C		
	PIC18LF2X21/4X21	220	**330**	µA	-40°C	VDD = 3.0V	
		240	**330**	µA	+25°C		
		250	**330**	µA	+85°C		
	All devices	410	**500**	µA	-40°C	VDD = 5.0V	
		420	**500**	µA	+25°C		
		430	**500**	µA	+85°C		
	Extended devices only	450	**500**	µA	+125°C		
	PIC18LF2X21/4X21	310	**440**	µA	-40°C	VDD = 2.0V	FOSC = 4 MHz (**RC_IDLE** mode, INTOSC source)
		330	**440**	µA	+25°C		
		340	**440**	µA	+85°C		
	PIC18LF2X21/4X21	480	750	µA	-40°C	VDD = 3.0V	
		500	750	µA	+25°C		
		520	750	µA	+85°C		
	All devices	0.91	**1.3**	mA	-40°C	VDD = 5.0V	
		0.93	**1.3**	mA	+25°C		
		0.96	**1.3**	mA	+85°C		
	Extended devices only	0.98	**1.3**	mA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2)						
	PIC18LF2X21/4X21	0.22	**0.35**	mA	-40°C	VDD = 2.0V	FOSC = 1 MHz (**PRI_RUN**, EC oscillator)
		0.22	**0.35**	mA	+25°C		
		0.21	**0.3**	mA	+85°C		
	PIC18LF2X21/4X21	0.51	0.55	mA	-40°C	VDD = 3.0V	
		0.45	0.50	mA	+25°C		
		0.39	0.45	mA	+85°C		
	All devices	1.14	**1.15**	mA	-40°C	VDD = 5.0V	
		0.99	**1.1**	mA	+25°C		
		0.83	**1.1**	mA	+85°C		
	Extended devices only	0.80	**1.1**	mA	+125°C		
	PIC18LF2X21/4X21	610	**870**	µA	-40°C	VDD = 2.0V	FOSC = 4 MHz (**PRI_RUN**, EC oscillator)
		610	**870**	µA	+25°C		
		610	**870**	µA	+85°C		
	PIC18LF2X21/4X21	**1.16**	**1.83**	mA	-40°C	VDD = 3.0V	
		1.10	**1.83**	mA	+25°C		
		1.07	**1.83**	mA	+85°C		
	All devices	2.35	**2.85**	mA	-40°C	VDD = 5.0V	
		2.24	**2.85**	mA	+25°C		
		2.14	**2.85**	mA	+85°C		
	Extended devices only	2.14	**2.85**	mA	+125°C		
	Extended devices only	9	15	mA	+125°C	VDD = 4.2V	FOSC = 25 MHz (**PRI_RUN**, EC oscillator)
		12	20	mA	+125°C	VDD = 5.0V	
	All devices	**16**	**19**	mA	-40°C	VDD = 4.2V	FOSC = 40 MHz (**PRI_RUN**, EC oscillator)
		14	**19**	mA	+25°C		
		14	**19**	mA	+85°C		
	All devices	17	**22.7**	mA	-40°C	VDD = 5.0V	
		17	**22.7**	mA	+25°C		
		17	**22.7**	mA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2)						
	All devices	**7**	**10**	mA	-40°C	VDD = 4.2V	FOSC = 4 MHz, 16 MHz internal (**PRI_RUN HS+PLL**)
		6	**10**	mA	+25°C		
		6	**10**	mA	+85°C		
	Extended devices only	**6**	**10**	mA	+125°C		
	All devices	10	**12**	mA	-40°C	VDD = 5.0V	FOSC = 4 MHz, 16 MHz internal (**PRI_RUN HS+PLL**)
		9	**12**	mA	+25°C		
		9	**12**	mA	+85°C		
	Extended devices only	**9**	**12**	mA	+125°C		
	All devices	17	**19**	mA	-40°C	VDD = 4.2V	FOSC = 10 MHz, 40 MHz internal (**PRI_RUN HS+PLL**)
		15	**19**	mA	+25°C		
		15	**19**	mA	+85°C		
	All devices	**18**	**23**	mA	-40°C	VDD = 5.0V	FOSC = 10 MHz, 40 MHz internal (**PRI_RUN HS+PLL**)
		18	**23**	mA	+25°C		
		18	**23**	mA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2)						
	PIC18LF2X21/4X21	51	**75**	µA	-40°C	VDD = 2.0V	FOSC = 1 MHz (**PRI_IDLE** mode, EC oscillator)
		54	**75**	µA	+25°C		
		60	**75**	µA	+85°C		
	PIC18LF2X21/4X21	83	**123**	µA	-40°C	VDD = 3.0V	
		88	**123**	µA	+25°C		
		93	**123**	µA	+85°C		
	All devices	180	**260**	µA	-40°C	VDD = 5.0V	
		180	**260**	µA	+25°C		
		180	**260**	µA	+85°C		
	Extended devices only	190	**260**	µA	+125°C		
	PIC18LF2X21/4X21	210	**290**	µA	-40°C	VDD = 2.0V	FOSC = 4 MHz (**PRI_IDLE** mode, EC oscillator)
		220	**290**	µA	+25°C		
		230	**290**	µA	+85°C		
	PIC18LF2X21/4X21	350	**480**	µA	-40°C	VDD = 3.0V	
		360	**480**	µA	+25°C		
		370	**480**	µA	+85°C		
	All devices	0.69	**1**	mA	-40°C	VDD = 5.0V	
		0.70	**1**	mA	+25°C		
		0.72	**1**	mA	+85°C		
	Extended devices only	0.74	**1**	mA	+125°C		
	Extended devices only	3.7	4.0	mA	+125°C	VDD = 4.2V	FOSC = 25 MHz (**PRI_IDLE** mode, EC oscillator)
		4.6	5.0	mA	+125°C	VDD = 5.0V	
	All devices	6.0	**7.3**	mA	-40°C	VDD = 4.2V	FOSC = 40 MHz (**PRI_IDLE** mode, EC oscillator)
		6.2	**7.3**	mA	+25°C		
		6.6	**7.3**	mA	+85°C		
	All devices	6.8	**9.2**	mA	-40°C	VDD = 5.0V	
		7.0	**9.2**	mA	+25°C		
		7.1	**9.2**	mA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC18F2221/2321/4221/4321 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD)(2)						
	PIC18LF2X21/4X21	12	**19**	µA	-40°C(5)	VDD = 2.0V	FOSC = 32 kHz(3) (**SEC_RUN** mode, Timer1 as clock)(3)
		—	**19**	µA	-10°C		
		13	**19**	µA	+25°C		
		13	**19**	µA	+85°C		
	PIC18LF2X21/4X21	40	45	µA	-40°C(5)	VDD = 3.0V	
		—	**45**	µA	-10°C		
		33	45	µA	+25°C		
		27	45	µA	+85°C		
	All devices	101	115	µA	-40°C(5)	VDD = 5.0V	
		—	**110**	µA	-10°C		
		83	**110**	µA	+25°C		
		65	**88**	µA	+85°C		
	PIC18LF2X21/4X21	2.5	**5**	µA	-40°C(5)	VDD = 2.0V	FOSC = 32 kHz(3) (**SEC_IDLE** mode, Timer1 as clock)(3)
		—	**5**	µA	-10°C		
		3.0	**5**	µA	+25°C		
		3.5	**8**	µA	+85°C		
	PIC18LF2X21/4X21	3.9	**7**	µA	-40°C(5)	VDD = 3.0V	
		—	**7**	µA	-10°C		
		4.5	**7**	µA	+25°C		
		5.2	**10.7**	µA	+85°C		
	All devices	7.5	**10**	µA	-40°C(5)	VDD = 5.0V	
		—	**10**	µA	-10°C		
		8.0	**10**	µA	+25°C		
		8.6	**15**	µA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Module Differential Currents (ΔIWDT, ΔIBOR, ΔILVD, ΔIOSCB, ΔIAD)						
D022 (ΔIWDT)	**Watchdog Timer**	1.6	**2.5**	µA	-40°C	VDD = 2.0V	
		1.6	**2.5**	µA	+25°C		
		1.5	**2.5**	µA	+85°C		
		2.3	**3.5**	µA	-40°C	VDD = 3.0V	
		2.2	**3.5**	µA	+25°C		
		2.1	**3**	µA	+85°C		
		3.4	**7.4**	µA	-40°C	VDD = 5.0V	
		3.9	**7.4**	µA	+25°C		
		4.4	**7.4**	µA	+85°C		
		4.5	**7.4**	µA	+125°C		
D022A (ΔIBOR)	**Brown-out Reset(4)**	34	45	µA	-40°C to +85°C	VDD = 3.0V	
		40	**62.6**	µA	-40°C to +85°C	VDD = 5.0V	
		42	**62.6**	µA	-40°C to +125°C		
		0	**2**	µA	-40°C to +85°C	VDD = 3.0V	SLEEP Mode BOREN1:BOREN0 = 10
		0	**5**	µA	-40°C to +125°C	VDD = 5.0V	
D022B (ΔILVD)	**High/Low-Voltage Detect(4)**	23	35	µA	-40°C to +85°C	VDD = 2.0V	
		23	35	µA	-40°C to +85°C	VDD = 3.0V	
		28	35	µA	-40°C to +85°C	VDD = 5.0V	
		30	40	µA	-40°C to +125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC18F2221/2321/4221/4321 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Typ	Max	Units	Conditions		
D025 (ΔIOSCB)	**Timer1 Oscillator**	2.1	4.5	µA	-40°C(5)	VDD = 2.0V	32 kHz Tuning Fork Crystal on Timer1 Oscillator(3)
		—	**4.5**	µA	-10°C		
		1.8	4.5	µA	+25°C		
		2.1	4.5	µA	+85°C		
		2.2	6.0	µA	-40°C(5)	VDD = 3.0V	
		—	**6**	µA	-10°C		
		2.6	6.0	µA	+25°C		
		2.9	6.0	µA	+85°C		
		3.0	8.0	µA	-40°C(5)	VDD = 5.0V	
		—	**8**	µA	-10°C		
		3.2	8.0	µA	+25°C		
		3.4	8.0	µA	+85°C		
D026 (ΔIAD)	**A/D Converter**	1.0	2.0	µA	-40°C to +85°C	VDD = 2.0V	A/D on, not converting
		1.0	2.0	µA	-40°C to +85°C	VDD = 3.0V	
		1.0	2.0	µA	-40°C to +85°C	VDD = 5.0V	
		2.0	8.0	µA	-40°C to +125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;
MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC high-power mode where LPT1OSC (CONFIG3H<2>) = 0.

TABLE 26-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
D420		HLVD Voltage on VDD Transition High to Low	LVV = 0000	2.06	2.17	2.28	V	
			LVV = 0001	2.12	2.23	2.34	V	
			LVV = 0010	2.24	2.36	2.48	V	
			LVV = 0011	2.32	2.44	2.56	V	
			LVV = 0100	2.47	2.60	2.73	V	
			LVV = 0101	2.65	2.79	2.93	V	
			LVV = 0110	2.74	2.89	3.04	V	
			LVV = 0111	2.96	3.12	3.28	V	
			LVV = 1000	3.22	3.39	3.56	V	
			LVV = 1001	3.37	3.55	3.73	V	
			LVV = 1010	3.52	3.71	3.90	V	
			LVV = 1011	3.70	3.90	4.10	V	
			LVV = 1100	3.90	4.11	4.32	V	
			LVV = 1101	4.11	4.33	4.55	V	
			LVV = 1110	4.36	4.59	4.82	V	
			LVV = 1111	1.10	1.20	1.30	V	HLVDIN input/internal reference voltage

12. Module: Electrical Characteristics (I/O Port Leakage Current)

The maximum values of the following parameters for input leakage current are changed:

- D060 – I/O Ports
- D061 – $\overline{\text{MCLR}}$, RA4
- D063 – OSC1

The new values change the first page of **Section 26.3 "DC Characteristics"** as shown. (New values are indicated by bold text.)

26.3 DC Characteristics: PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	IIL	**Input Leakage Current(2,3)**				
D060		I/O ports	—	±**200**	nA	**VDD< 5.5V,** VSS ≤ VPIN ≤ VDD, Pin at high-impedance
			—	±**50**	**nA**	**VDD< 3V, VSS ≤ VPIN ≤ VDD, Pin at high-impedance**
D061		$\overline{\text{MCLR}}$	—	±**1**	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	±**1**	µA	VSS ≤ VPIN ≤ VDD

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

13. Module: Peripheral Highlights

Under the **"Peripheral Highlights"** section on page 1, Enhanced Addressable USART module, the first bullet should be changed to:

- Supports RS-485, RS-232 and LIN/J2602

14. Module: A/D Converter Characteristics

Table 26-24: A/D Converter Characteristics, on page 363, has been changed to update the offset error. The table has been reprinted with the updated values shown in bold text.

TABLE 26-24: A/D CONVERTER CHARACTERISTICS: PIC18F2221/2321/4221/4321 (INDUSTRIAL) PIC18LF2221/2321/4221/4321 (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	10	bit	$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	—	<±1	LSb	$\Delta V_{REF} \geq 3.0V$
A04	EDL	Differential Linearity Error	—	—	<±1	LSb	$\Delta V_{REF} \geq 3.0V$
A06	EOFF	Offset Error	—	—	**<±2**	LSb	$\Delta V_{REF} \geq 3.0V$
A07	EGN	Gain Error	—	—	<±1	LSb	$\Delta V_{REF} \geq 3.0V$
A10	—	Monotonicity	Guaranteed(1)			—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔV_{REF}	Reference Voltage Range ($V_{REFH} - V_{REFL}$)	1.8 3	— —	— —	V V	$V_{DD} < 3.0V$ $V_{DD} \geq 3.0V$
A21	VREFH	Reference Voltage High	—	—	VDD + 3.0V	V	
A22	VREFL	Reference Voltage Low	VSS – 0.3V	—	—	V	
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	
A50	IREF	VREF Input Current(2)	— —	— —	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

REVISION HISTORY

Rev A Document (3/2007)
Original version of this document. Includes Data Sheet Clarifications 1 through 7, removing all ICPORT references from the data sheet.

Rev B Document (4/2007)
Added Data Sheet Clarification 8 (Product Identification System).

Rev C Document (5/2007)
Added Data Sheet Clarification 9 (EUSART).

Rev D Document (7/2007)
Added Data Sheet Clarification 10 (Packaging Information).

Rev E Document (11/2007)
Modified Data Sheet Clarification 9 (EUSART) and added Data Sheet Clarification 11 (Electrical Characteristics).

Rev F Document (1/2008)
Added Data Sheet Clarification 12 (Electrical Characteristics, I/O Port Leakage Current).

Rev G Document (5/2008)
Modified Data Sheet Clarifications 11 (Electrical Characteristics) and 12 (Electrical Characteristics, I/O Port Leakage Current). Added Data Sheet Clarifications 13 (Peripheral Highlights) and 14 (A/D Converter Characteristics).

NOTES:

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