PIC18F85J11 FAMILY

PIC18F85J11 Family Rev. A4 Silicon Errata

The PIC18F85J11 family Rev. A4 parts you have received conform functionally to the Device Data Sheet (DS39774**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F85J11 family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F85J11 family devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC18F63J11	0011 1001 000	0 0100
PIC18F64J11	0011 1001 001	0 0100
PIC18F65J11	0011 1001 011	0 0100
PIC18F83J11	0011 1001 100	0 0100
PIC18F84J11	0011 1001 101	0 0100
PIC18F85J11	0011 1001 111	0 0100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F85J11 family silicon.

1. Module: Reset

When a Brown-out Reset (BOR) occurs and the BOR bit is reset, the Power-on Reset (POR) bit also may be reset. The resulting state matches that of the RCON register following a Power-on Reset event.

Consequently, an application may not be able to detect whether a BOR or POR event has occurred.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: MSSP (I^2C™ Slave)

When configured for I^2C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: MSSP (I^2C™ Master)

When in I^2C Master mode, if the slave performs clock stretching, the first clock pulse after the slave releases the SCL line may be narrower than the configured clock width. This may result in the slave missing the first clock in the next transmission/ reception.

Work around

The clock pulse will be the normal width if the slave does not perform clock stretching.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA<7> = 0)
- The EUSART is re-enabled (RCSTA<7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2 TCY delay after re-enabling the EUSART.

1. Disable receive interrupts (RCIE bit, PIE1<5> = 0).
2. Disable the EUSART (RCSTA<7> = 0).
3. Re-enable the EUSART (RCSTA<7> = 1).
4. Re-enable receive interrupts (PIE1<5> = 1).

   (This is the first TCY delay.)
5. Execute a NOP instruction.

   (This is the second TCY delay.)

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (11/2008)

Initial release of this errata. Includes silicon issues 1 (Reset), 2 (MSSP – I^2C Slave), 3 (MSSP – I^2C Master) and 4 (Enhanced Universal Synchronous Asynchronous Receiver Transmitter – EUSART).

NOTES:

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