dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family devices that you have received conform functionally to the current Device Data Sheet (DS70291**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				
		A1	A2	A3	A4	A5
dsPIC33FJ32MC302	0x0601	0x3001	0x3002	0x3002	0x3003	0x3004
dsPIC33FJ32MC304	0x0603					
dsPIC33FJ64MC202	0x0611					
dsPIC33FJ64MC204	0x0613					
dsPIC33FJ64MC802	0x0619					
dsPIC33FJ64MC804	0x061B					

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				
		A1	A2	A3	A4	A5
dsPIC33FJ128MC202	0x0621	0x3001	0x3002	0x3002	0x3003	0x3004
dsPIC33FJ128MC204	0x0623					
dsPIC33FJ128MC802	0x0629					
dsPIC33FJ128MC804	0x062B					

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)				
				A1	A2	A3	A4	A5
UART	IR Mode	1.	The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.	X	X	X	X	X
UART	High-Speed Mode	2.	When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.	X	X	X	X	X
SPI	Transmit Operation	3.	The SPI Transmit Buffer Full (SPITBF) flag does not get set immediately after writing to the buffer.	X	X	X	X	X
SPI	Frame Mode	4.	The SPI module will generate incorrect frame synchronization pulses in Frame Master mode if FRMDLY = 1.	X	X	X	X	X
I^2C™	SFR Writes	5.	The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.	X	X	X	X	X
I^2C	10-bit Addressing	6.	When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, A10 and A9 bits may not work as expected.	X	X	X	X	X
I^2C	10-bit Addressing	7.	When the I^2C module is configured as a 10-bit slave with an address of 0x02, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.	X	X	X	X	X
I^2C	—	8.	With the I^2C module enabled, the PORT bits and external Interrupt Input functions (if any) associated with SCL and SDA pins will not reflect the actual digital logic levels on the pins.	X	X	X	X	X
I^2C	10-bit Addressing	9.	The 10-bit slave does not set the RBF flag or load the I2CxRCV register, on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.	X	X	X	X	X
I^2C	—	10.	After the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.	X	X	X	X	X
UART	Interrupts	11.	The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)				
				A1	A2	A3	A4	A5
UART	IR Mode	12.	When the UART module is operating in 8-bit mode (PDSEL = 0x) and using the IrDA® encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.	X	X	X	X	X
Comparator	Output Pin	13.	When CMCON<CxOUTEN> bit is set, the Comparator output pin cannot be used as a general purpose I/O pin even if the Comparator is disabled.	X	X	X	X	X
Internal Voltage Regulator	Sleep Mode	14.	When the VREGS bit (RCON<8>) is set to a logic '0' the device may reset and higher Sleep current may be observed.	X	X	X	X	X
PSV Operations	—	15.	An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.	X	X	X	X	X
ECAN	Sleep Mode	16.	The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.	X	X	X	X	X
ECAN	Receive Operation	17.	The ECAN module may not store the received data in the correct location.	X	X	X		
CPU	EXCH Instruction	18.	The EXCH instruction does not execute correctly.	X	X	X	X	X
PWM	Debug Mode	19.	PTMR does not keep counting down after halting code execution in Debug mode.	X	X	X	X	X
PWM	DOZE Mode	20.	The Motor Control PWM module generates more interrupts than expected when DOZE mode is used and the output postscaler value is different than 1:1.	X	X	X	X	X
SPI	Transmit Operation	21.	Writing to the SPIxBUF register as soon as TBF bit is cleared will cause SPI module to ignore written data.	X	X	X	X	X
UART	Break Character Generation	22.	The UART module will not generate back-to-back Break characters.	X	X	X	X	X
QEI	Timer Gated Accumulation Mode	23.	When Timer Gated Accumulation is enabled, the QEI does not generate an interrupt on every falling edge.	X	X	X	X	X
QEI	Timer Gated Accumulation Mode	24.	When Timer Gated Accumulation is enabled, and an external signal is applied, the POSCNT increments and generates an interrupt after a match with MAXCNT.	X	X	X	X	X
Audio DAC	Voltage Specifications	25.	The Audio DAC positive and negative output differential voltages may not meet the specifications listed in the data sheet.	X	X	X		
ADC	Current Consumption in Sleep Mode	26.	If the ADC module is in an enabled state when the device enters Sleep mode, the power-down current (IPD) of the device may exceed the device data sheet specifications.	X	X	X	X	X
JTAG	Boundary Scan	27.	On 28-pin devices, Boundary Scan does not function correctly for pin 7.	X	X	X	X	X
RTCC	Operation During Reset	28.	The RTCC module gets reset on any device Reset, instead of getting reset only on a POR or BOR.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)				
				A1	A2	A3	A4	A5
All	150ºC Operation	29.	These revisions of silicon only support 140ºC operation instead of 150ºC for Hi-Temp operating temperature.	X	X	X		
I/O Port	Data Direction Setting	30.	When the RB8 pin is in open-drain configuration, the data direction depends upon the TRISB9 bit instead of the TRISB8 bit.	X	X	X	X	X
CPU	Interrupt Disable	31.	When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X	X	X	X	X
CPU	`div.sd`	32.	When using the `div.sd` instruction, the overflow bit is not getting set when an overflow occurs.	X	X	X	X	X
UART	TX Interrupt	33.	A transmit (TX) Interrupt may occur before the data transmission is complete.	X	X	X	X	X
JTAG	Flash Programming	34.	JTAG Flash programming is not supported.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

2. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

3. Module: SPI

The SPI Transmit Buffer Full (SPITBF) flag does not get set immediately after writing to the buffer.

Work around

After a write to the SPI buffer, poll the SPITBF flag until the flag gets set, indicating that the transmit buffer is not full. Afterwards, poll the SPITBF flag again until the flag gets cleared, indicating that the transmit has started and that the transmit buffer is empty and another write can occur.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

4. Module: SPI

The SPI module will generate incorrect frame synchronization pulses when configured in Frame Master mode if the start of data is selected to coincide with the start of the frame synchronization pulse (FRMEN = 1, SPIFSD = 0, FRMDLY = 1). However, the module functions correctly in Frame Slave mode, and also in Frame Master mode if FRMDLY = 0.

Work around

If DMA is not being used, manually drive the SSx pin (x = 1 or 2) high using the associated PORT register, and then drive it low after the required 1 bit-time pulse width. This operation needs to be performed when the transmit buffer is written.

If DMA is being used, and if no other peripheral modules are using DMA transfers, use a timer interrupt to periodically generate the frame synchronization pulse (using the method described above) after every 8 or 16-bit periods (depending on the data word size, configured using the MODE16 bit).

If FRMDLY = 0, no work around is needed.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

5. Module: I^2C

The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.

Work around

Use Word instructions to clear the BCL bit.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

6. Module: I²C

If there are two I²C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit Addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I²C devices, the addresses as well as bits A10 and A9 should be different.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

7. Module: I²C

When the I²C module is configured as a 10-bit slave with and address of 0x02, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

8. Module: I²C

With the I²C module enabled, the PORT bits and external interrupt input functions (if any) associated with the SCL and SDA pins do not reflect the actual digital logic levels on the pins.

Work around

If the SDA and/or SCL pins need to be polled, these pins should be connected to other port pins in order to be read correctly. This issue *does not* affect the operation of the I²C module.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

9. Module: I²C

In 10-bit Addressing mode, some address matches do not set the RBF flag or load the receive register I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

10. Module: I²C

When the I²C module is operating in either Master or Slave mode, after the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK from the master.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

11. Module: UART

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

12. Module: UART

When the UART is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

13. Module: Comparator

If CMCON<CxOUTEN> bit is set and the comparator module CMCON<CxEN> bit is disabled, the remappable comparator output pins, C1OUT and C2OUT, cannot be used as general purpose I/O pins.

Work around

When the comparator module is disabled the CMCON<CxOUTEN> bit should be reset so that the remappable comparator output pins C1OUT and C2OUT are not driven onto the output pad.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

14. Module: Internal Voltage Regulator

When the VREGS bit (RCON<8>) is set to a logic '0', the device may reset and a higher Sleep current may be observed.

Work around

Ensure the VREGS bit (RCON<8>) is set to a logic '1' for device Sleep mode operation.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

15. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (Word or Byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

16. Module: ECAN

The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.

When the device wakes up from Sleep due to CAN bus activity, the ECAN module is placed in operational mode. The ECAN Event interrupt occurs due to the WAKIF flag. Trying to clear the flag in the Interrupt Service Routine (ISR) may not clear the flag. The WAKIF bit being set will not cause repetitive Interrupt Service Routine execution.

Work around

Although the WAKIF bit does not clear, the device Sleep and ECAN Wake function continue to work as expected. If the ECAN event is enabled, the CPU will enter the Interrupt Service Routine due to the WAKIF flag getting set. The application can maintain a secondary flag, which tracks the device Sleep and Wake events.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

17. Module: ECAN

The ECAN module may not store received data in the correct location. When this occurs, the receive buffers will become corrupted. In addition, it is also possible for the transmit buffers to become corrupted. This issue is more likely to occur as the CAN bus speed approaches 1 Mbps.

Work around

Do not use the DMA with ECAN in Peripheral Indirect mode. Use the DMA in Register Indirect mode, Continuous mode enabled and Ping Pong mode disabled. The receive DMA channel count should be set to 8 words. The transmit DMA channel count should be set for the actual message size (maximum of 7 words for Extended CAN messages and 6 words for Standard CAN Messages). To simplify application error handling while using this mode, only one TX buffer should be used. While message filtering is not affected, messages will not be stored at distinct RX buffers. Instead all messages are stored contiguously in memory. The start of this memory is pointed to by the receive DMA channel. The application must still clear RXFUL flags and other interrupt flags. The application must manage the RX buffer memory.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X					

18. Module: CPU

The EXCH instruction does not execute correctly.

Work around

If writing source code in assembly, the recommended work around is to replace:

```
EXCH Wsource, Wdestination
```

with:

```
PUSH Wdestination
MOV Wsource, Wdestination
POP Wsource
```

If using the MPLAB C30 C compiler, specify the compiler option: `-merrata=exch` (*Project > Build Options > Projects > MPLAB C30 > Use Alternate Settings*).

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

19. Module: PWM

If the PTDIR bit is set (when PTMR is counting down), and the CPU execution is halted (after a breakpoint is reached), PTMR will start counting up, as if PTDIR was zero.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

20. Module: PWM

When the device is operated in DOZE mode and the Motor Control PWM module has a postscaler set to any value different than 1:1 (PTOPS > `0` in PxTCON register), the Motor Control PWM module generates more interrupts than expected.

Work around

Do not use DOZE mode with the Motor Control PWM if the time base output postscaler is different than 1:1 (PTOPS > `0` in PxTCON register).

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

21. Module: SPI

Writing to the SPIxBUF register as soon as the TBF bit is cleared will cause the SPI module to ignore the written data. Applications which use SPI with DMA will not be affected by this erratum.

Work around

After the TBF bit is cleared, wait for a minimum duration of one SPI Clock before writing to the SPIxBUF register.

Alternatively, do one of the following:

- Poll the RBF bit and wait for it to get set before writing to the SPIxBUF register
- Poll the SPI Interrupt flag and wait for it to get set before writing to the SPIxBUF register
- Use an SPI Interrupt Service Routine
- Use DMA

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

22. Module: UART

The UART module will not generate consecutive break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

23. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, a QEI interrupt should be generated after an input pulse on the QEA input. This interrupt is not generated in the affected silicon.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

24. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, the POSCNT counter should not increment but erroneously does, and if allowed to increment to match MAXCNT, a QEI interrupt will be generated.

Work around

To prevent the erroneous increment of POSCNT while running the QEI in Timer Gated Accumulation mode, initialize MAXCNT = 0.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

25. Module: Audio DAC

The Audio DAC positive differential output voltage and negative differential output voltage (parameters DA01 and DA02, respectively) may not meet the specifications listed in the data sheet.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X					

26. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a PWRSAV #0 instruction, the device power-down current (I_{PD}) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work around 1:

In order to remain within the I_{PD} specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a PWRSAV #0 instruction.

Note:	The ADC module must be reinitialized by the user application before resuming ADC operation.

Work around 2:

If the ADC module was previously initialized and enabled, before entering Sleep, execute the lines of code provided in Example 1.

Note:	Unlike **Work around 1**, the user application does not need to reinitialize the ADC module; however, it is necessary to re-enable the ADC module by setting the ADON bit after waking from Sleep.

EXAMPLE 1:

```
AD1CON1bits.ADON = 0;             //Disable the ADC module
__asm__ volatile ("REPEAT #50");  //Wait 50 Tcy
__asm__ volatile ("NOP");         //Repeat NOP 51 times
Sleep();                          // Execute PWRSAV #0 and go to Sleep
```

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

27. Module: JTAG

On 28-pin devices, JTAG Boundary Scan does not function correctly for pin 7. Both pins 6 and 7 respond to stimulus applied to pin 7.

Work around

Do not include pin 7 in the JTAG Boundary Scan chain for 28-pin devices.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

28. Module: RTCC

The RTCC module gets reset on any device Reset, instead of getting reset only on a POR or BOR.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

29. Module: All

The affected silicon revisions listed below are not warranted for operation at 150ºC.

Work around

Only use the affected revisions of silicon for Hi-Temp operating range from -40ºC to +140ºC.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X					

30. Module: I/O Port

When the ODCB8 bit is set to '1' (open-drain configuration), the data direction on the RB8 pin is controlled by the TRISB9 bit instead of the TRISB8 bit.

Work around

Do not use the RB8 pin in open-drain configuration while simultaneously using the RB9 pin.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

31. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for 'n'.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

32. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

33. Module: UART

When using UTXISEL = 01 (Interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) Interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occur only when all transmit operations are complete. Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

34. Module: JTAG

JTAG Flash programming is not supported.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A5			
X	X	X	X	X			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70291**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No issues to report at this time.

APPENDIX A: REVISION HISTORY

Rev A Document (3/2009)

Initial release of this document; issued for revision A1, A2 and A3 silicon.

Includes silicon issues 1-2 (UART), 3-4 (SPI), 5-10 (I^2C), 11-12 (UART), 13 (Comparator), 14 (Internal Voltage Regulator), 15 (PSV Operations), 16-17 (ECAN), 18 (CPU), 19-20 (PWM) and 21 (SPI).

This document replaces the following errata document:

"dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 Rev. A1/A2/A3 Silicon Errata" (DS80372)

Rev B Document (4/2009)

Corrected part numbers.

Rev C Document (8/2009)

Added silicon issues 22 (UART) and 23-24 (QEI).

Rev D Document (1/2010)

Added Rev. A4 silicon information.

Added silicon issue 25 (Audio DAC).

Rev E Document (6/2010)

Updated silicon issue 18 (CPU).

Added silicon issues 26 (ADC), 27 (JTAG) and 28 (RTCC), and data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

Rev F Document (10/2010)

Updated the work around in silicon issue 26 (ADC).

Added silicon issue 29 (All).

Rev G Document (3/2011)

Removed data sheet clarification 1.

Updated the Affected Silicon Revisions for item 29 in Table 2 and in silicon issue 29 (All).

Added silicon issue 30 (I/O Port).

Rev H Document (11/2011)

Updated the current Device Data Sheet revision to "F".

Added Rev. A5 silicon information.

Added silicon issues 31 (CPU), 32 (CPU), 33 (UART), and 34 (JTAG).

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