ORT82G5/42G5

3.7 Gbps DEMONSTRATED!

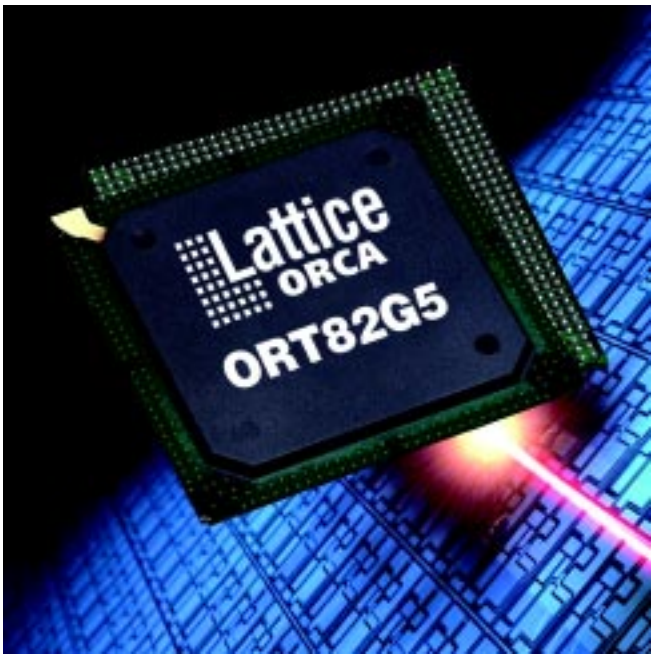
The World's Fastest Programmable Backplane Transceivers!

Building Better Backplanes...

Lattice Semiconductor has developed a new generation of Field Programmable System Chips (FPSC) targeted at high-speed serial backplane data transmission. Built on the ORCA® Series 4 reconfigurable embedded system-on-a-chip (SoC) architecture, the ORT82G5 contains eight backplane transceiver channels, each operating in the range from 600 Mbits/sec to 3.7 Gbps, together with a full-duplex synchronous interface with built-in clock and data recovery (CDR), and more than 10,000 lookup tables. The ORT42G5 provides the same functionality with four SERDES channels.

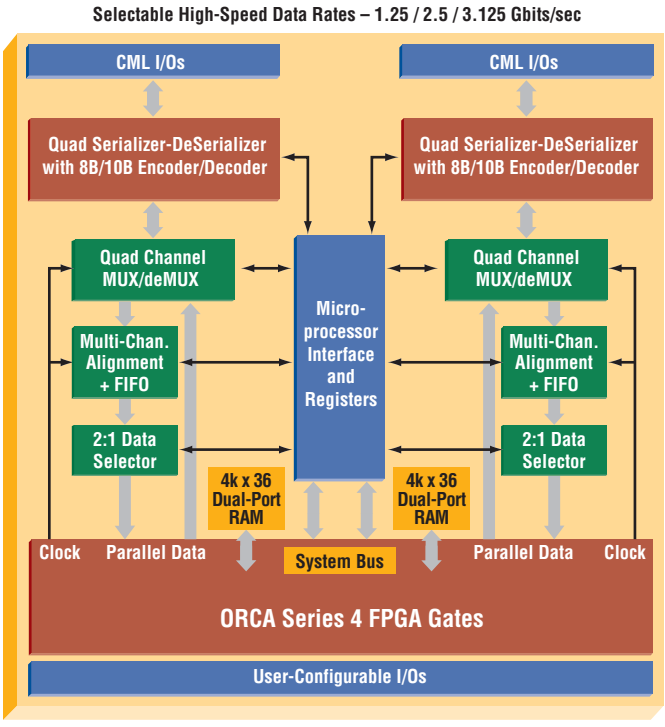
Designers can also use the devices to drive high-speed data transfers across buses within systems because of the embedded 8b/10b capability. For example, with the ORT82G5, designers can build a 20 Gbps bridge (10 Gbps work and 10 Gbps protect) for 10 Gbps Ethernet; the high-speed SERDES interfaces implement two XAUI interfaces with configurable back-end interfaces such as XGMII implemented on the FPGA side. The ORT82G5 can also be used to provide two full 10 Gbps backplane data connections for work and protection between a line card and switch fabric. The ORT42G5 can be used for one full-duplex 10 Gbps backplane data connection between a line card and switch fabric.

Both the ORT82G5 and ORT42G5 offer a clockless high-speed interface for inter-device communication on a board or across a backplane. The built-in clock recovery of the ORT82G5 and ORT42G5 allows higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane.



Network designers will also benefit from the backplane transceivers as network termination devices. The devices support embedded 8b/10b encoding/decoding and link state machines for 10G Ethernet, as well as Fibre Channel.

ORCA ORT82G5 Block Diagram



Note: The ORT42G5 provides one quad SERDES channel.

Key Features and Benefits

- **High Performance ORCA Series 4 FPGA Gates:**
  - Internal performance of > 250 MHz.
  - Over 10,000 Lookup Tables.
  - 1.5V operation (30% less power than 1.8V operation)
  - Comprehensive I/O selections including LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL3/2, HSTL, ZBT, DDR, LVDS, bus-LVDS, and LVPECL.
- **Ease of Design**
  - Supported by ispLEVER™ ver. 3.0 design software.
  - Complete ORT82G5 and ORT42G5 design kits supplies simulation models for embedded core, configuration tool, and integrates with ispLEVER ver. 3.0 design software.
- **Easy System Integration**
  - SERDES performance exceeds XAUI specifications.
  - XGMII IP core for FPGA side supports interfacing to 10 Gbps Ethernet MACs.
  - XAUI to XGMII translator (XGXS IP Core)
  - Easy integration of 10 Gbps Ethernet and Fibre-Channel for data over fibre applications.

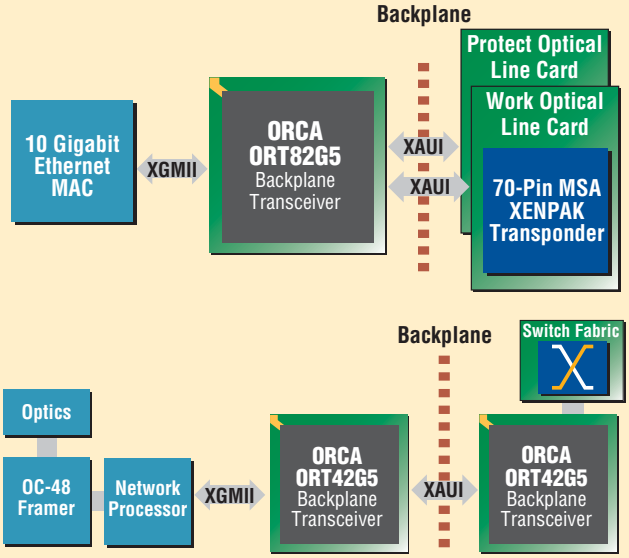
ORCA ORT82G5 and ORT42G5 Attributes

Device	FPGA Usable Gates	PFUs	LUTs	Registers	PFU RAM Bits	EBR RAM Bits	FPGA User I/O	Package	FPGA I/O Compatibility	SERDES Channels	Max Data Rate per Channel
ORT82G5	333 - 643K	1,296	10,368	12,780	277K	111K	372	680PBGAM	1.5/1.8/2.5/3.3V	8	3.7 Gbps
ORT42G5	333 - 643K	1,296	10,368	12,780	277K	111K	204	484PBGAM	1.5/1.8/2.5/3.3V	4	3.7 Gbps

ORCA ORT82G5 and ORT42G5 Applications

The ORT82G5 and ORT42G5 are ideal for 10 Gigabit Ethernet systems. The ORT82G5 provides 8 channels of 3.125 Gbps data to drive across two XAUI backplanes for work and protection. The ORT42G5 provides one channel of 3.125 Gbps data to drive across one XAUI backplane connection. Both devices connects directly to a XENPAK optical transponder on the line card side, and to a 10 GbE MAC via an XGMII interface implemented in FPGA gates. This elegant solution allows network system designers to immediately deploy 10 GbE in the LAN, in the MAN, and in the WAN.

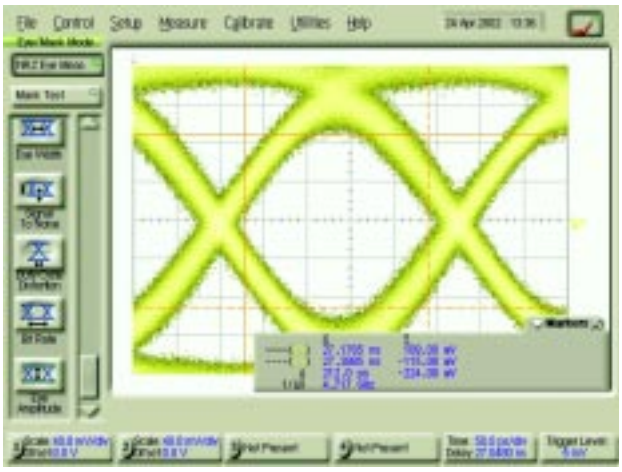
The ORT42G5 can be used as a cost-effective backplane driver for systems requiring up to 10Gbps across a XAUI-based backplane. The programmable gates on the ORT42G5 are ideal for implementing interfaces to switch fabrics or network processors.



Embedded Core Features

- Robust High Speed - Reliable transmission over:
  - 26 inches of FR4 at 3.7 Gbps
  - 40 inches of FR4 at 3.125 Gbps
  - 75 feet of co-axial cable at 622 Mbps
- Lowest power consumption of any programmable SERDES – less than 225mW (worst case) per channel at 3.125 Gbps over full temperature/voltage range.
- Low Tx Jitter: 0.17UI @ 3.125 Gbps
- Excellent Receive Jitter Tolerance: 0.75 UI @ 3.125 Gbps
- Transmit pre-emphasis (programmable) for improved receive data eye opening: 0%, 12.5%, 25%
- 32-bit (8b/10b) or 40-bit (raw data) parallel internal bus for data processing in FPGA logic.
- Exceeds XAUI serial data specification for 10 GbE applications with protection. Includes integrated XAUI state machine.
- Compliant to Fibre Channel physical layer specification, including integrated Fibre Channel state machine.
- SERDES has low-power CML buffers to allow use with optical transceiver, coaxial copper media, shielded twisted pair wiring or high-speed backplanes such as FR-4.

ORT82G5 and ORT42G5 CDR Eye Diagram Measurements



Actual data eye at 3.7 Gbps across 26 inches of FR-4 backplane with 25% pre-emphasis.

Applications Support
1-800-LATTICE (528-8423)
(408) 826-6002
techsupport@latticesemi.com

Lattice Semiconductor Corporation
www.latticesemi.com

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