ConnectCore™ 9P 9215, Wi-9P 9215, and 3G 9P 9215

Hardware Reference

90000879_L

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Using this Guide

This guide provides information about the Digi ConnectCore 9P 9215 family of embedded core modules.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

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About the Module

CHAPTER 1

The ConnectCore 9P 9215 family of modules delivers powerful network-enabled core processor solutions with up to 16 MB of NOR flash, up to 32 MB SDRAM, a rich set of integrated peripherals, and superior design flexibility.

At the heart of the modules is a Digi 32-bit ARM9-based Digi NS9215 processor running at 150 MHz. Key features include 10/100 Mbit Ethernet, two on-chip Flexible Interface Modules (FIMs), 256-bit AES accelerator, power management modes with dynamic clock scaling, and a rich set of on-chip peripherals. Based on Digi 802.11 baseband technology, the ConnectCore Wi-9P 9215 also provides an additional 802.11a/b/g interface with enterprise-grade WPA2/802.11i support.

The ConnectCore 3G 9P 915 module allows you to instantly add intelligent cellular communication to your products.

Built on leading Qualcomm Gobi 2000 technology, the module delivers a pre-certified embedded cellular connectivity solution without the traditional carrier/network limitations. Selecting cellular network technology and carriers is now a matter of software configuration and service provisioning, any time.

The unique FIMs on the Digi NS9215 processor are two independent 300 MHz DRPIC165X processor cores that allow customers to dynamically select application-specific interfaces in software. The growing list of supported interfaces includes UART, SD/SDIO, CAN bus, USB-device low-speed, 1-Wire®, USB device low-speed, parallel bus interface, and others.

Utilizing the Digi NET+ARM processor and secure 802.11a/b/g WLAN technology, the family of ConnectCore 9P 9215 modules offers the industry's only network-enabled core module with true long-term product availability to meet the extended life cycle requirements of embedded product designs.

For further information about the Digi NS9215, see the Digi NS9215 Hardware Reference Manual.

Features and functionality

- 32-bit NET+ARM (ARM926EJ-S) RISC processor Digi NS9215 @ 150MHz
- ARM9 core with memory management unit (MMU)
- 4K data cache/4K instruction cache
- 8MB SDRAM (can support a maximum of 64MB SDRAM)
  - ConnectCore 3G 9P 9215: 32MB SDRAM, 8MB NOR, 128MB NAND
  - SDRAM width: 32
- 4MB NOR Flash (can support a maximum of 16MB NOR flash)
- 10 general purpose timers; ConnectCore 9P 9215 supports 7 as timer/counters and one quadrature decoder
- 64 GPIOs signals with up to five different multiplexing schemes (all are on connector X2)
- Two 80-pin connectors
- Up to four UARTs
- One SPI channel, multiplexed on different places
- Integrated 10/100Mbps Ethernet MAC/PHY
- Integrated IEEE802.11a/b/g WLAN with U.FL connectors on module (ConnectCore Wi-9P 9215 specific)
- I^2C interface
- JTAG signals available on module connector
- 8 ADC (analog to digital converter) inputs
- 2x flexible interface modules (FIMs) running at max. 300 MHz, integrated in NS9215 processor
- 2 LEDs (LE1: green, and LE2:orange) available on the Development Board
- 16-bit data and 17-bit address buses, both are buffered
- Single +3.3V power supply

Module variant

The ConnectCore 9P 9215 module is currently available in standard variants below.

Product numbers:	Features
CC-9P-V502-C	150 MHz CPU speed, 8MB SDRAM, 4 MB NOR flash, RTC, 10/100 Mbps Ethernet
CC-9P-V501-C	150 MHz CPU speed, 8MB SDRAM, 2MB NOR flash, RTC, 10/100 Mbps Ethernet
CC-9P-V526UH-S	150 MHz CPU speed, 32MB SDRAM, 8MB NOR flash, 128MB NAND, single SIM
CC-9P-V526UJ-S	150 MHz CPU speed, 32MB SDRAM, 8MB NOR flash, 128MB NAND, dual SIM

Module pinout

The module has two 80 pins connectors, X1 and X2. The next tables describe each pin, its properties, and its use on the Development Board.

Pinout legend:

Type

I	Input
O	Output
I/O	Input or output
P	Power

X1 pinout

X1 pin number	Type	Module functionality	Usage on Development Board	Comments
1	P	GND	GND	
2	P	GND	GND	
3	I	RSTIN#	RSTIN#	10k pull-up on module
4	O	PWRGOOD	PWRGOOD	Output of the reset controller push pull with 470R current limiting resistor
5	O	RSTOUT#	RSTOUT#	Output of logical AND function between NS9215 RESET_DONE and NS9215 RESET_OUT#
6	I	TCK	TCK	JTAG - 10k pull-up on module
7	I	TMS	TMS	JTAG - 10k pull-up on module
8	I	TDI	TDI	JTAG - 10k pull-up on module
9	O	TDO	TDO	JTAG - 10k pull-up on module
10	I	TRST#	TRST#	JTAG - 2k2 pull-down on module
11	O	RTCK	RTCK	JTAG - Optional
12	I	CONF2/OCD_EN#	CONF2/OCD_EN#	10k pull-up on module
13	I	LITTLE# / BIG ENDIAN	LITTLE# / BIG ENDIAN	2k2 series resistor on module
14	I	ConnectCore Wi-9P 9215: WLAN_DISABLE#	WLAN_DISABLE#	Low active WLAN Disable signal
	I	ConnectCore 3G 9P 9215: CELL_DISABLE_N	CELL_DISABLE_N	Normally connected to X2-15
15	I	SOFT_CONF0	SOFT_CONF0	2k2 series resistor on module

X1 pin number	Type	Module functionality	Usage on Development Board	Comments
16	I	SOFT_CONF1	SOFT_CONF1	2k2 series resistor on module
17	I	SOFT_CONF2	SOFT_CONF2	2k2 series resistor on module
18	I	SOFT_CONF3	SOFT_CONF3	2k2 series resistor on module
19	O	ConnectCore Wi-9P 9215: (WLAN_LED#)	(WLAN_LED#)	Active low signal coming from low-active WLAN signal. This signal comes directly from the Piper chip without series resistor.
	O	ConnectCore 3G 9P 9215: LED_WWAN#	LED_WWAN#	Reserved
20	P	GND	GND	
21	I/O	D0	D0	Buffered Data - only active when either CS0# or CS2# is active NS9215 D[31:16]
22	I/O	D1	D1	
23	I/O	D2	D2	
24	I/O	D3	D3	
25	I/O	D4	D4	
26	I/O	D5	D5	
27	I/O	D6	D6	
28	I/O	D7	D7	
29	I/O	D8	D8	
30	I/O	D9	D9	
31	I/O	D10	D10	
32	I/O	D11	D11	
33	I/O	D12	D12	
34	I/O	D13	D13	
35	I/O	D14	D14	
36	I/O	D15	D15	
37	P	GND	GND	
38	O	AO	AO	Buffered Address always active
39	O	A1	A1	
40	O	A2	A2	
41	O	A3	A3	
42	O	A4	A4	

X1 pin number	Type	Module functionality	Usage on Development Board	Comments
43	O	A5	A5	
44	O	A6	A6	
45	O	A7	A7	
46	O	A8	A8	
47	O	A9	A9	
48	O	A10	A10	
49	O	A11	A11	
50	O	A12	A12	
51	O	A13	A13	
52	O	A14	A14	
53	O	A15	A15	
54	O	A16	A16	
55	O	GND	GND	
56	O	EXT_OE#	EXT_OE#	
57	O	EXT_WE#	EXT_WE#	
58	O	CSO#	CSO#	
59	O	CS2#	CS2#	Reserved for the ConnectCore 3G 9P 9215, leave unconnected.
60	O	BLE#	BLE#	NS9215 BE2#
61	O	BHE#	BHE#	NS9215 BE3#
62	I	EXT_WAIT#	EXT_WAIT#	10k pull-up on module
63	O	BCLK	BCLK	Connected over a 22R resistor to NS9215 CLK_OUT1 pin
64	P	GND	GND	
65	I	ETH_TPIN	ETH_TPIN	
66	O	ETH_ACTIVITY#	ETH_ACTIVITY#	Low active signal with 330R resistor on module
67	I	ETH_TPIP	ETH_TPIP	
68	O	ETH_LINK#	ETH_LINK	Low active signal with 330R resistor on module
69	O	ETH_TPON	ETH_TPON	
70	O	ETH_TROP	ETH_TROP	
71	P	GND	GND	

X1 pin number	Type	Module functionality	Usage on Development Board	Comments
72	P			Reserved for the ConnectCore 3G 9P 9215: +3.3V additional power supply pin
73	I	Reserved (USB_OC#)	Reserved (USB_OC#)	Reserved for the ConnectCore 3G 9P 9215: USB_OC# over current input of OXU210
74	I/O	Reserved (USB_P)	Reserved (USB_P)	Reserved for the ConnectCore 3G 9P 9215: USB_P OTG channel
75	I/O	Reserved (USB_N)	Reserved (USB_N)	Reserved for the ConnectCore 3G 9P 9215: USB_N OTG channel
76	O	Reserved (USB_PWREN#)	Reserved (USB_PWREN#)	Reserved for the ConnectCore 3G 9P 9215: USB_PWR# output of OXU210
77	I	Reserved	Reserved	
78	P	VRTC	VRTC	Backup Battery for RTC, for 3V cell. Can be left floating, if RTC backup not needed.
79	P	VLIO	VLIO	Mobile: Power from Li-Ion Battery (2.5V-5.5V) Non-Mobile: connected to 3.3V
80	P	GND	GND	

X2 pinout

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
1	P	GND		
2	P	GND		
3	I/O	DCDA#/ DMA0_DONE/ PIC_0_GEN_IO[0] GPIO0/ SPI_EN (dup)		See Note 1.
4	I/O	CTSA#/ EIRQ0/ PIC_0_GEN_IO[1] GPIO1/ -reserved-		See Note 1.
5	I/O	DSRA#/ EIRQ1/ PIC_0_GEN_IO[2] GPIO2/ -reserved-		See Note 1.
6	I/O	RXDA/ DMA0_PDEN/ PIC_0_GEN_IO[3] GPIO3/ SPI_RX (dup)		See Note 1.
7	I/O	RIA#/ EIRQ2/ Timer6_in/ GPIO4 SPI_CLK (dup)/		See Note 1.
8	I/O	RTSA#/ RS485CTLA EIRQ3/ Timer6_Out/ GPIO5/ SPI_CLK (dup)/		See Note 1.
9	I/O	DTRA#/ TXCLKA DMA0_REQ/ Timer7_In/ GPIO6/ PIC_DBG_DATA_OUT		See Note 1.

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
10	I/O	TXDA/ Timer8_In/ Timer7_Out/ GPIO7/ SPI_TX (dup)		See Note 1.
11	I/O	DCDC#/ DMA1_DONE/ Timer8_Out/ GPIO8/ SPIB_EN (dup)/		See Note 2.
12	I/O	CTSC#/ I2C_SCK/ EIRQ0 (dup)/ GPIO9/ PIC_DBG_DATA_IN		See Note 2.
13	I/O	DSRC#/ QDCI/ EIRQ1 (dup) GPIO10/ PIC_DBG_CLK		See Note 2.
14	I/O	RXDC/ DMA1_DP/ EIRQ2 (dup)/ GPIO11/ SPI_RXboot		
15	I/O	RIC#/ RXCLKC I2C_SDA/ RST_DONE/ GPIO12/ SPI_CLK (dup)		When booting, NS9215 RIC# signal is default configured as Output, RST_DONE. To avoid input/output conflicts, put a series resistor on this signal if necessary. Also, for the ConnectCore 3G 9P 9215, this pin is the cellular disable output and should be tied directly to the CELL_DISABLE_N, pin X1-14.

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
16	I/O	RTSC#/ QDCQ/ Ext Timer Event Out Ch 9/ GPIO13/ SPI_CLKboot		See Note 2.
17	I/O	DTRC#/ TXCLKC DMA1_REQ/ PIC_0_CAN_RXD GPIO14/ SPI_TXDboot		
18	I/O	TXDC/ Timer9_In/ PIC_0_CAN_TXD GPIO15/ SPI_ENboot		See Note 2.
19	I/O	DCDB# (dup)/ PIC_0_BUS_1[8] PIC_1_BUS_1[8] GPIO51/		See Note 1.
20	I/O	CTSB# (dup)/ PIC_0_BUS_1[9] PIC_1_BUS_1[9] GPIO52/		See Note 1.
21	I/O	DSRB# (dup)/ PIC_0_BUS_1[10] PIC_1_BUS_1[10] GPIO53/		See Note 1.
22	I/O	RXDB (dup)/ PIC_0_BUS_1[11] PIC_1_BUS_1[11] GPIO54/		See Note 1.
23	I/O	RIB# (dup)/ PIC_0_BUS_1[12] PIC_1_BUS_1[12] GPIO55/		See Note 1.
24	I/O	RTSB# (dup) / RS485CTLB (dup) / PIC_0_BUS_1[13] PIC_1_BUS_1[13] GPIO56/		See Note 1.

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
25	I/O	TXCLKB (dup)/ DTRB# (dup) / PIC_0_BUS_1[14] PIC_1_BUS_1[14] GPIO57/		See Note 1.
26	I/O	TXDB (dup)/ PIC_0_BUS_1[15] PIC_1_BUS_1[15] GPIO58/		See Note 1.
27	I/O	DCDD# (dup) / PIC_0_BUS_1[16] PIC_1_BUS_1[16] GPIO59/		See Note 1.
28	I/O	CTSD# (dup)/ PIC_0_BUS_1[17] PIC_1_BUS_1[17] GPIO60/		See Note 1.
29	I/O	DSRD# (dup)/ PIC_0_BUS_1[18] PIC_1_BUS_1[18] GPIO61/		See Note 1.
30	I/O	RXDD (dup)/ PIC_0_BUS_1[19] PIC_1_BUS_1[19] GPIO62/		See Note 1.
31	I/O	RID# (dup)/ PIC_0_BUS_1[20] PIC_1_BUS_1[20] GPIO63/		See Note 1.
32	I/O	RTSD# (dup) / RS485CTLD(dup) / PIC_0_BUS_1[21] PIC_1_BUS_1[21] GPIO64/		See Note 1.
33	I/O	TXCLKD (dup) / DTRD# (dup) / PIC_0_BUS_1[22] PIC_1_BUS_1[22] GPIO65		See Note 1.
34	I/O	TXDD (dup) / PIC_0_BUS_1[23] PIC_1_BUS_1[23] GPIO66		See Note 1.

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
35	I/O	PIC_0_CLK[I] PIC_0_CLK[0] EIRQ3 (dup)/ GPIO67		See Note 1.
36	I/O	PIC_0_GEN_IO[0] PIC_1_GEN_IO[0] PIC_1_CAN_RXD GPIO68		See Note 1.
37	I/O	PIC_0_GEN_IO[1] PIC_1_GEN_IO[1] PIC_1_CAN_TXD GPIO69		See Note 1.
38	I/O	PIC_0_GEN_IO[2] PIC_1_GEN_IO[2] PWM0/ GPIO70		See Note 1.
39	I/O	PIC_0_GEN_IO[3] PIC_1_GEN_IO[3] PWM1/ GPIO71		See Note 1.
40	I/O	PIC_0_GEN_IO[4] PIC_1_GEN_IO[4] PWM2/ GPIO72		See Note 1.
41	I/O	PIC_0_GEN_IO[5] PIC_1_GEN_IO[5] PWM3/ GPIO73		See Note 1.
42	I/O	PIC_0_GEN_IO[6] PIC_1_GEN_IO[6] Timer0_In/ GPIO74		See Note 1.
43	I/O	PIC_0_GEN_IO[7] PIC_1_GEN_IO[7] Timer1_In/ GPIO75		See Note 1.
44	I/O	PIC_0_CTL_IO[0] PIC_1_CTL_IO[0] Timer2_In/ GPIO76		See Note 1.

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
45	I/O	PIC_0_CTL_IO[1] PIC_1_CTL_IO[1] Timer3_In/ GPIO77		See Note 1.
46	I/O	PIC_0_CTL_IO[2] PIC_1_CTL_IO[2] Timer4_In/ GPIO78		See Note 1.
47	I/O	PIC_0_CTL_IO[3] PIC_1_CTL_IO[3] Timer5_In/ GPIO79		See Note 1.
48	I/O	PIC_0_BUS_0[0] PIC_1_BUS_0[0] Timer6_In (dup)/ GPIO80		See Note 1.
49	I/O	PIC_0_BUS_0[1] PIC_1_BUS_0[1] Timer7_In (dup)/ GPIO81		
50	I/O	PIC_0_BUS_0[2] PIC_1_BUS_0[2] Timer8_In (dup)/ GPIO82		See Note 1.
51	I/O	PIC_0_BUS_0[3] PIC_1_BUS_0[3] Timer9_In (dup)/ GPIO83		
52	I/O	PIC_0_BUS_0[4] PIC_1_BUS_0[4] Timer0_Out/ GPIO84		See Note 1.
53	I/O	PIC_0_BUS_0[5] PIC_1_BUS_0[5] Timer1_Out/ GPIO85		For the ConnectCore 3G 9P 9215, this pin is reserved as a soft reset input, active low.
54	I/O	PIC_0_BUS_0[6] PIC_1_BUS_0[6] Timer2_Out/ GPIO86		

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
55	I/O	PIC_0_BUS_0[7] PIC_1_BUS_0[7] Timer3_Out/ GPIO87		
56	I/O	PIC_0_BUS_0[13]/ PIC_1_BUS_0[13]/ Timer9_Out (dup)/ GPIO93		
57	I/O	PIC_0_BUS_0[14]/ PIC_1_BUS_0[14]/ QDCI (dup)/ GPIO94		
58	I/O	PIC_0_BUS_0[15]/ PIC_1_BUS_0[15]/ QDCQ (dup)/ GPIO95		
59	I/O	PIC_0_BUS_1[0]/ PIC_1_BUS_1[0]/ PIC_0_CAN_RXD GPIO96		
60	I/O	PIC_0_BUS_1[1]/ PIC_1_BUS_1[1]/ PIC_0_CAN_TXD GPIO97		
61	I/O	PIC_0_BUS_1[2]/ PIC_1_BUS_1[2]/ PIC_1_CAN_RXD GPIO98		
62	I/O	PIC_0_BUS_1[3]/ PIC_1_BUS_1[3]/ PIC_1_CAN_TXD GPIO99		
63	I/O	PIC_0_BUS_1[4]/ PIC_1_BUS_1[4]/ PWM4/ GPIO100		See Note 1.
64	I/O	PIC_0_BUS_1[5]/ PIC_1_BUS_1[5]/ EIRQ3/ GPIO101		See Note 1.

X2 pin number	Type	Module functionality	Usage on Development Board	Comments
65	I/O	PIC_0_BUS_1[6]/ PIC_1_BUS_1[6]/ I2C_SCL (dup)/ GPIO102		4k7 pull-up on module
66	I/O	PIC_0_BUS_1[7]/ PIC_1_BUS_1[7]/ I2C_SDA (dup)/ GPIO103		4k7 pull-up on module
67	I	VIN0_ADC		
68	I	VIN1_ADC		
69	I	VIN2_ADC		
70	I	VIN3_ADC		
71	I	VIN4_ADC		
72	I	VIN5_ADC		
73	I	VIN6_ADC		
74	I	VIN7_ADC		
75	P	VSS_ADC		Connected on module to AGND through 0Ù resistor
76	P	VREF_ADC		100nF decoupling capacitor between VREF_ADC and VSS_ADC
77	P	3.3V		
78	P	3.3V		
79	P	GND		
80	P	GND		

Note1: For ConnectCore 3G 9P 9215, this pin is defined in the GPIO table of Appendix D: ConnectCore 3G 9P 9215 GPIO.

Note 2: For ConnectCore 3G 9P 9215, the following pins are outputs with fixed functionality:

X2-11: Cellular link activity output.

X2-12: Cellular 3G connectivity indicator.

X2-13: Cellular signal strength (1st bar).

X2-16: Cellular signal strength (2nd bar).

X2-18: Cellular signal strength (3rd bar).

These can be used to drive LEDs.

Configuration pins — CPU

None of the 64 GPIO pins on connector X2 disturb CPU boot strap functions. The boot strap functions are controlled by address signals; the user can not disturb boot strap functions from outside, if the module configuration signals, described below, are correctly configured.

Default module CPU configuration

The user has access to six configuration signals:

- LITTLE#/BIG_ ENDIAN which allows the user to select the endianess of the module
- OCD_EN# which allows the user to activate on-chip debugging
- SW_CONF [3:0] which are reserved for the user; the user software can read out these signals through the GEN ID register (@ 0xA090_0210).

Configuration pins — Module

The ConnectCore 9P 9215 family of modules support the following JTAG signals: TCK, TMS, TDI, TDO, TRST#, and RTCK. Selection can be made between ARM debug mode and boundary scan mode with the signal OCD_EN#.

Identification of the module

In order to make it easier for software to recognize a module and especially a hardware variant of the module, a specific bit field made of 4-bits has been reserved on the module. This bit field can be read out through GEN ID register and correspond to A[12:9]. These configuration signals use the internal CPU pull-up resistor and can be pulled down through external population option 2k2 resistors.

In the same way, 3 bits have been available on the module to identify the SDRAM configuration scheme. This bits correspond to A[19:17]. It is impossible for the user to disturb either the variant specific or SDRAM configuration specific bits from outside.

In Addition, the ConnectCore 9P 9215 family of modules have reserved 4 bits for special platform identification. This bit field can be read out through GEN ID register and correspond to A[16:13]. Configuration of these signals is done through the SW_CONF pins. SW_CONF0 is connected to A13 through a 2k2 series resistor, and so on for the further SW_CONF pins. So this bit can be set high by leaving the corresponding SW_CONF pin unconnected and set low by connecting the corresponding SW_CONF pin directly low.

These pins are available for user defined application or platform specific software configurations.

Note: For the ConnectCore 3G 9P 9215 module, these pins have a reserved usage described in Appendix C: ConnectCore 3G 9P 9215 Strapping on page 122.

Module pin configuration

Signal name	Function	PU/PD	Comment
LITTLE#/BIG_ ENDIAN	Set module endianess. 0 module boots in little endian mode. 1 module boots in big endian mode.	PU	Signal LITTLE#/BIG_ENDIAN is connected to GPIO_A3/A27 through a 2k2 series resistor.
OCD_EN#	JTAG / Boundary scan function select 0 ARM debug mode, BISTEN# set to high 1 Boundary scan mode, BISTEN# set to low	PU 10K	
SW_CONF0	See note 1.		Connected to A13 through a 2k2 series resistor. Read bit 4 of GEN ID register (@ 0xA0900210).

Signal name	Function	PU/PD	Comment
SW_CONF1	See note 1.		Connected to A14 through a 2k2 series resistor.Read bit 5 of GEN ID register (@ 0xA0900210).
SW_CONF2	See note 1.		Connected to A15 through a 2k2 series resistor. Read bit 6 of GEN ID register (@ 0xA0900210).
SW_CONF3	See note 1.		Connected to A16 through a 2k2 series resistor. Read bit 7 of GEN ID register (@ 0xA0900210).
Note 1:	For the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215: This pin is a user/application defined software configuration pin. For the ConnectCore 3G 9P 9215: This pin is described in Appendix C: ConnectCore 3G 9P 9215 Strapping on page 122.		

Clock generation

Clock frequencies

Hardware strapping determines the initial powerup PLL settings. The table below summarizes the default clock frequencies for the ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 modules:

Hardware strapping:

"PLL reference clock divider setting:
A[4:0] = 0x1D (0b11101)
NR = 5

"PLL output divider setting:
A[6:5] = 0x3 (0b11)
OD = 0

"PLL bypass setting:
A[7] = 0x1 (0b1)
Normal operation

PLL frequency formula:

PLL Vco = (RefClk / NR+1) * (NF+1)
ClkOut = PLL Vco / (OD+1)

RefClk (Crystal) = 29.4912MHz
NF = 0x3C (reset value - can only be changed by software).

PLL Vco = (29.4912 / 6) * 61 = 299.8272 MHz
ClkOut = 299.8272 MHz

Resulting clock settings:

PIC clock = 299.8272 MHz

CPU clock = 299.8272 MHz / 2 = 149.9136 MHz

AHB clock = 149.9136 MHz / 2 = 74.9568 MHz

Changing the CPU speed

After powerup, software can change the PLL settings by writing to the PLL configuration register (@ 0xA090_0188)

Important: When PLL parameters are changed, a reset is provided for the PLL to stabilize. Applications using this feature need to be aware the SDRAM contents will be lost. See reset behavior in the table below.

Reset Behavior	RESET _n pin	SRESET _n pin	PLL Config Reg. Update	Watchdog Time-Out Reset
SPI boot	YES	YES	YES	YES
Strapping PLL	YES	NO	NO	NO
Other strappings (Endianess)	YES	NO	NO	NO
GPIO configuration	YES	NO	NO	NO
Other (ASIC) registers	YES	YES	YES	YES
SDRAM keeps its contents	NO	YES	NO	YES

Boot process

The ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 modules boot directly from NOR flash. The start-up code is located at address 0x00000000 during the boot process. When the system is booted, the SDRAM is remapped to address 0x00000000 and NOR Flash to 0x50000000 by modifying the address map in the AHB decoder.

Chip selects

The module has eight chip selects: four for dynamic memory and four for static memory. Each chip select has a 256MB range.

Chip select memory map

Name	CPU Sig. name	Pin	Address range	Size [Mb]	Usage	Comments
SDM_CS0#	CS1#	D6	0x00000000–0x0FFFFFFF	256	SDRAM bank 0	First bank on module
SDM_CS1#	CS3#	B5	0x10000000–0x1FFFFFFF	256	not used	
SDM_CS2#	CS5#	A4	0x20000000–0x2FFFFFFF	256	not used	
SDM_CS3#	CS7#	B4	0x30000000–0x3FFFFFFF	256	not used	
EXT_CS0#	CS0#	C6	0x40000000–0x4FFFFFFF	256	external, CS0#	
INT_CS1#	CS2#	B6	0x50000000–0x5FFFFFFF	256	NOR-Flash	Program memory on module
EXT_CS2#	CS4#	C5	0x60000000–0x6FFFFFFF	256	external, CS2#	CC3G: internally used for USB controller
INT_CS3#	CS6#	A3	0x70000000–0x7FFFFFFF	256	internal, CS3#	Reserved for internal usage CC3G: NAND flash on module

SDRAM banks

ConnectCore 9P 9215 and ConnectCore Wi-9P 9215:

The modules provide connection to 1 SDRAM chip, connected to CS1# (SDM_CS0#). The other SDRAM chip selects are not used. The standard module has one of these SDRAM onboard: 1Mx16x4-banks. A13 is the highest address connected. BA0 and BA1 are connected to A21 and A22, respectively.

ConnectCore 3G 9P 9215:

The module provides connection to 1 SDRAM chip, connected to CS1# (SDM_CS0#). The other SDRAM chip selects are not used. The standard module has one of these SDRAM onboard: 2Mx32x4-banks. A14 is the highest address connected. BA0 and BA1 are connected to A22 and A23, respectively.

NAND Flash Memory

For the Connect Core 3G 9P 9215 module only, NAND Flash has been included. This is because extra memory was required to hold the GOBI cellular images, as well as the Python related files. This module contains a 128M x 8 NAND Flash with 2Kbyte page size. The NAND Flash is connected to INTCS3#, where A13 is used as the ALE and A14 is used as the CLE.

Multiplexed GPIO pins

ConnectCore 9P 9215 and ConnectCore Wi-9P 9215:

The 104 GPIOs pins (plus address bits A24 through A27) available on the module connector are multiplexed with other functions like:

- UART
- SPI
- Ethernet
- DMA
- I^2C port
- Timers and interrupt inputs
- Memory bus data

Pin notes

- GPIO [15:0] allow five multiplex modes.
- GPIO [103:16] and GPIO_A [3:0] have four multiplex modes.
- Using a pin as GPIO means always to give up other functionalities. Some functions are duplicated to enhance the chance to use them without giving up other vital functions.
- Using original and (dup) functions in parallel is not recommended.
- Default function of GPIOs after CPU power up is function 03, except GPIO12 (function 02-reset_done) and GPIO [31:16] (function 00 - DATA[15:0]).

GPIO multiplex table

In the GPIO multiplex table below,

- the default function is written bold,
- # means low active signal,
- (dup) means function is available multiple times.

Port name, Function 03	Alternate function 00	Alternate function 01	Alternate function 02	Alternate function 04 (only GPIO00...GPIO15)	On module, default used as
GPIO0	DCDA#	DMA0_DONE	PIC_0_GEN_IO[0]	SPI_EN# (dup)	DCDA# / SPI_EN#
GPIO1	CTSA#	EIRQ0	PIC_0_GEN_IO[1]	Reserved	CTSA#
GPIO2	DSRA#	EIRQ1	PIC_0_GEN_IO[2]	Reserved	DSRA#
GPIO3	RXDA#	DMA0_PDEN	PIC_0_GEN_IO[3]	SPI_RXD (dup)	RXDA / SPI_RXD
GPIO4	RIA#	EIRQ2	Timer6_In	SPI_CLK (dup)	RIA# / SPI_CLK
GPIO5	RTSA# / 485CTLA	EIRQ3	Timer6_Out	SPI_CLK (dup)	RTSA#
GPIO6	TXCLKA / DTRA#	DMA0_REQ	Timer7_In	PIC_DBG_DATA_OUT	DTRA#
GPIO7	TXDA	Timer8_In	Timer7_Out	SPI_TXD (dup)	TXDA / SPI_TXD
GPIO8	DCDC# / TXCLKC	DMA1_DONE	Timer8_Out	SPI_EN# (dup)	DCDC#
GPIO9	CTSC#	I2C_SCL	EIRQ0 (dup)	PIC_DBG_DATA_IN	CTSC#
GPIO10	DSRC#	QDCI	EIRQ1 (dup)	PIC_DBG_CLK	DSRC#
GPIO11	RXDC#	DMA1_PDEN	EIRQ2 (dup)	SPI_RXD (boot)	RXDC
GPIO12	RXCLKC / RIC#	I2C_SDA	RESET_DONE	SPI_CLK (dup)	RIC# [1]
GPIO13	RXCLKC / RTSC# /485CTLC	QDCQ	Timer9_out	SPI_CLK (boot)	RXCLKC / RTSC#
GPIO14	TXCLKC / DTRC#	DMA1_REQ	PIC_0_CAN_RXD	SPI_TXD (boot)	TXCLKC
GPIO15	TXDC	Timer9_In	PIC_0_CAN_TXD	SPI_EN# (boot)	TXDC
GPIO16	D0	DCDB#	EIRQ0 (dup)		Reserved for upper data lines

Port name, Function 03	Alternate function 00	Alternate function 01	Alternate function 02	Alternate function 04 (only GPIO00...GPIO15)	On module, default used as
GPIO17	D1	CTSB#	EIRQ1 (dup)		Reserved for upper data lines
GPIO18	D2	DSRB#	EIRQ2 (dup)		Reserved for upper data lines
GPIO19	D3	RXDB	EIRQ3 (dup)		Reserved for upper data lines
GPIO20	D4	RIB#	DMA0_DONE (dup)		Reserved for upper data lines
GPIO21	D5	RTSB# / 485CTLB	DMA0_PDEN (dup)		Reserved for upper data lines
GPIO22	D6	TXCLKB / DTRB#	DMA1_DONE (dup)		Reserved for upper data lines
GPIO23	D7	TXDB	PIC_1_CAN_RXD		Reserved for upper data lines
GPIO24	D8	DCDD#	PIC_1_CAN_TXD		Reserved for upper data lines
GPIO25	D9	CTSD#	RESET_DONE (dup)		Reserved for upper data lines
GPIO26	D10	DSRD#	PIC_1_GEN_IO[0]		Reserved for upper data lines
GPIO27	D11	RXDD	PIC_1_GEN_IO[1]		Reserved for upper data lines
GPIO28	D12	RID#	PIC_1_GEN_IO[2]		Reserved for upper data lines
GPIO29	D13	RTSD# / 485CTLD	PIC_1_GEN_IO[3]		Reserved for upper data lines
GPIO30	D14	TXCLKD / DTRD#	Reserved		Reserved for upper data lines
GPIO31	D15	TXDD	Reserved		Reserved for upper data lines
GPIO32	MII_MDC	PIC_0_GEN_IO[0]	Reserved		MII Interface
GPIO33	MII_TXC	PIC_0_GEN_IO[1]	Reserved		MII Interface
GPIO34	MII_RXC	PIC_0_GEN_IO[2]	Reserved		MII Interface
GPIO35	MII_MDIO	PIC_0_GEN_IO[3]	Reserved		MII Interface
GPIO36	MII_RXDV	PIC_0_GEN_IO[4]	Reserved		MII Interface
GPIO37	MII_RXER	PIC_0_GEN_IO[5]	Reserved		MII Interface
GPIO38	MII_RXD0	PIC_0_GEN_IO[6]	Reserved		MII Interface

Port name, Function 03	Alternate function 00	Alternate function 01	Alternate function 02	Alternate function 04 (only GPIO00...GPIO15)	On module, default used as
GPIO39	MII_RXD1	PIC_0_GEN_IO[7]	Reserved		MII Interface
GPIO40	MII_RXD2	PIC_1_GEN_IO[0]	Reserved		MII Interface
GPIO41	MII_RXD3	PIC_1_GEN_IO[1]	Reserved		MII Interface
GPIO42	MII_TXEN	PIC_1_GEN_IO[2]	Reserved		MII Interface
GPIO43	MII_TXER	PIC_1_GEN_IO[3]	Reserved		MII Interface
GPIO44	MII_TXD0	PIC_1_GEN_IO[4]	Reserved		MII Interface
GPIO45	MII_TXD1	PIC_1_GEN_IO[5]	Reserved		MII Interface
GPIO46	MII_TXD2	PIC_1_GEN_IO[6]	Reserved		MII Interface
GPIO47	MII_TXD3	PIC_1_GEN_IO[7]	Reserved		MII Interface
GPIO48	MII_COL	Reserved	Reserved		MII Interface
GPIO49	MII_CRS	Reserved	Reserved		MII Interface
GPIO50	MII_PHY_Int	PIC_1_CLK (I)	PIC_1_CLK(0)		MII Interface
GPIO51	DCDB# (dup)	PIC_0_BUS_1[8]	PIC_1_BUS_1[8]		DCDB#
GPIO52	CTSB# (dup)	PIC_0_BUS_1[9]	PIC_1_BUS_1[9]		CTSB#
GPIO53	DSRB# (dup)	PIC_0_BUS_1[10]	PIC_1_BUS_1[10]		DSRB#
GPIO54	RXDB (dup)	PIC_0_BUS_1[11]	PIC_1_BUS_1[11]		RXDB
GPIO55	RIB# (dup)	PIC_0_BUS_1[12]	PIC_1_BUS_1[12]		RIB#
GPIO56	RTSB# / 485CTLB (dup)	PIC_0_BUS_1[13]	PIC_1_BUS_1[13]		RTSB#
GPIO57	TXCLKB (dup) / DTRB# (dup)	PIC_0_BUS_1[14]	PIC_1_BUS_1[14]		DTRB#
GPIO58	TXDB (dup)	PIC_0_BUS_1[15]	PIC_1_BUS_1[15]		TXDB
GPIO59	DCDD# (dup)	PIC_0_BUS_1[16]	PIC_1_BUS_1[16]		DCDD#
GPIO60	CTSD# (dup)	PIC_0_BUS_1[17]	PIC_1_BUS_1[17]		CTSD#
GPIO61	DSRD# (dup)	PIC_0_BUS_1[18]	PIC_1_BUS_1[18]		DSRD#
GPIO62	RXDD (dup)	PIC_0_BUS_1[19]	PIC_1_BUS_1[19]		RXDD
GPIO63	RID# (dup)	PIC_0_BUS_1[20]	PIC_1_BUS_1[20]		RID#
GPIO64	RTSD# / 485CTLD (dup)	PIC_0_BUS_1[21]	PIC_1_BUS_1[21]		RTSD#
GPIO65	TXCLKD (dup) / DTRD# (dup)	PIC_0_BUS_1[22]	PIC_1_BUS_1[22]		DTRD#
GPIO66	TXDD (dup)	PIC_0_BUS_1[23]	PIC_1_BUS_1[23]		TXDD
GPIO67	PIC_0_CLK (I)	PIC_0_CLK (O)	EIRQ3 (dup)		PIC_0_CLK

Port name, Function 03	Alternate function 00	Alternate function 01	Alternate function 02	Alternate function 04 (only GPIO00...GPIO15)	On module, default used as
GPIO68	PIC_0_GEN_IO[0]	PIC_1_GEN_IO[0]	PIC_1_CAN_RXD		PIC_0_GEN_IO[0]
GPIO69	PIC_0_GEN_IO[1]	PIC_1_GEN_IO[1]	PIC_1_CAN_TXD		PIC_0_GEN_IO[1]
GPIO70	PIC_0_GEN_IO[2]	PIC_1_GEN_IO[2]	PWM0		PIC_0_GEN_IO[2]
GPIO71	PIC_0_GEN_IO[3]	PIC_1_GEN_IO[3]	PWM1		PIC_0_GEN_IO[3]
GPIO72	PIC_0_GEN_IO[4]	PIC_1_GEN_IO[4]	PWM2		PIC_0_GEN_IO[4]
GPIO73	PIC_0_GEN_IO[5]	PIC_1_GEN_IO[5]	PWM3		PIC_0_GEN_IO[5]
GPIO74	PIC_0_GEN_IO[6]	PIC_1_GEN_IO[6]	Timer0_In		PIC_0_GEN_IO[6]
GPIO75	PIC_0_GEN_IO[7]	PIC_1_GEN_IO[7]	Timer1_In		PIC_0_GEN_IO[7]
GPIO76	PIC_0_CTL_IO[0]	PIC_1_CTL_IO[0]	Timer2_In		PIC_0_CTL_IO[0]
GPIO77	PIC_0_CTL_IO[1]	PIC_1_CTL_IO[1]	Timer3_In		PIC_0_CTL_IO[1]
GPIO78	PIC_0_CTL_IO[2]	PIC_1_CTL_IO[2]	Timer4_In		PIC_0_CTL_IO[2]
GPIO79	PIC_0_CTL_IO[3]	PIC_1_CTL_IO[3]	Timer5_In		PIC_0_CTL_IO[3]
GPIO80	PIC_0_BUS_0[0]	PIC_1_BUS_0[0]	Timer6_In (dup)		Timer6_In
GPIO81	PIC_0_BUS_0[1]	PIC_1_BUS_0[1]	Timer7_In (dup)		Timer7_In
GPIO82	PIC_0_BUS_0[2]	PIC_1_BUS_0[2]	Timer8_In (dup)		Timer8_In
GPIO83	PIC_0_BUS_0[3]	PIC_1_BUS_0[3]	Timer9_In (dup)		Timer9_In
GPIO84	PIC_0_BUS_0[4]	PIC_1_BUS_0[4]	Timer0_Out		Timer0_Out
GPIO85	PIC_0_BUS_0[5]	PIC_1_BUS_0[5]	Timer1_Out		Timer1_Out
GPIO86	PIC_0_BUS_0[6]	PIC_1_BUS_0[6]	Timer2_Out		Timer2_Out
GPIO87	PIC_0_BUS_0[7]	PIC_1_BUS_0[7]	Timer3_Out		Timer3_Out
GPIO88	PIC_0_BUS_0[8]	PIC_1_BUS_0[8]	Timer4_Out		User LED 0 => LED 1 (on module)
GPIO89	PIC_0_BUS_0[9]	PIC_1_BUS_0[9]	Timer5_Out		User LED 1 => LED 2 (on module)
GPIO90	PIC_0_BUS_0[10]	PIC_1_BUS_0[10]	Timer6_Out (dup)		GPIO reserved on module
GPIO91	PIC_0_BUS_0[11]	PIC_1_BUS_0[11]	Timer7_Out (dup)		Reserved NAND_R/B#
GPIO92	PIC_0_BUS_0[12]	PIC_1_BUS_0[12]	Timer8_Out (dup)		GPIO reserved on module
GPIO93	PIC_0_BUS_0[13]	PIC_1_BUS_0[13]	Timer9_Out (dup)		Timer9_Out
GPIO94	PIC_0_BUS_0[14]	PIC_1_BUS_0[14]	QDCI (dup)		QDCI
GPIO95	PIC_0_BUS_0[15]	PIC_1_BUS_0[15]	QDCQ (dup)		QDCQ
GPIO96	PIC_0_BUS_1[0]	PIC_1_BUS_1[0]	PIC_0_CAN_RXD		PIC_0_CAN_RXD

Port name, Function 03	Alternate function 00	Alternate function 01	Alternate function 02	Alternate function 04 (only GPIO00...GPIO15)	On module, default used as
GPIO97	PIC_0_BUS_1[1]	PIC_1_BUS_1[1]	PIC_0_CAN_TXD		PIC_0_CAN_TXD
GPIO98	PIC_0_BUS_1[2]	PIC_1_BUS_1[2]	PIC_1_CAN_RXD		PIC_1_CAN_RXD
GPIO99	PIC_0_BUS_1[3]	PIC_1_BUS_1[3]	PIC_1_CAN_TXD		PIC_1_CAN_TXD
GPIO100	PIC_0_BUS_1[4]	PIC_1_BUS_1[4]	PWM4		PWM4
GPIO101	PIC_0_BUS_1[5]	PIC_1_BUS_1[5]	EIRQ3		EIRQ3
GPIO102	PIC_0_BUS_1[6]	PIC_1_BUS_1[6]	I2C_SCL (dup)		I2C_SCL
GPIO103	PIC_0_BUS_1[7]	PIC_1_BUS_1[7]	I2C_SDA (dup)		I2C_SDA
GPIO_A0	A24	I2C_SCL dupe	EIRQ0 (dup)		Reserved EIRQ0
GPIO_A1	A25	I2C_SDA dupe	EIRQ1 (dup)		Reserved EIRQ1 - USB
GPIO_A2	A26	CS0_WE#	EIRQ2 (dup)		GPIO reserved on module
GPIO_A3	A27	CS0_OE#	UART_REFCLK		Little/Big Endian

[1] Put a series resistor on the baseboard in this case to avoid input/output conflict between RESET_DONE (output/boot default) and RIC# (input/configuration default).

ConnectCore 3G 9P 9215:

The 42 GPIOs pins available on the module connector are multiplexed with other functions like:

- UART
- XBEE

For GPIO multiplexing details, see Appendix D: ConnectCore 3G 9P 9215 GPIO.

Module LEDs

The ConnectCore 9P 9215 family of modules have two on module LEDs: LE1 and LE2. For each module variant, the default use varies:

- **ConnectCore 9P 9215:** LE1 will flash a repeating blink pattern in a major system failure; for ecample, a processor execption or power on self test failure.
- **ConnectCore Wi-9P 9215:** To indicate WLAN-related information, such as association status and network activity.
- **ConnectCore 3G 9P 9315:** LE2 will flash a repeating blink pattern in a major system failure; for example, a processor exception or power on self test failure. LE1 is available for programming.

ConnectCore 9P 9215 LEDs

ID	Connects to	Default	Description
LE1	GPIO88	Off	Setting to output logic “0” turns on the LED.
LE2	GPIO89	Off	Setting to output logic “0” turns on the LED.

ConnectCore Wi-9P 9215 LEDs

ID	Color	LED	Blink pattern	Status / Activity
LE1	Green	Link integrity	On	The unit is associated to an access point (infrastructure mode)
			Slow	The unit is in ad-hoc mode
			Quick	The unit is scanning for a network
LE2	Yellow	Network activity	Blinking	Network traffic is received or transmitted
			Off	Network is idle

Note: The network activity LED is used for diagnostic purposes during boot-up.

ConnectCore 3G 9P 9215 LEDs

ID	Connects to	Default	Description
LE1	GPIO88	Off	Available at the Python programming layer, via the user_led_set() function.
LE2	GPIO89	Off	For use as a diagnostic..

External interrupts

The ConnectCore 9P 9215 family of modules provide access to four external interrupts signals, which are multiplexed with other functions on the GPIO pins. Every interrupt is multiplexed to two or three different GPIO pins. These duplicate signals are marked as *(dup)* in the GPIO table.

External interrupt	GPIO multiplexing	Other functions, 1st position	Comments
EIRQ0	GPIO1 GPIO9	X2.4 X2.12	
EIRQ1	GPIO2 GPIO10	X2.5 X2.13	
EIRQ2	GPIO4 GPIO11	X2.7 X2.14	
EIRQ3	GPIO5 GPIO67 GPIO101	X2.8 X2.35 X2.64	EIRQ3# is used on the Development Board to implement I²C I/O expander interrupt functionality.

Interfaces

10/100 Mbps Ethernet port

The Digi NS9215 processor's 10/100 Mbps Ethernet MAC allows a glueless connection of a 3.3V MII PHY chip that generates the physical Ethernet signals.

The module has a MII PHY chip in a 56-pin QFN package on board. By default, the module does not have a transformer or Ethernet connector; the base board must provide these parts. However, it's possible to populate a specific RJ45 connector with magnetics on the module. The appropriate RJ-45 is Midcom MIC2412A-5108W-LF3.

A PHY clock of 25 MHz is generated in the PHY chip with a 25 MHz crystal.

GPIO90 is controlling the PHY RESET# signal. This GPIO has a 2k2 pull-down resistor to GND populated on the module. GPIO90 must be asserted high before PHY can be used. When not used, the PHY can be put in low-power mode by asserting GPIO90 low.

The PHY address on the MII bus is 0x7 (0b00111).

The module does not only provide access to the Ethernet signals coming out of the PHY, but supports also two status LEDs: ETH_ACTIVITY# and ETH_LINK#.

UART

The ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules provide up to four UART ports, the ConnectCore 3G 9P 9215 module provides up to three UART ports, used in asynchronous mode:

- Port A = GPIOO through GPIO7
- Port B = GPIO51 through GPIO58
- Port C = GPIO8 through GPIO15 (Not available on the ConnectCore 3G 9P 9215)
- Port D = GPIO59 through GPIO66

The module supports baud rates up to 1.8432 Mbps in asynchronous mode. Each UART has a 64-byte TX and RX FIFO available.

SPI

The following interfaces are only available on the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215.

The module provides one SPI port which can be used in either master or slave mode.

- Master: 33.33 Mbps
- Slave: 7.50 Mbps

The SPI module is made of four signals: RXD, TXD, CLK and CS#

I²C bus

The I²C bus is completely free on the module - no EEPROM and no RTC - since the RTC is in the processor.

The I²C clock is max 400kHz.

I2C signals are provided on the module with 4k7 pull-up resistors.

RTC

The RTC is integrated in the processor and has its own 32.768 KHz clock crystal.

- When powered by VBAT, RTC unit will function until VBAT (X1.78) reaches a threshold of 2.3 - 2.4V - then the internal unit switches off.
- The battery current without +3.3V power applied is up to 40µA. The current is used to power the RTC, 32.768kHz oscillator and 64-byte internal RAM.
- When the Development Board ships from the factory the battery is disabled. To enable the battery, place a jumper on the Development Board at J2.

WLAN

In addition to the wired Ethernet interface, the ConnectCore Wi-9P 9215 module also offers an integrated dual-diversity 802.11a/b/g interface with data rates up to 54 Mbps. Two U.FL antenna connectors are provided on the module.

WWAN

The ConnectCore 3G 9P 9215 offers 3G connection technologies by using the Qualcomm Gobi PCIe module.

ADC

The ADC on the module provides 12-bit resolution / 1 MHz conversion capabilities, single-ended 8:1 multiplexed inputs, rail-to-rail input range, 12-bit output (DMA/direct), and external reference.

FIM

The Flexible Interface Modules (FIM) are based on two independent 8-bit DRPIC1655X cores running at 300 MHz maximum core clock (4x NS9215 bus speed) with 192-byte data and 2 KB program SRAM. The FIMs allow the flexible software-based selection of

Digi-provided application specific hardware interfaces such as UART, SD/SDIO, 1-Wire, CAN bus, and others.

External Address/Data Bus

The modules provide a 17-bit address and 16-bit data bus with 2 external chip selects for peripheral connections.

Antenna

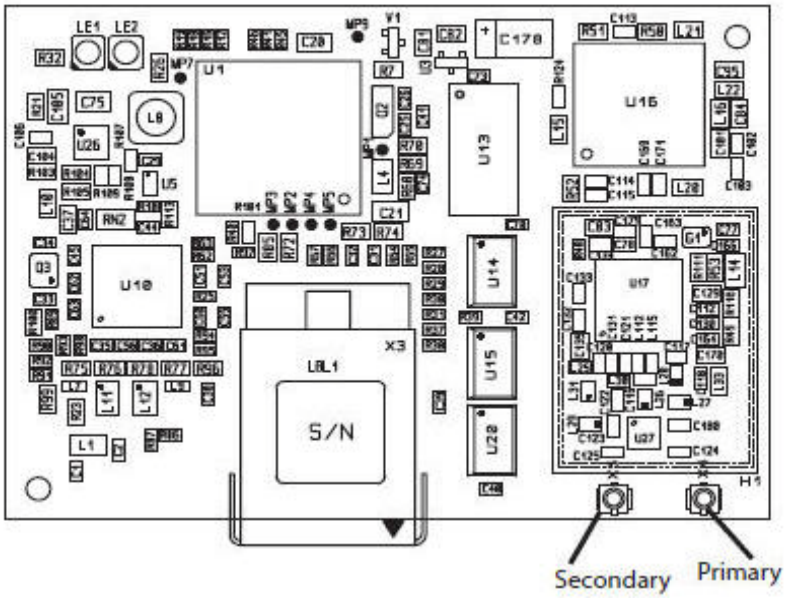
Note: When disconnecting U.FL connectors, the use of U.FL plug extraction tool (Hirose P/N U.FL-LP-N-2 or U.FL-LP(V)-N-2) is strongly recommended to avoid damage to the U.FL connectors on the ConnectCore Wi-9P 9215 and ConnectCore 3G 9P 9215 modules.

To mate U.FL connectors, the mating axes of both connectors must be aligned. The "click" will confirm fully mated connection.

Do not attempt insertion at an extreme angle.

ConnectCore Wi-9P 9215 WLAN:

ConnectCore Wi-9P 9215 Module



For the ConnectCore Wi-9P 9215, connect antennas to the primary and secondary connectors.

The module uses the same antennas to transmit and receive the 802.11b/g RF signal. An antenna switch is required to isolate the transmit signal from the receive signal. The antenna switch works by alternately connecting the antennas to either the transceiver PA transmit output or the transceiver receive input. To support this antenna sharing scheme, the module operates in half-duplex mode; receive and transmit operations do not occur at the same time.

WLAN Antenna Switch

The antenna switch is a digitally controlled 2.4 GHz, 50 ohm, multi-function solid state switch, controlled by software.

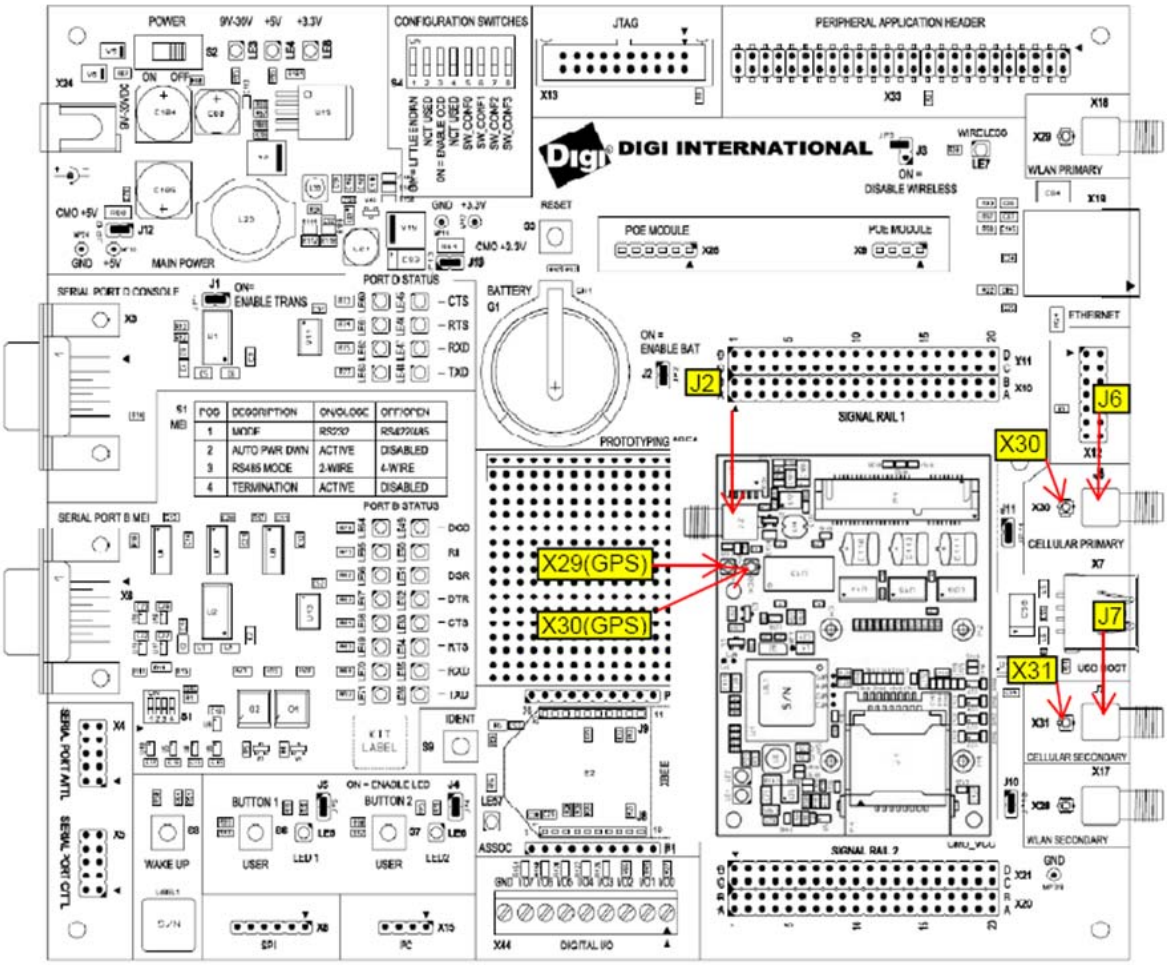
The receive port can be switched between antenna 1 or antenna 2.

The transmit port can be switched between antenna 1 or antenna 2.

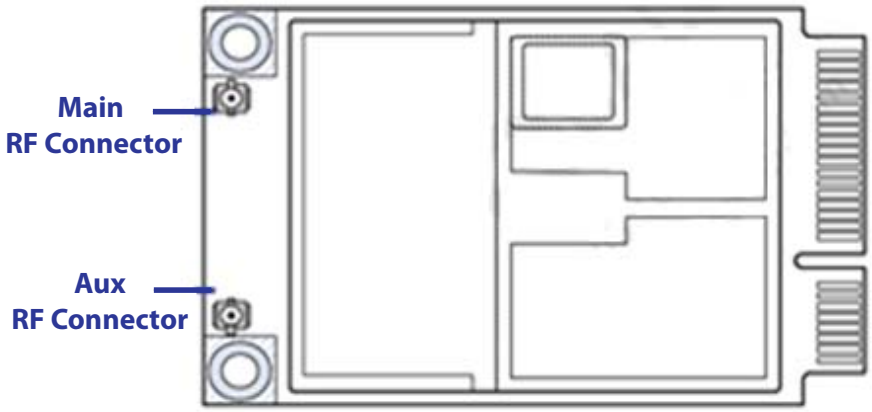
The switch can handle >28dBm of signal on the transmit port. The insertion loss of the antenna switch is <0.5dB and the receive to transmit port isolation is >23dB.

ConnectCore 3G 9P 9215 WWAN:

ConnectCore 3G 9P 9215 Module and Development Board



Gobi 2000 Module



The connect Core 3G 9P 9215 Development board and module contains several RF connectors, as well as the two connectors located on the Gobi 2000 module (refer to the above diagrams.)

Cellular RF Path: The cellular RF path is established when the Gobi 2000 module MAIN connector is cabled to the Development board X30 connector, along with a cellular antenna connected to the Cellular Primary connector J6. Alternatively, the Gobi 2000 MAIN connector could be cabled directly to the back of the module's J2 connector, with a cellular antenna connected to J2. (Note the latter is how the module is certified and any deviation from this configuration will require re-certification.)

GPS RF Path: The GPS RF path has two possible configurations, based on the GPS antenna: Active and Passive.

When using an active GPS antenna, the Gobi 2000 module AUX connector is cabled to the module X30 connector, and the module X29 connector is cabled to the Development board Cellular Secondary connector X31. When an Active GPS antenna is connected to development board at J7, GPS traffic is then available to the module.

Alternatively, the Gobi 2000 AUX connector could be cabled directly to the Development board Cellular Secondary connector X31, with a passive GPS antenna connected at J7.

Power

Power supply

The module has +3.3V and VLIO supply pins.

VLIO can be connected either to a Li-Ion battery (2.5V - 5.5V) in a mobile application, or it can be connected directly to +3.3V. Connecting VLIO to a battery causes efficiency to be gained without an additional voltage regulator.

Internal voltage

The internal 1.8V core voltage is generated through a high-efficiency synchronous step-down converter, which uses VLIO as input voltage. The core voltage regulator can provide up to 600mA.

About the Development Board

CHAPTER 2

The ConnectCore 9P 9215 Development Board supports the ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 modules. This chapter describes the components of the Development Board and explains how to configure the board for your requirements.

The Development Board has two 4x20 pin connectors that are 1:1 copies of the module pins.

What's on the Development Board?

- RJ-45 Ethernet connector
- Four RP-SMA antenna connectors.
  - Connection to module via U.FL connectors
- Four serial interface connectors:
  - 1 x UART B MEI (RS232/RS4xx) with status LEDs on SUB-D 9-pin connector (X6)
  - 1 x UART D RS232 with status LEDs, on SUB-D 9-pin connector (X3)
  - 1 x UART C with TTL levels shared with HDLC signals on 10-pin header (X5)
  - 1 x UART A with TTL levels shared with SPI signals on 10-pin header (X4)
- ADC, SPI, and I^2C headers
- Socket for XBee module
- JTAG connector
- Peripheral application header
  - Including access to 16-bit data/10-bit address bus signals
- Headers with 1:1 copies of the module pins (X1/X2)
- Two user pushbuttons, two user LEDs, wake-up button

- Eight-position configuration dip switches

Four each for hardware/software configuration

  - GPIO screw-flange connector
  - +9/30VDC power supply

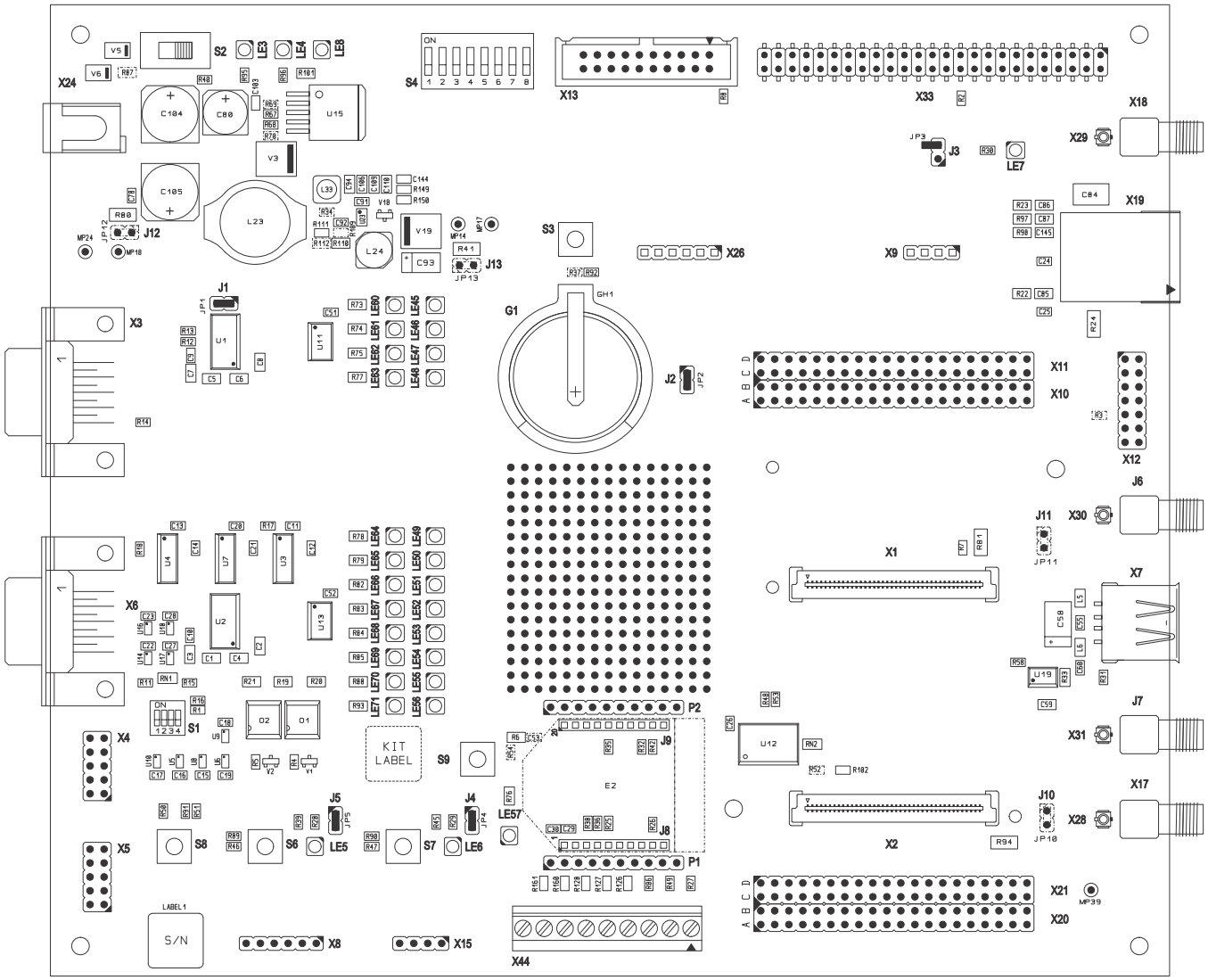
Current measurement option

  - Development Board + module, and module alone
  - 3.3V coincell battery with socket
  - PoE connectors for optional 802.3af PoE Application Kit (P/N DG-ACC-POE)
  - Prototyping area (15 x 28 holes) with +3.3V and GND connections

ConnectCore 3G 9P 9215 only:

- USB host connector
- 2 x SMA antenna connectors for cellular/GPS antennas
  - Connection to module via U.FL connectors

ConnectCore 9P 9215 Development Board



User interface

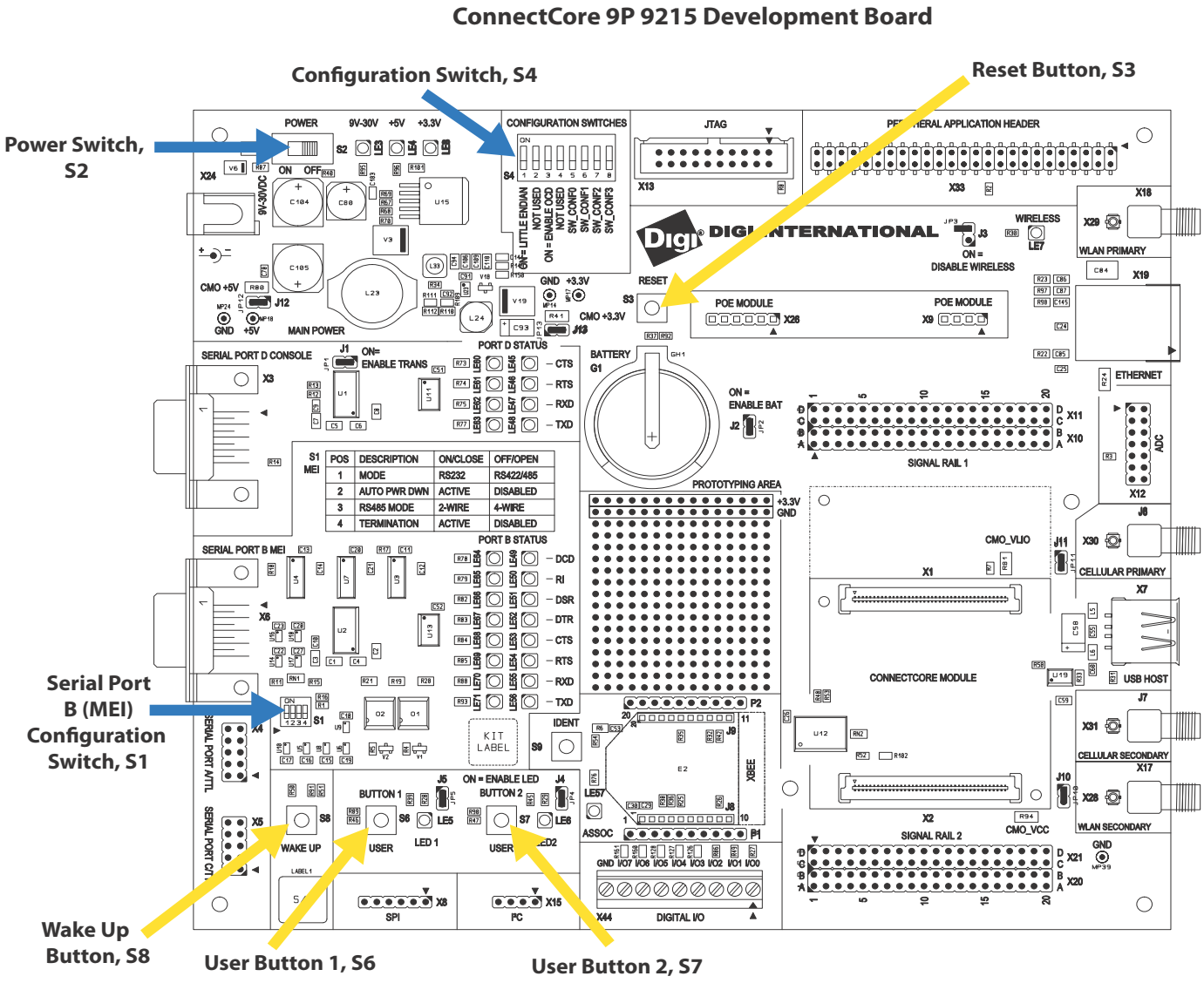
The ConnectCore 9P 9215 Development Board implements two user buttons and two user LEDs in addition to those provided on the module.

The user LEDs on the Development Board can be enabled or disabled by population option jumper J4 & J5.

The table below shows which NS9215 GPIO is available for implementing the user interface.

Signal name	GPIO used	Commetns
USER_BUTTON1	GPIO81	10k pull-up to +3.3V on the Development Board
USER_LED1#	GPIO82	Remove jumper J5 to isolate (and disable) LED
USER_BUTTON2	GPIO84	10k pull-up to +3.3V on the Development Board
USER_LED2#	GPIO85	Remove jumper J4 to isolate (and disable) LED

Switches and Pushbuttons



Reset control, S3

The reset pushbutton, S3, resets the module. On the module, RSTOUT# and PWRGOOD are produced for peripherals. A pushbutton allows manual reset by connecting RSTIN# to ground.

Power switch, S2

The Development Board has an ON/OFF switch, S2. The power switch S2 can switch both 9V-30V input power supply and 12V coming out of the PoE module. However, if a power plug is connected in the DC power jack, the PoE module is disabled.

User pushbuttons, S6 and S7

Use the user pushbuttons to interact with the applications running on the ConnectCore 9P 9215, ConnectCore Wi-9P 9215 and ConnectCore 3G 9P 9215 modules. Use these module signals to implement the pushbuttons:

Signal name	Switch (pushbutton)	GPIO used
USER_PUSH_BUTTON_1	S6	GPIO81
USER_PUSH_BUTTON_2	S7	GPIO84

Note: For the ConnectCore 3G 9P 9215, User Button 1 has reserved functionality. A quick button press causes a soft reset. Holding the button at Power Up for 20 seconds and then releasing will factory default the module.

Legend for multi-pin switches

Switches 1 and 4 are multi-pin switches. In the description tables for these switches, the pin is designated as *S[switch number].[pin number]*. For example, pin 1 in switch 4 is specified as S4.1.

Module configuration switches, S4

Use S4 to configure the module:

Switch pin	Function
S4.1	On = Little endian Off = Big endian
S4.2	Not used
S4.3	On = ARM Debug Off = Boundary Scan
S4.4	Not used
S4.5 – S4.8	ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 - Not defined. Used for application configuration settings. ConnectCore 3G 9P 9215 - See Appendix C: ConnectCore 3G 9P 9215 Strapping on page 122 for information on the S4 SW_CONF settings.

Note: When running Linux based applications, always select Little Endian. All other applications must use Big Endian. Failure to do so will prevent your board from running or booting.

Wake-up button, S8

The wake-up pushbutton, S8, generates an external interrupt to the module's NS9215 processor using the EIRQ2 signal.

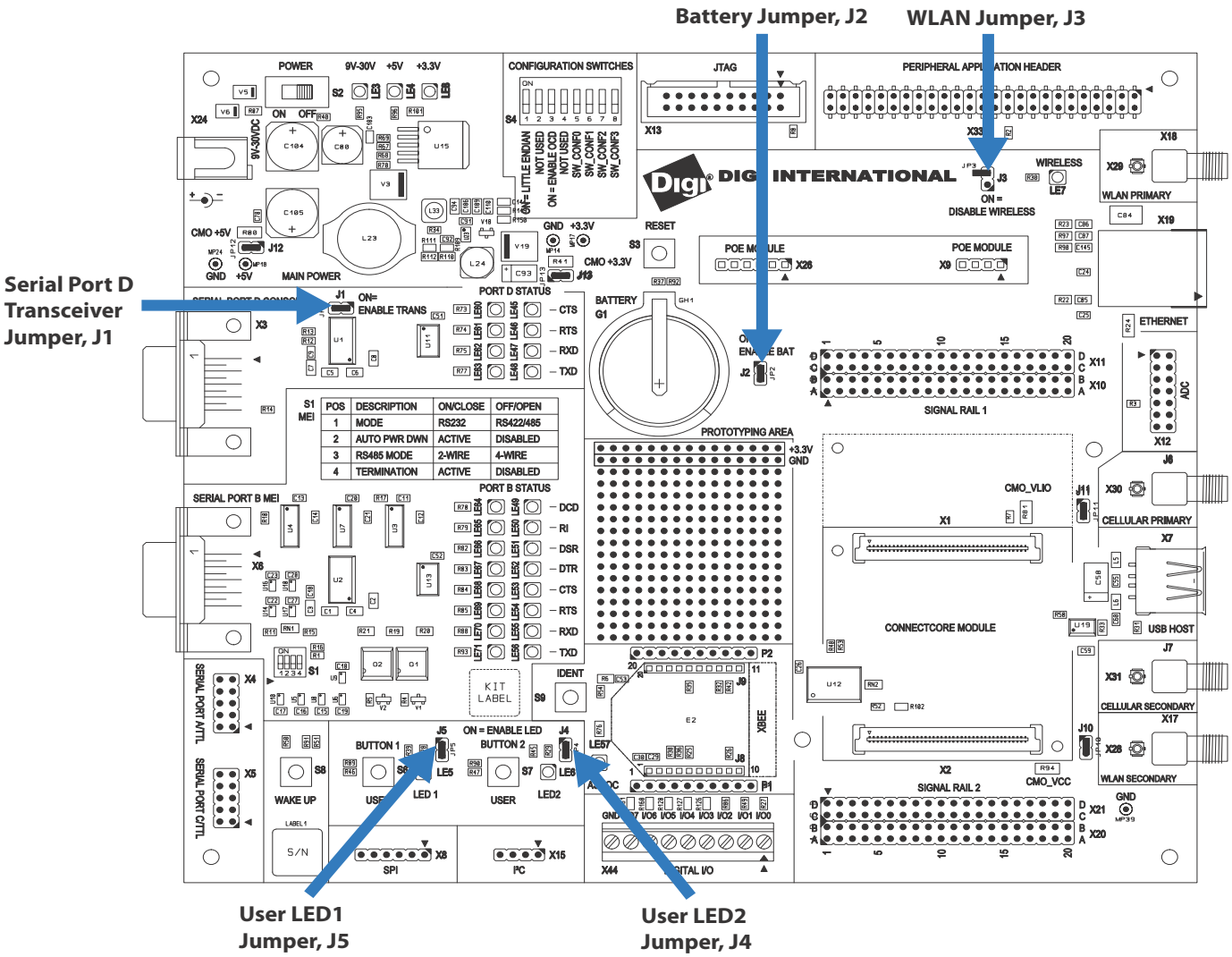
Serial Port B MEI configuration switches, S1

Use S1 to configure the line interface for serial port B MEI:

Switch pin	Function	Comments
S1.1	On = RS232 transceiver enabled RS422/RS485 transceivers disabled Off = RS232 transceiver disabled RS422/RS485 transceivers enabled	
S1.2	On = Auto Power Down enabled Off = Auto Power Down disabled	Auto Power Down is not supported on this board. This signal is only accessible to permit the user to completely disabled the MEI interface for using the signals for other purposes. To disable the MEI interface, go in RS232 mode (S1.1 = ON) and activate the Auto Power Down feature (S1.2 = ON) - be sure that no cable is connected to connector X3.
S1.3	On = 2-wire interface (RS422/RS485) Off = 4-wire interface (RS422)	
S1.4	On = Termination on Off = No termination	

Jumpers

ConnectCore 9P 9215 Development Board



Jumper functions

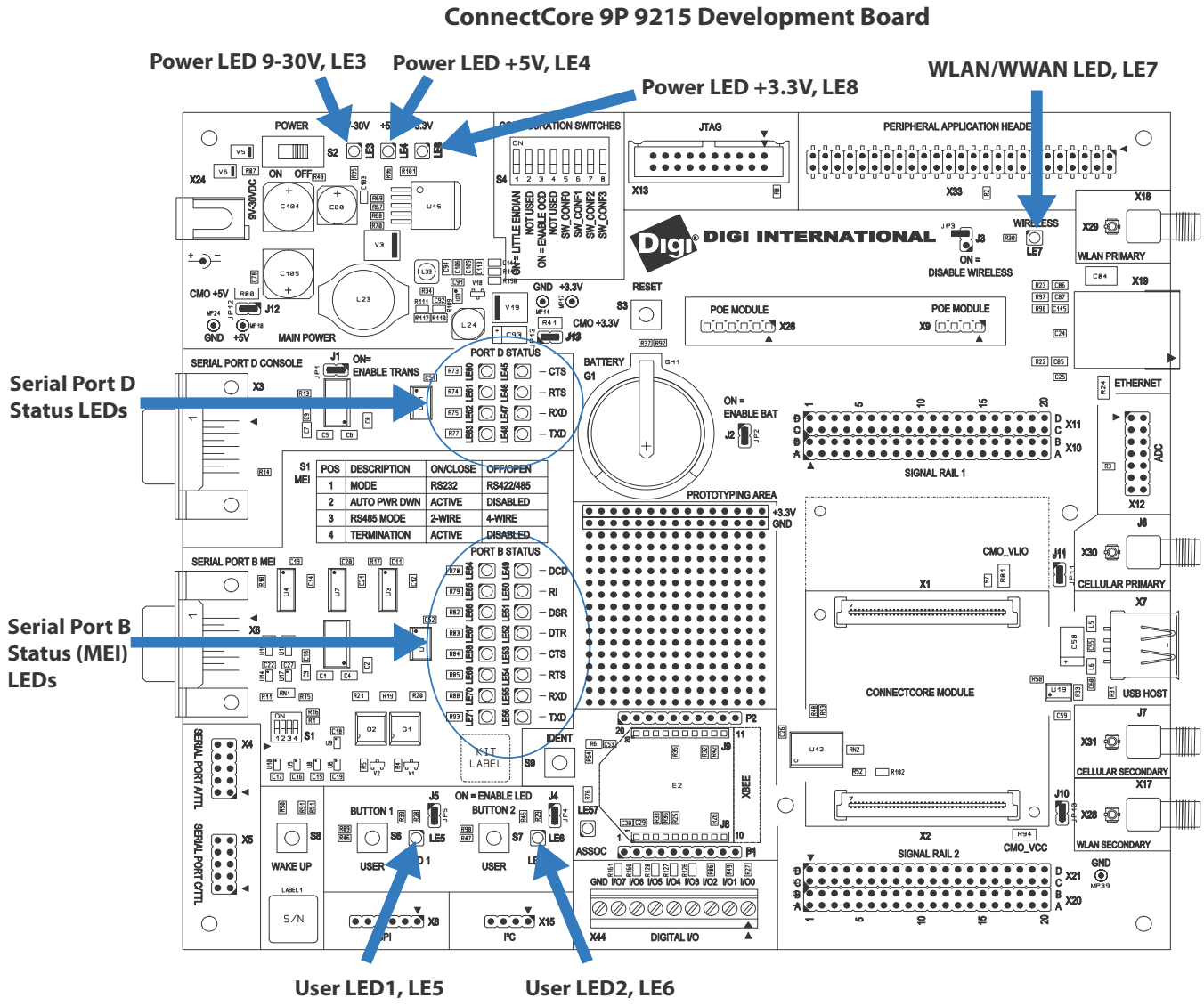
Jumper	Name	If connection made	Default
J1	Enable transceiver	This jumper allows to disable the console RS232 transceiver.	Connection made = console active
J2	Battery enable	Supplies the real time clock with 3V from the battery (lithium coin cell battery, G1) even if the board is switched off. This is for keeping time in the RTC.	Connection not made = Backup battery disabled
J3	WLAN_DISABLE#	Disables the WiFi unit on the module. ConnectCore 3G 9P 9215 - Disabled the WWAN (directly connected to the PCIe connector pin 20)	Connection made = WLAN disabled
J4	USER_LED2#	Enables User LED2 (LE6) to show the status of this signal (lit if low).	Connection made = User LED2 enabled
J5	USER_LED1#	Enables User LED1 (LE5) to show the status of this signal (lit if low).	Connection made = User LED1 enabled

Note: The User LEDs are specific to the ConnectCore 3G 9P 9215 module:
USER_LED2 - indicated GPS lock
USER_LED1 - available through the Python GPIO API

Battery and Battery Holder

Battery Holder	Battery
Coin-Cell Holder for CR2477 Battery, THT	Lithium coin cell, CR2477, 24mm, 950mAh
Keystone 1025-7	Panasonic CR2477
Ettinger 15.61.252	Renata CR2477N

LEDs



WLAN LED LE7

LED indicating WLAN activity.

ConnectCore 3G 9P 9215 - LED indicating WWAN activity (directly connected to the PCIe connector pin 42).

Power LEDs, LE3 and LE4

The power LEDs are all red LEDs. These power supplies must be present and cannot be switched.

- LE3 ON indicates the +9VDC / +30VDC power is present.
- LE4 ON indicates the +5VDC power is present.
- LE8 ON indicates the +3.3VDC power is present.

User LEDs, LE5 and LE6

The user LEDs are controlled through applications running on the ConnectCore 9P 9215 family of modules, if jumpers J5 and J4 are inserted. Use these module signals to implement the LEDs:

Signal name	LED	GPIO used
USER_LED1#	LE5	GPIO82
USER_LED2#	LE6	GPIO85

Note: On the ConnectCore 3G 9P 9215 USER_LED2 is reserved for the GPS lock indication.

Serial status LEDs

The Development Board has two sets of serial port LEDs — four for serial port D and eight for serial port B. The LEDs are connected to the TTL side of the RS232 or RS422/485 transceivers.

- Green means corresponding signal high.
- Red means corresponding signal low.
- The intensity and color of the LED will change when the voltage is switching.

Status LEDs Serial Port D LEDs

LED reference		Function
RED	GREEN	
LE60	LE45	CTSD#/GPIO60
LE61	LE46	RTSD#/GPIO64
LE62	LE47	RXDD/GPIO62
LE63	LE48	TXDD/GPIO66

Status LEDs Serial Port B LEDs

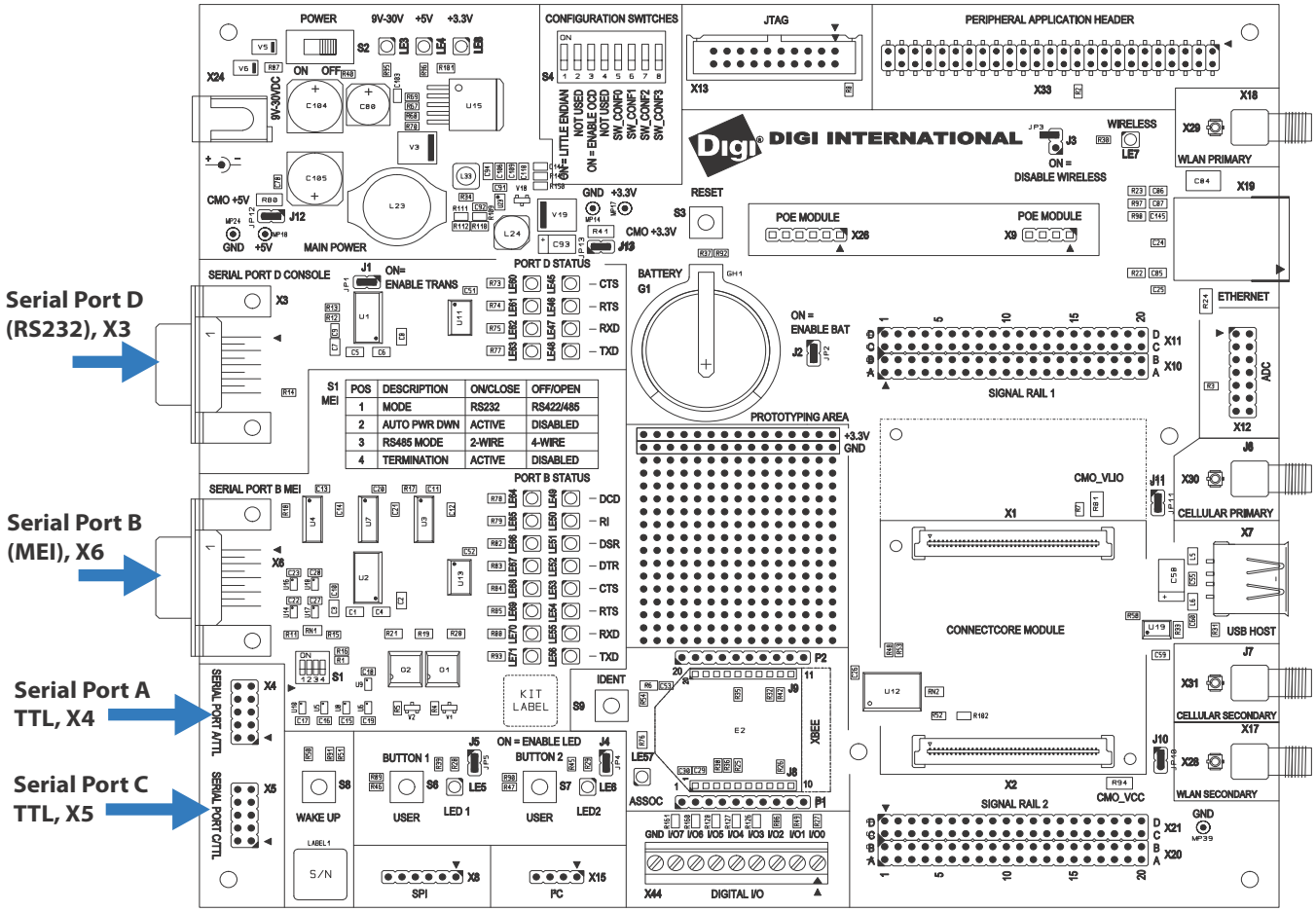
LED reference		Function
RED	GREEN	
LE64	LE49	DCDB#/GPIO51
LE65	LE50	RIB#/GPIO55
LE66	LE51	DSRB#/GPIO53
LE67	LE52	DTRB#/GPIO57
LE68	LE53	CTSB#/GPIO52
LE69	LE54	RTSB#/GPIO56
LE70	LE55	RXDB/GPIO54
LE71	LE56	TXDB/GPIO58

Note: For more information please see the ConnectCore 9P 9215 schematics document online.

Serial UART Ports

The Development Board supports the four serial ports available on the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules, including the three serial ports available on the Connect Core 3G 9P 9215. (ConnectCore 9P 9215 Port C is not available on the Connect Core 3G 9P 9215.)

ConnectCore 9P 9215 Development Board



Serial port D, RS232

The serial (UART) port D connector, X3, is a DSUB9 male connector and is also used as the standard console. This asynchronous serial port is DTE and requires a null-modem cable to connect to a computer serial port.

The serial port D interface corresponds to NS9215 UART port D. The line driver is enabled or disabled using the jumper J1.

Serial port D pins are allocated as shown:

Pin	Function	Defaults to
1	DCD#	GPIO59
2	RXD	GPIO62
3	TXD	GPIO66
4	DTR#	GPIO65
5	GND	
6	DSR#	GPIO61
7	RTS#	GPIO64
8	CTS#	GPIO60
9	RIB#	GPIO63

By default, Serial D signals are configured to their respective GPIO signals.

It isthe responsibility of the driver to configure them properly.

Serial port A TTL interface

The serial (UART) port A interface is a TTL interface connected to a 2x5 pin, 0.1" connector, X4. The connector supports only TTL level.

The serial port A interface corresponds to NS9215 UART port A.

Serial port A pins are allocated as shown:

Pin	Function	Defaults to	Comment
1	DCDA#/SPI_EN#	GPIO0	Can be programmed as SPI enable to X4
2	DSRA#	GPIO2	
3	RXDA/SPI_RXD	GPIO3	Can be programmed as SPI receive data to X4
4	RTSA#/SPI_CLK	GPIO5	Can be programmed as SPI clock to X4
5	TXDA/SPI_TXD	GPIO7	Can be programmed as SPI transmit data to X4
6	CTSA#	GPIO1	
7	DTRA#	GPIO6	
8	RIA#/EIRQ2	GPIO4	This signal is default configured to support the wake-up button on the Development Board..

Pin	Function	Defaults to	Comment
9	GND		
10	3.3V		

By default, Serial A signals are configured to their respective GPIO signals. It is the responsibility of the driver to configure them properly.

Serial Port A must not be connected if SPI, WakeUp, or XBee module functionality is used.

Serialport A, XBee socket

The XBee socket consists of two separate connectors J8 and J9. The XBee pinning counts counter clock wise, so pin 1 of J9 is pin 20 of the module. All pins are connected 1:1 to a pin row to enable the usage of unconnected pins.

Pin	Function	Defaults to	Comments
1	VCC		Onboard 3.3V
2	RXDA/SPI_RXD/GPIO3	GPIO3	Can be programmed as SPI receive data to X4
3	TXDA/SPI_TXD/GPIO7	GPIO7	Can be programmed as SPI transmit data to X4
4	NC		
5	DSRA#/GPIO2/XBEE_RESET#	GPIO2	
6	NC		
7	NC		
8	NC		
9	DTRA#/GPIO6/SLEEP_RQ	GPIO6	
10	GND		
11	NC		
12	CTSA#/	GPIO1	
13	DCDA#/SPI_EN#/GPIO0	GPIO0	Can be programmed as SPI enable to X4
14	XBEE_ON_SLEEP#		Low is sleep
15	NC		
16	ASSOC	ASSOC	LED output of XBEE module (LE57 on dev-board)
17	RTSA#/SPI_CLK/GPIO5	GPIO5	Can be programmed as SPI clock on X4
18	NC		
19	NC		
20	NC		
21	IDNET	IDENT	Connected to S9 on dev-board

Serial port C TTL interface

The serial (UART) port C interface is a TTL interface connected to a 2x5 pin, 0.1" connector, X5. The connector supports only TTL level.

The serial port C interface corresponds to the NS9215 UART port C. The signals are shared with the HDLC interface.

Serial port C pins are allocated as shown:

Pin	Function	Defaults to	Comments
1	DCDC#/TXCLKC	GPIO8.	
2	DSRC#	GPIO10.	
3	RXDC#	GPIO11	CC3G: RXDC# internally used
4	RTSC#/RXCLKC	GPIO13	
5	TXDC	GPIO15	
6	CTSC#	GPIO9	
7	DTRC#/TXCLKC	GPIO14	CC3G: TXCLKC internally used
8	RIC#/RXCLKC/GPIO 12	RESET_DONE See note	
9	GND		
10	3.3V		

Note: Port C is not available on the ConnectCore 3G 9P 9215.

By using GPIO12 as RIC#, be sure to populate a series resistor on the baseboard. This is necessary to avoid conflict between the default configuration of the GPIO when booting (RESET_DONE / output) and the chosen configuration once booted (RIC# / input).

By default, Serial C signals are configured to their respective GPIO signals, except for GPIO12. It is the responsibility of the driver to configure them properly.

Serial port B, MEI interface

The serial (UART) port B connector, X6, is a DSUB9 male connector. This asynchronous serial port is DTE and requires a null-modem cable to connect to a computer serial port.

The serial port B MEI (Multiple Electrical Interface) interface corresponds to NS9215 UART port B. The line drivers are configured using switch S1.

Note that all pins on S1 contribute to the line driver settings for this port.

Serial port B pins are allocated as shown:

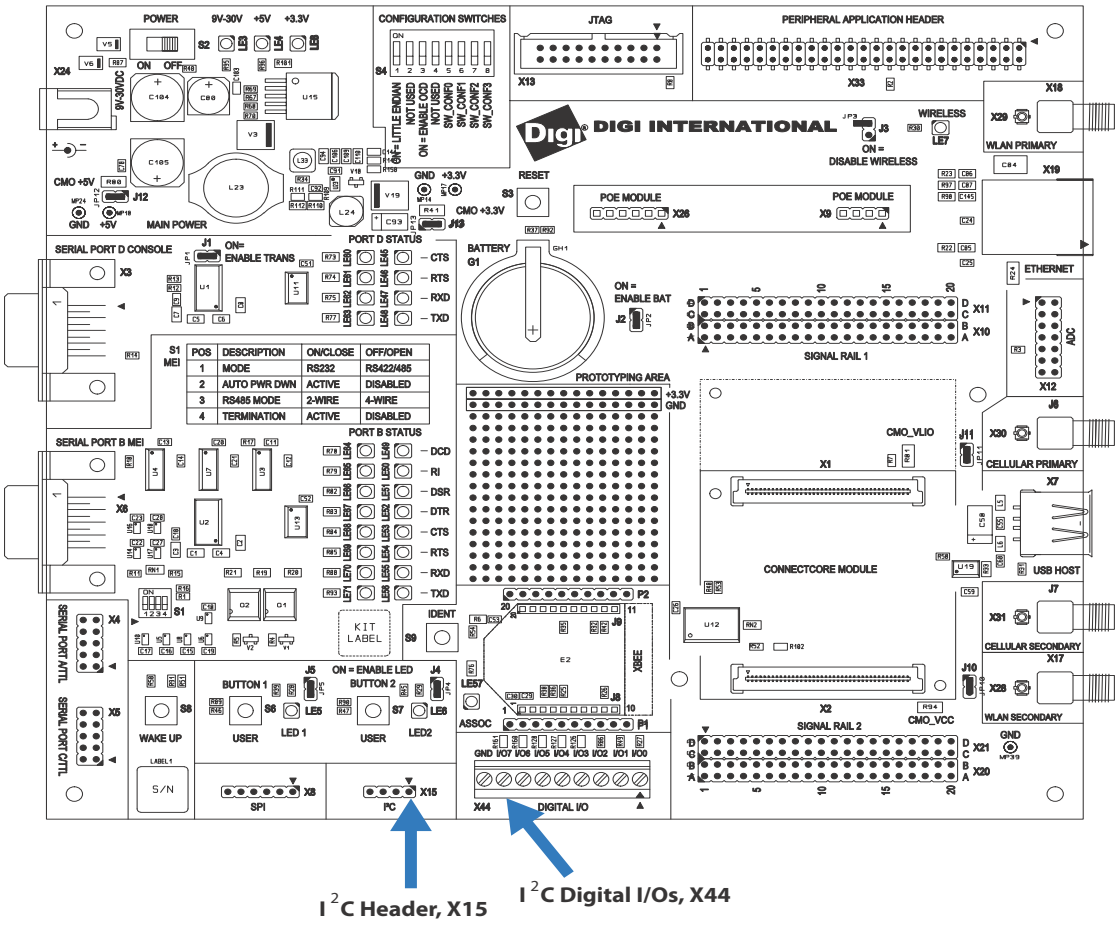
Pin	RS232 fucntion	RS232 default	RS485 function	RS485 default
1	DCD#	GPIO51	CTS-	n/a
2	RXD	GPIO54	RX+	GPIO54
3	TXD	GPIO58	TX+	GPIO58
4	DTR#	GPIO57	RTS-	n/a
5	GND		GND	
6	DSR#	GPIO53	RX-	n/a
7	RTS#	GPIO56	RTS+	GPIO56
8	CTS#	GPIO52	CTS+	GPIO52
9	RI#	GPIO55	TX-	n/a

By default, Serial B signals are configured to their respective GPIO signals.

It is the responsibility of the driver to configure them properly.

I²C Interface

ConnectCore 9P 9215 Development Board



I²C header

The I²C interface has only one device connected to the bus on the Development Board - an I/O expander (see next paragraph). Otherwise, additional I²C devices (like EEPROMs) can be connected to the module by using I²C header X15. The pinning of this header is provided below.

Pin	Signal
1	I2C_SDA/GPIO103
2	+3.3V
3	I2C_SCL/GPIO102
4	GND

I²C digital I/O expansion

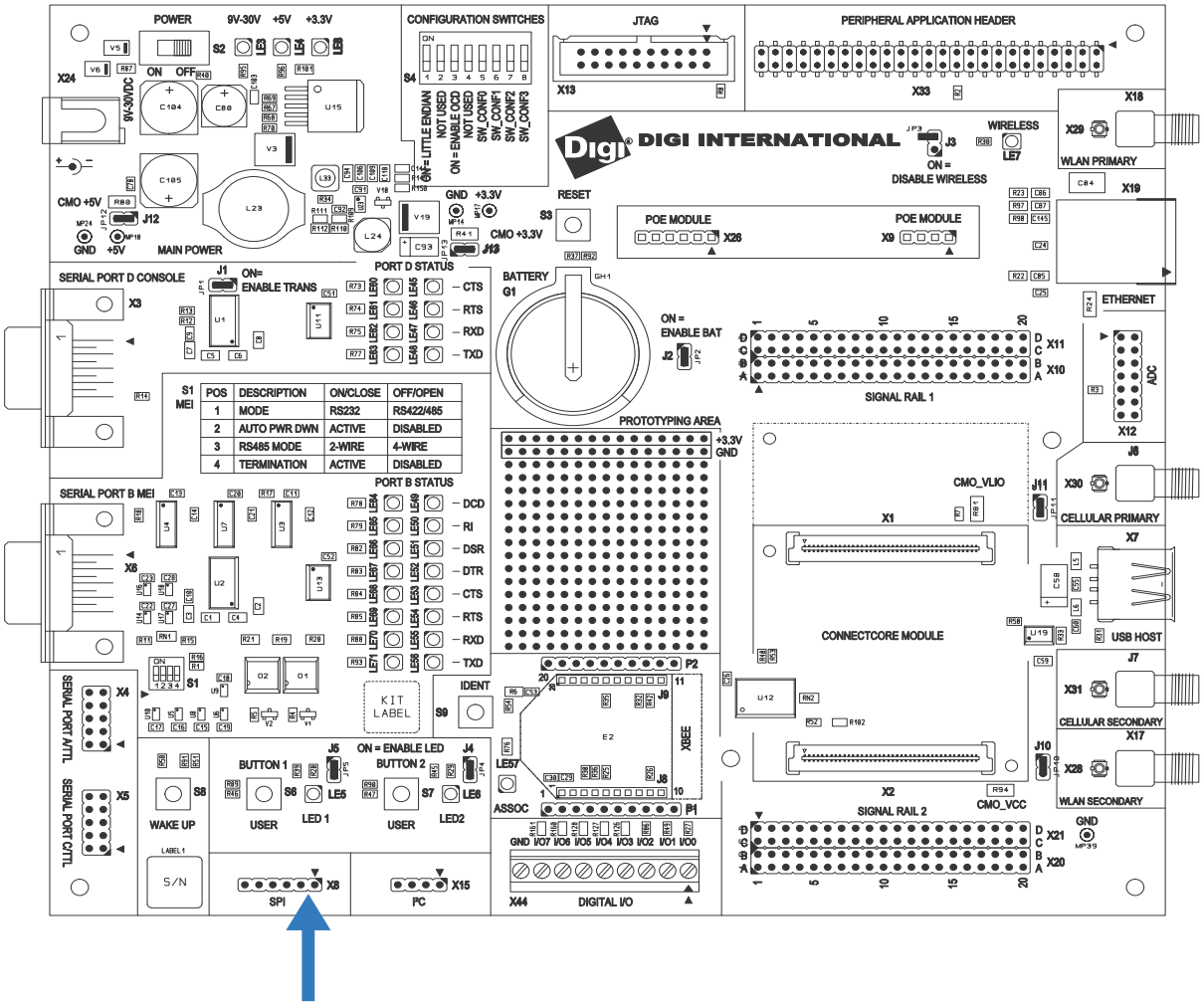
The Development Board provides a 3.81mm (1.50") green terminal block, X44, for additional digital I/Os. The I²C I/O port chip is on-chip ESD-protected, and provides an open drain interrupt output.

The I/O expander is a Philips PCA9554D at I²C address 0x20 / 0x21. The pins are allocated as shown:

Pin	Signal
1	IO_0
2	IO_1
3	IO_2
4	IO_3
5	IO_4
6	IO_5
7	IO_6
8	IO_7
9	GND

SPI interface

ConnectCore 9P 9215 Development Board



SPI Header, X8

The Development Board provides access to the SPI interface on the module using the SPI connector, X8. The SPI interface on the Development Board is shared with UART_A (NS9215 port A). Because the module's SPI interface is shared with a UART interface, you cannot use both simultaneously.

Note: The default configuration of UART port A is to support GPIOs. To move from GPIO to UART or SPI, you need to configure the software properly.

Pin allocation

SPI connector pins are allocated as shown:

Pin	Signal
1	+3.3V
2	TXDA/SPI_TXD/GPIO7
3	RXDA/SPI_RXD/GPIO3
4	RTSA#/SPI_CLK/GPIO5
5	DCDA#/SPI_EN#/GPIO0
6	GND

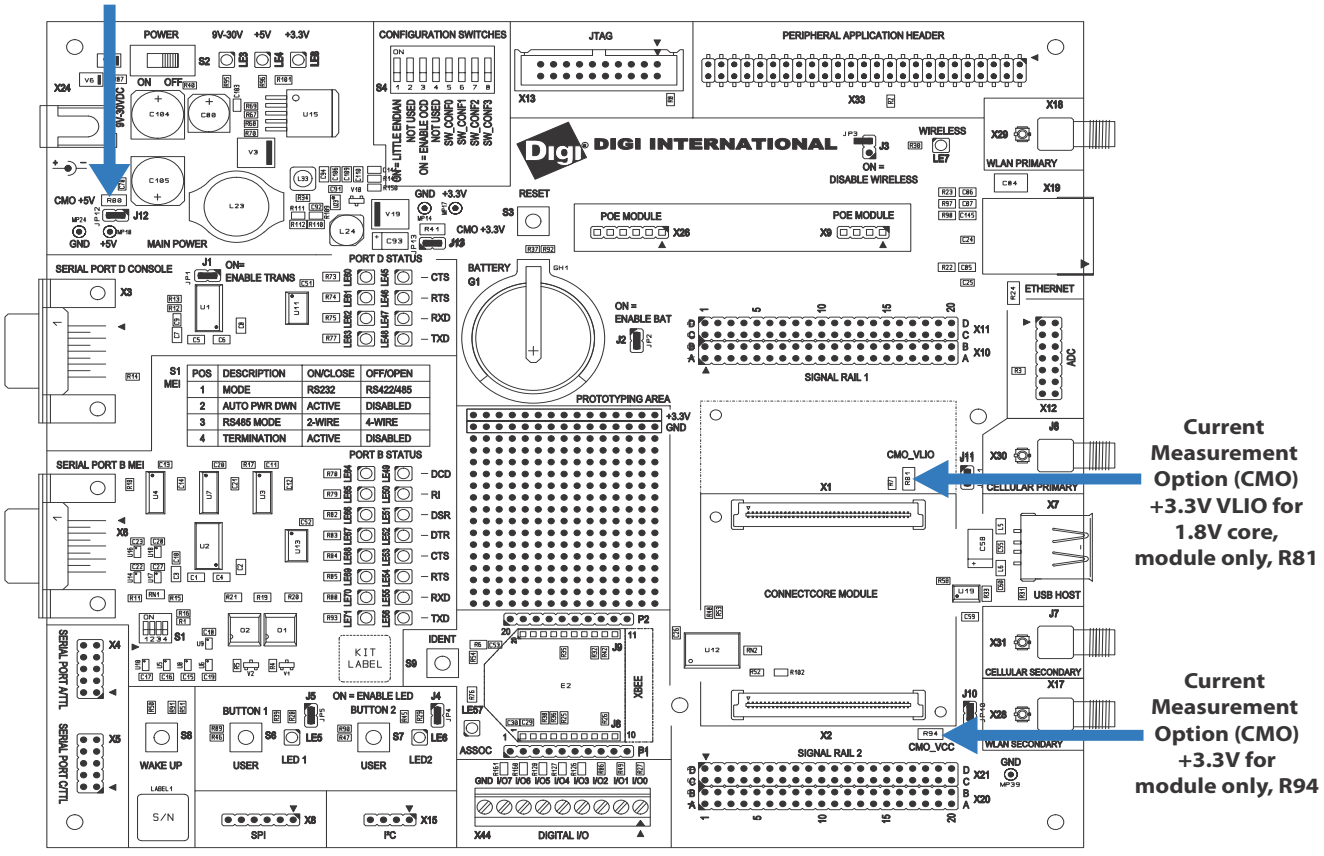
Current Measurement Option

The Current Measurement Option uses 0.025R ohm series resistors to measure the current. The ConnectCore 9P 9215 Development Board allows to measure:

- the current used by the Development Board and module (through R80), and
- the current used by the internal NS9215 1.8V core generated from VLIO using a high-efficiency synchronous step-down converter (through R81)

ConnectCore 9P 9215 Development Board

Current Measurement Option (CMO) +3.3V development board and module, R80



How the CMO works

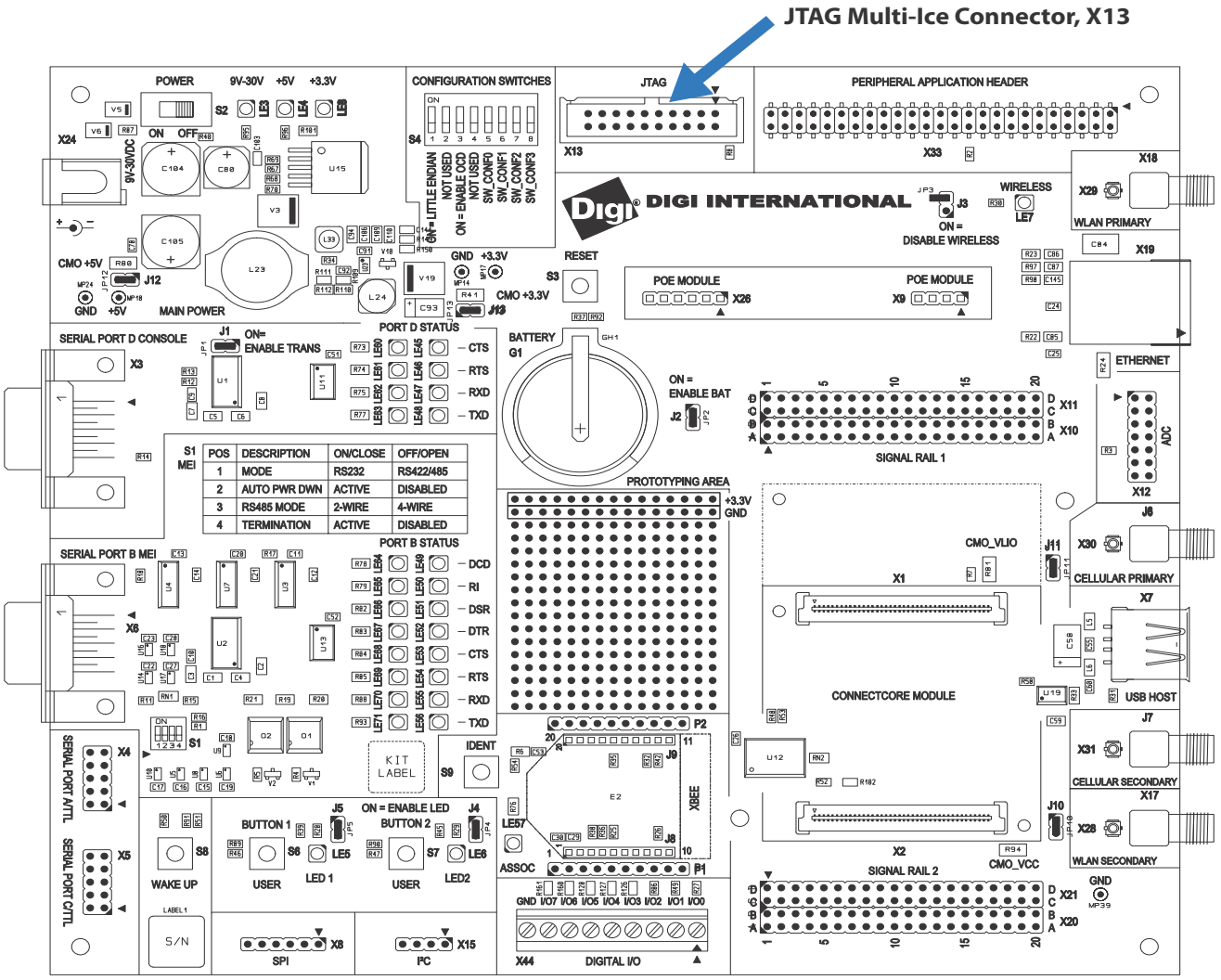
To measure the load current used on different power supplies, measure DC voltage across the sense (CMO) resistor. The value of the resistor is 0.025R ± 1%. Calculate the current using this equation: $I = U/R$

where

- I = current in Amps
- U = measured voltage in Volts
- R = 0.025 Ohms

JTAG Interface

ConnectCore 9P 9215 Development Board



Standard JTAG ARM connector, X13

The standard JTAG ARM connector is a 20-pin header and can be used to connect development tools such as Digi's JTAG Link, ARM's Multi-ICE, Abatron BDI2000, and others.

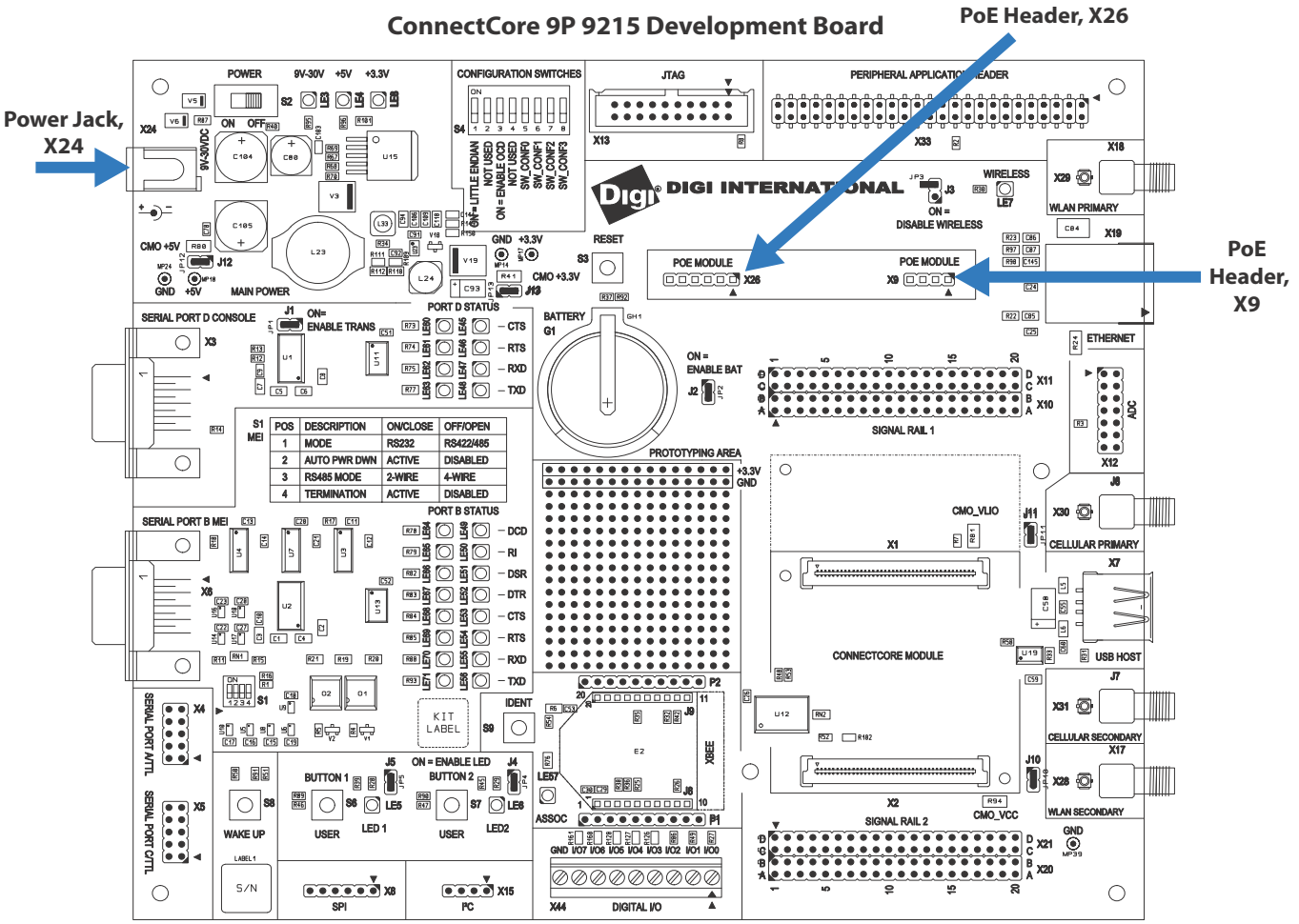
Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	TRST#	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	RTCK (optional)	12	GND
13	TDO	14	GND
15	SRESET#	16	GND
17	No connect	18	GND
19	No connect	20	GND

PoE module connectors - IEEE802.3af

The Development Board has two PoE module connectors, X9 and X26. The PoE module is an optional accessory item that can be plugged on the Development Board through the two connectors:

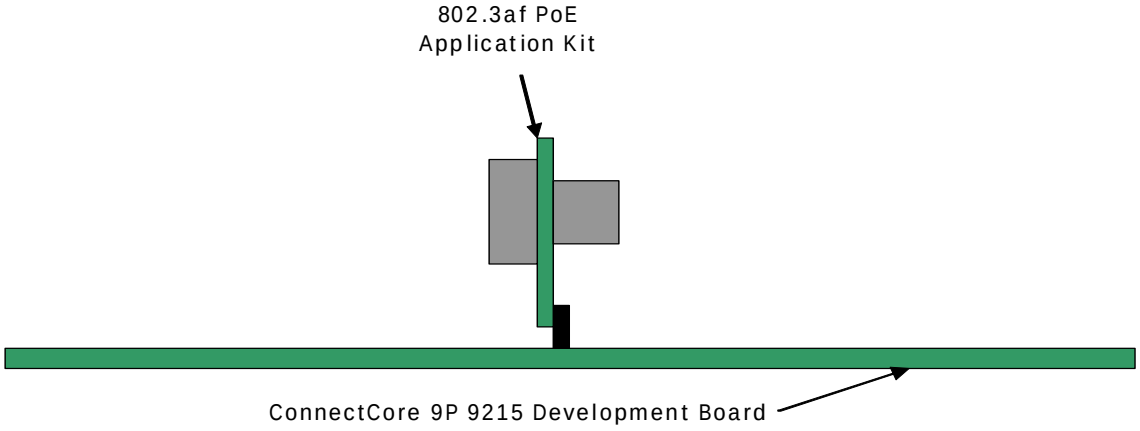
- X9, input connector: Provides access to the PoE signals coming from the Ethernet interface.
- X26, output connector: Provides the output power supply from the PoE module.

Note: The PoE interface is only available for the ConnectCore 9P 9215 module.



The 802.3af PoE Application Kit

Plug in the 802.3af PoE Application Kit (P/N DG-ACC-POE) at a right angle to the Development Board, as shown in this drawing:



X9

This is how the PoE input connector pins are allocated:

Pin	Signal
1	POE_TX_CT
2	POE_RX_CT
3	POE_RJ45_4/5
4	POE_RJ45_7/8

X26

This is how the PoE output connector pins are allocated:

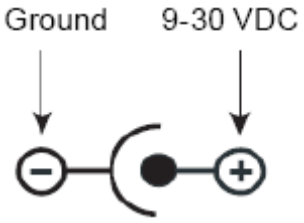
Pin	Signal
1	+12V_PoE
2	+12V_PoE
3	GND
4	GND
5	PoE_GND
6	PoE_GND

POE_GND

The Development Board provides access to POE_GND allowing it to be turned off when power is provided through Power Jack X26.4 and X26.5.

Power Jack, X24

The power jack is a barrel connector with 9-30VDC operating range. The power jack is labeled X24 on the Development Board. This figure schematically represents the power jack's polarity.

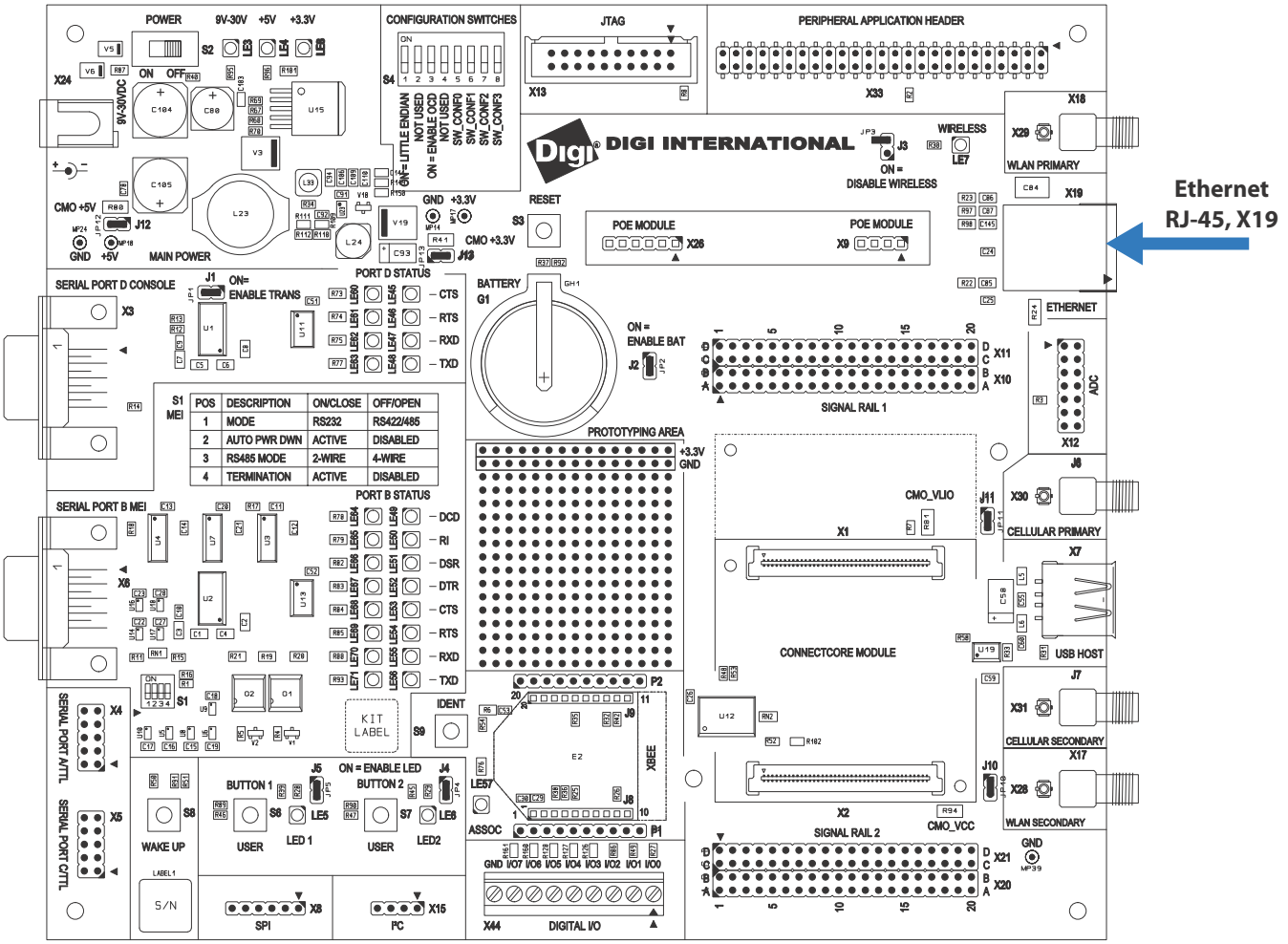


Ethernet Interface

The module provides the 10/100 Ethernet PHY chip. The Development Board provides the 1:1 transformer and Ethernet connector.

The Ethernet connector is an 8-wire RJ-45 jack, labeled X19, on the Development Board. The connector has eight interface pins, as well as two integrated LEDs that provide link status and network activity information.

ConnectCore 9P 9215 Development Board



RJ-45 pin allocation, X19

RJ-45 connector pins are configured as shown:

Pin	Signal	802.3af End-Span (mode A)	802.3af Mid-Span (Mode B)	Description
1	TXD+	Negative V_{Port}		Transmit data +
2	TXD-	Negative V_{Port}		Transmit data -
3	RXD+	Positive V_{Port}		Receive data +
4	EPWR+		Positive V_{Port}	Power from switch +
5	EPWR+		Positive V_{Port}	Power from switch +
6	RXD-	Positive V_{Port}		Receive data -
7	EPWR-		Negative V_{Port}	Power from switch -
8	EPWR-		Negative V_{Port}	Power from switch -

LEDs

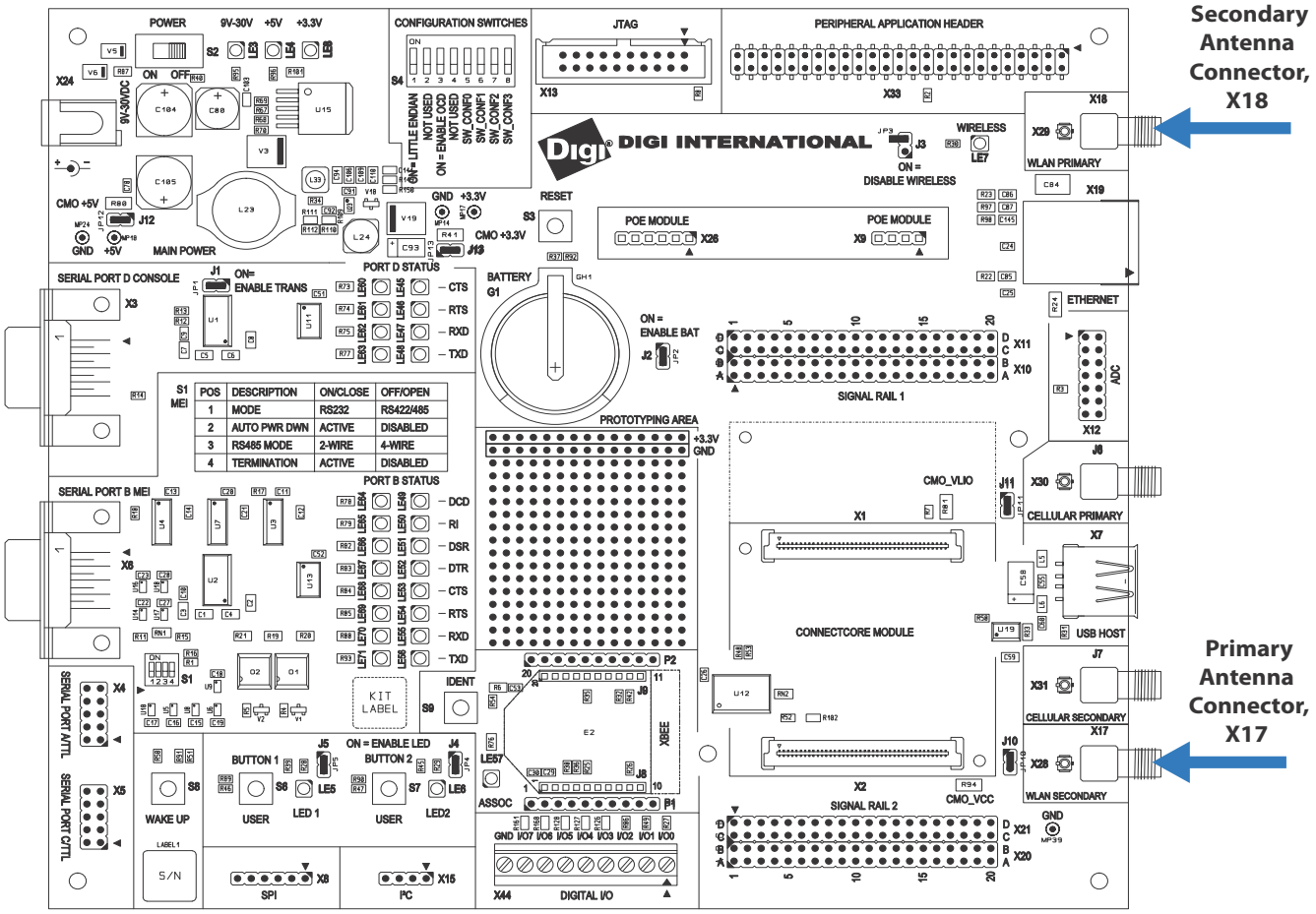
The RJ-45 connector has two LEDs located near the outer lower corners of the connector. These LEDs are not programmable.

LED	Description
Yellow	Network activity (speed): Flashing when network traffic detected; Off when no network traffic detected.
Green	Network link: On indicates an active network link; Off indicates that no network link is present.

WLAN Interface

For the ConnectCore Wi-9P 9215, attach the antenna to the primary connector [X17] and the secondary connector [X18] on the Development Board. See figure below.

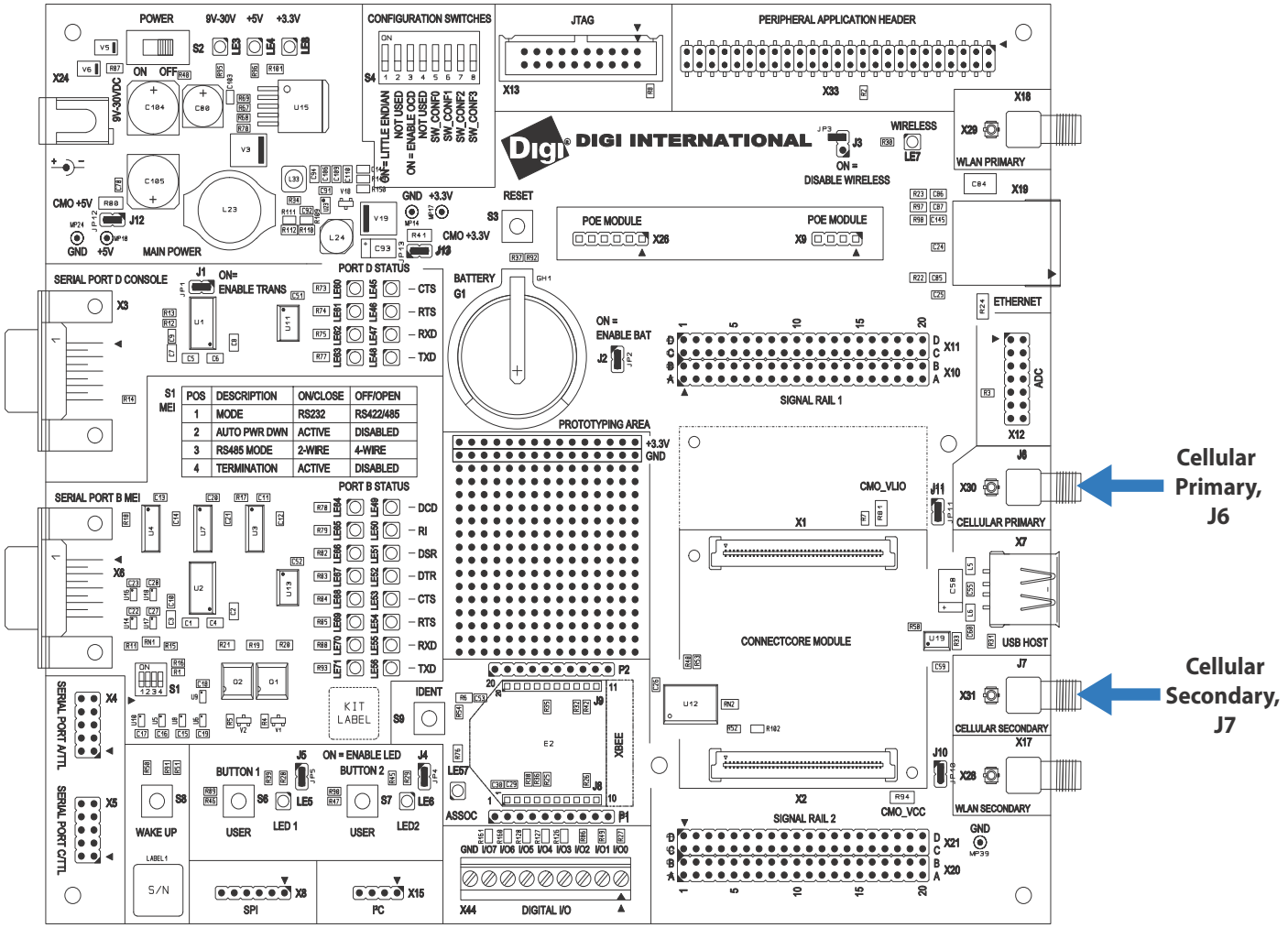
ConnectCore 9P 9215 Development Board

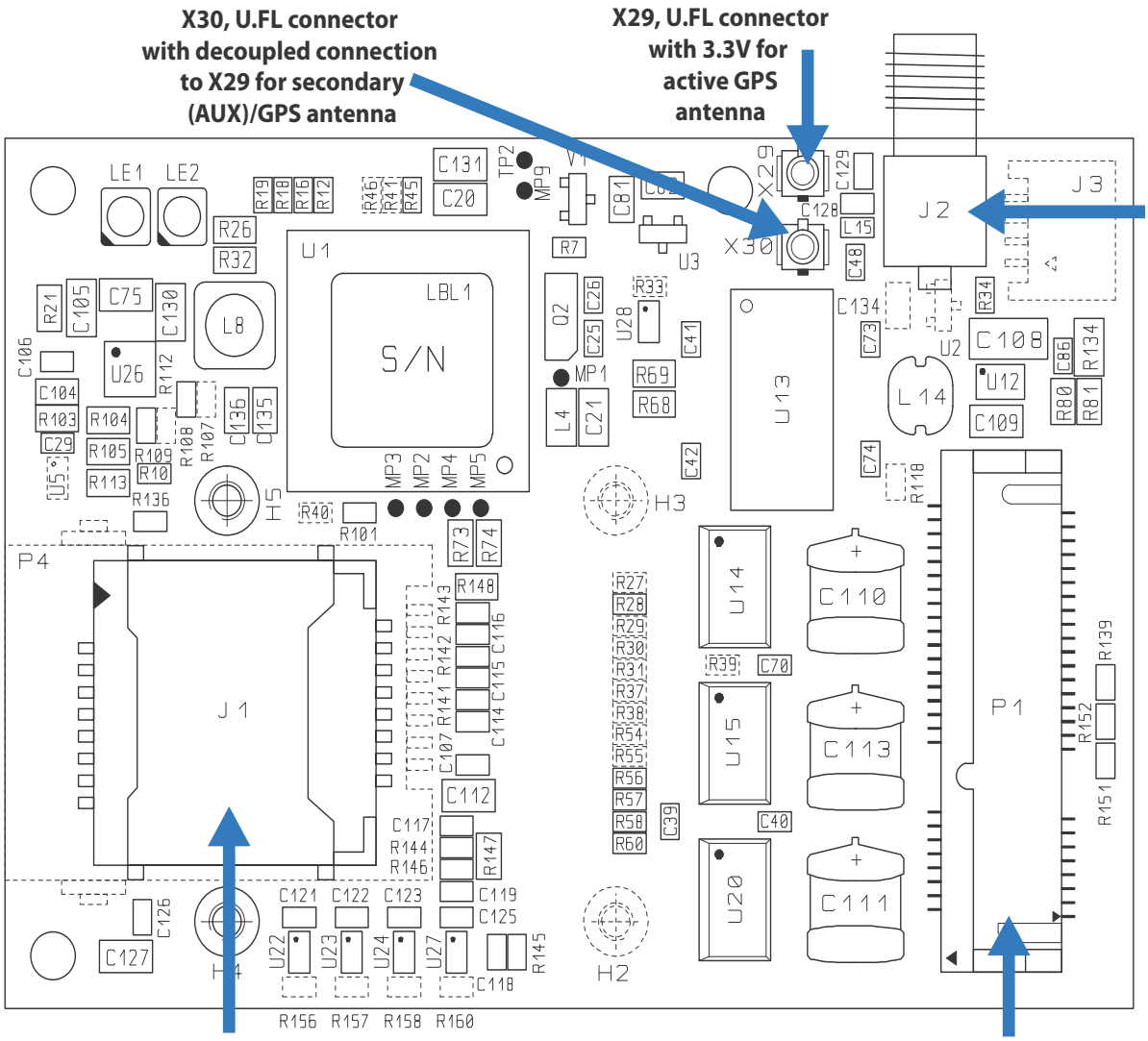


WWAN Interface

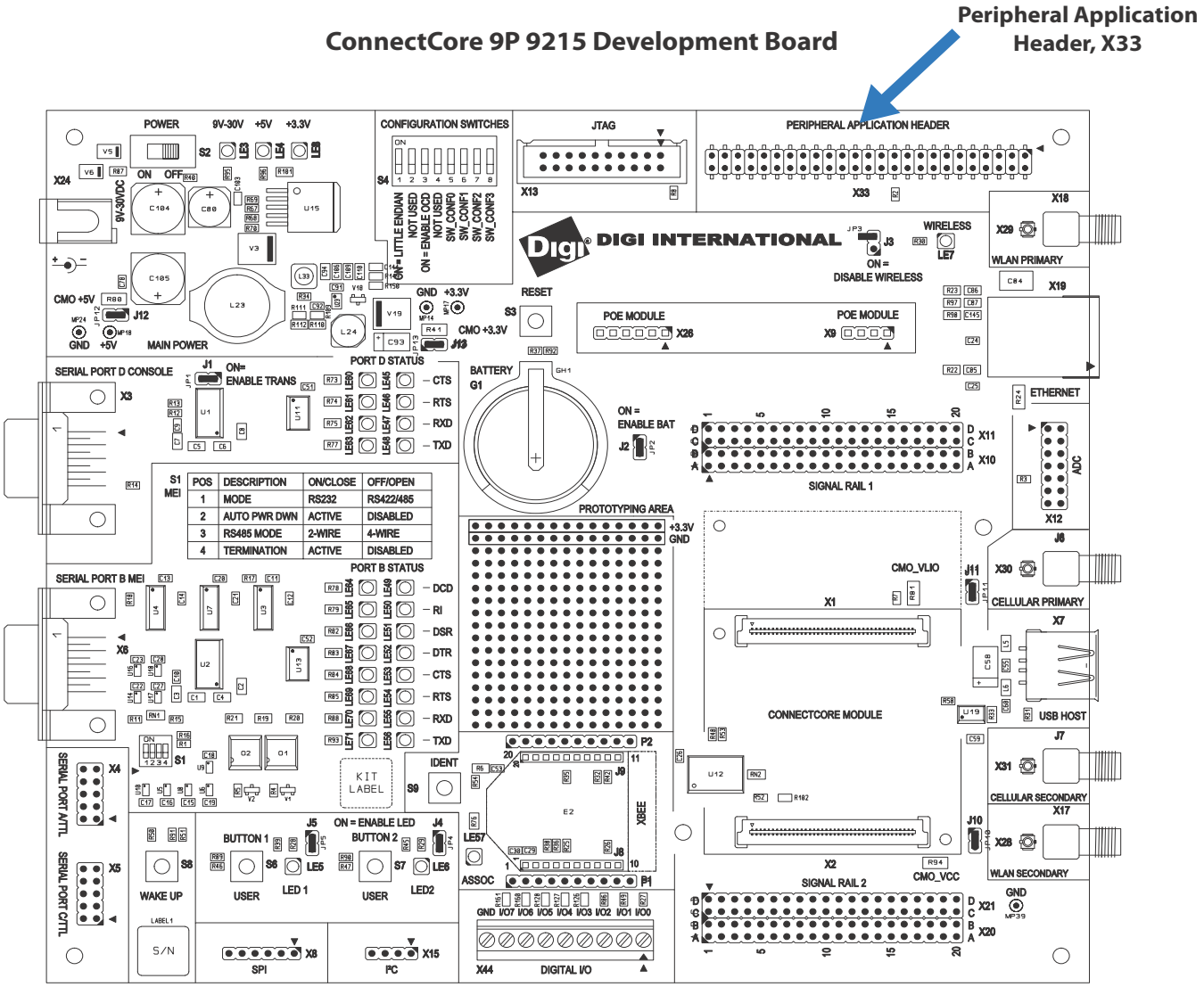
For the ConnectCore 3G 9P 9215, attach the cellular antenna to the primary connector [J6] and the GPS antenna to the secondary connector [J7].

ConnectCore 9P 9215 Development Board




X30, U.FL connector with decoupled connection to X29 for secondary (AUX)/GPS antenna
X29, U.FL connector with 3.3V for active GPS antenna
J2, SMA to U.FL adapter (U.FL connector is on the back side of the SMA connector) for primary antenna connection
Primary antenna connection, Dual SIM socket
P1, PCIe connector for the cellular module
LE1
LE2
U1
LBL1
S/N
L8
U26
J1
P1
P4
J2
J3
X29
X30
U13
U14
U15
U20
L14
C110
C113
C111
C108
U12
C109
U2
H1
H2
H3
H4
H5

Peripheral (Expansion) Headers



The Development Board provides one, 2x25-pin, 0.10" (2.54mm) pitch header for supporting application-specific daughter cards/expansion boards:

- **X33, Peripheral application header.** Provides access to an 16-bit data bus, 10-bit address bus, and control signals (such as CE#, IRQ#, WE#), as well as I^2C and power (+3.3V). Using these signals, you can connect Digi-specific extension modules or your own daughter card to the module's address/data bus.

Peripheral application header, X33

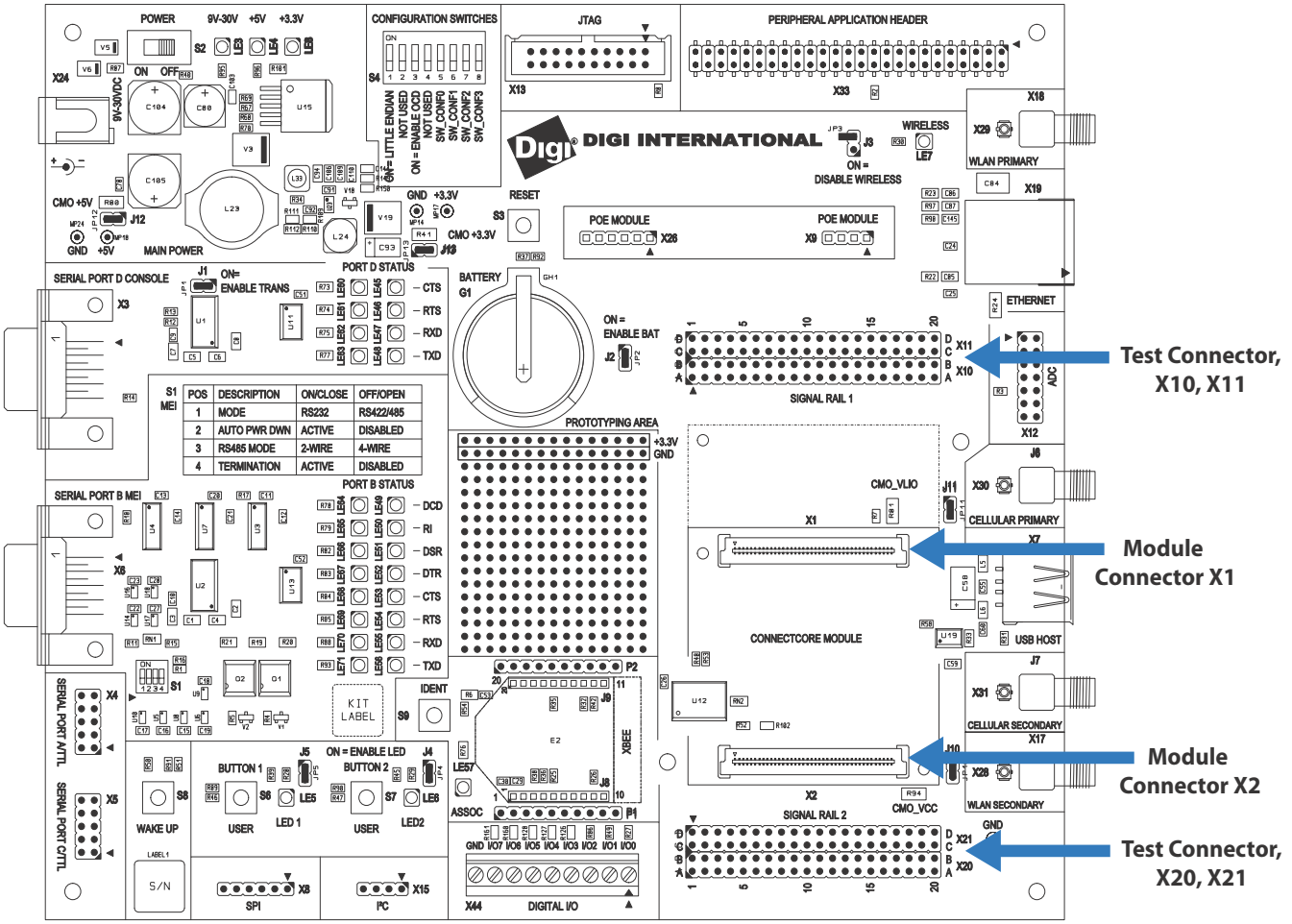
Peripheral application pins are allocated as shown in the table below:

Pin	Signal	Pin	Signal
1	GND	2	BDO
3	BD1	4	BD2
5	BD3	6	GND
7	BD4	8	BD5
9	BD6	10	BD7
11	GND	12	BD8
13	BD9	14	BD10
15	BD11	16	GND
17	BD12	18	BD13
19	BD14	20	BD15
21	GND	22	* 8-bit / 16-bit# GND selects 16-bit data bus
23	GND	24	+3.3V
25	+3.3V	26	BA0
27	BA1	28	BA2
29	BA3	30	GND
31	BA4	32	BA5
33	BA6	34	BA7
35	GND	36	BA8
37	BA9	38	GND
39	EXT_CSO#	40	I2C_SDA/GPIO103
41	EXT_WE#	42	EXT_OE#
43	I2C_SCL/GPIO102	44	EIRQ3/GPIO101
45	+3.3V	46	+3.3V
47	GPIO86	48	GPIO87
49	EXT_CLK	50	GND

Module and Test Connectors

The ConnectCore 9P 9215 family of modules plug into the module connectors X1 and X2 on the Development Board.

ConnectCore 9P 9215 Development Board



Module connectors

See “Module pinout” on page 14 for related information.

Test connectors

The Development Board provides two 4x20 pin test connectors, labeled X10/X11 and X20/X21. These connectors are 1:1 copies of the module pins and are used for measurement or test purposes.

- X10 and X11 correspond to module connector X1.
- X20 and X21 correspond to module connector X2.

X10 pinout

X10 pin	Signal	X10 pin	Signal
A1	GND	B1	GND
A2	RSTOUT#	B2	TCK
A3	TDO	B3	TRST#
A4	LITTLE#/BIG_ENDIAN	B4	WLAN_DISABLE#
A5	SW_CONF2	B5	SW_CONF3
A6	BD0	B6	BD1
A7	BD4	B7	BD5
A8	BD8	B8	BD9
A9	BD12	B9	BD13
A10	GND	B10	BA0
A11	BA3	B11	BA4
A12	BA7	B12	BA8
A13	BA11	B13	BA12
A14	BA15	B14	BA16
A15	EXT_WE#	B15	EXT_CS0#
A16	BE3#	B16	EXT_WAIT#
A17	NC	B17	NC
A18	NC	B18	NC
A19		B19	
A20		B20	VBAT

*USB and Etherent signals are not connected to this connector due to signal quality.

X11 pinout

X11 pin	Signal	X11 pin	Signal
C1	RSTIN#	D1	SRESET#
C2	TMS	D2	TDI
C3	RTCK	D3	OCD_EN#
C4	SW_CONF0	D4	SW_CONF1
C5	WLAN_LED# (CC Wi-9P 9215)	D5	GND
C6	BD2	D6	BD3
C7	BD6	D7	BD7
C8	BD10	D8	BD11
C9	BD14	D9	BD15

X11 pin	Signal	X11 pin	Signal
C10	BA1	D10	BA2
C11	BA5	D11	BA6
C12	BA9	D12	BA10
C13	BA13	D13	BA14
C14	GND	D14	EXT_OE#
C15	EXT_CS2#	D15	BE2#
C16	EXT_CLK	D16	GND
C17	NC	D17	NC
C18	GND	D18	
C19		D19	
C20	3.3V	D20	GND

*USB and Etherent signals are not connected to this connector due to signal quality.

X20 pinout

X20 pin	Signal	X20 pin	Signal
A1	GND	B1	GND
A2	DSRA#/GPIO2	B2	RXDA/SPI_RXD/GPIO3
A3	DTRA#/GPIO6	B3	TXDA/SPI_TXD/GPIO7
A4	DSRC#/GPIO10	B4	RXDC/GPIO11
A5	DTRC#/TXCLKC/GPIO14	B5	TXDC/GPIO15
A6	DSRB#/GPIO53	B6	RXDB/GPIO54
A7	DTRB#/GPIO57	B7	TXDB/GPIO58
A8	DSRD#/GPIO61	B8	RXDD/GPIO62
A9	DTRD#/GPIO65	B9	TXDD/GPIO66
A10	GPIO69	B10	GPIO70
A11	GPIO73	B11	GPIO74
A12	GPIO77	B12	GPIO78
A13	USER_BUTTON1#/GPIO81	B13	USER_LED1#/GPIO82
A14	USER_LED2#/GPIO85	B14	GPIO86
A15	GPIO94	B15	GPIO95
A16	CAN1_RXD/GPIO98	B16	CAN1_TXD/GPIO99
A17	I2C_SCL/GPIO102	B17	12C_SDA/GPIO103
A18	ADC_IN2	B18	ADC_IN3

X20 pin	Signal	X20 pin	Signal
A19	ADC_IN6	B19	ADC_IN7
A20	+3.3V	B20	+3.3V

X21 pinout

X21 pin	Signal	X21 pin	Signal
C1	DCDA#/SPI_EN/GPIO0	D1	CTSA#/GPIO1
C2	RIA#/EIRO2/GPIO4	D2	RTSA#/SPI_CLK/GPIO5
C3	DCDC#/TXCLKC/GPIO8	D3	CTSC#/GPIO9
C4	RIC#/RXCLKC/GPIO12	D4	RTSC#/RCLKC/GPIO13
C5	DCDB#/GPIO51	D5	CTSB#/GPIO52
C6	RIB#/GPIO55	D6	RTSB#/GPIO56
C7	DCDD#/GPIO59	D7	CTSD#/GPIO60
C8	RID#/GPIO63	D8	RTSD#/GPIO64
C9	GPIO67	D9	GPIO68
C10	GPIO71	D10	GPIO72
C11	GPIO75	D11	GPIO76
C12	GPIO79	D12	GPIO80
C13	GPIO83	D13	USER_BUTTON2#/GPIO84
C14	GPIO87	D14	GPIO93
C15	CAN0_RXD/GPIO96	D15	CAN0_TXD/GPIO97
C16	GPIO100	D16	EIR03#/GPIO101
C17	ADC_IN0	D17	ADC_IN1
C18	ADC_IN4	D18	ADC_IN5
C19	AGND_ADC	D19	VREF_ADC
C20	GND	D20	GND

Appendix A:Specifications

This appendix provides environmental, mechanical, safety and power information for the ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 modules.

Mechanical Information

ConnectCore 9P 9215:

The module size is 50 x 50mm.

Two board-to-board connectors are used on the module. The distance between the module and the base board depends on the counterpart on the base board. The minimum distance is 5mm.

The height of the parts mounted on the bottom side of the module does not exceed 2.5mm. The height of the parts mounted on the top side of the module does not exceed 2.5mm if X3 is not populated, or 14 mm if X3 is populated.

ConnectCore Wi-9P 9215:

The module size is 50 x 70mm.

Two board-to-board connectors are used on the module. The distance between the module and the base board depends on the counterpart on the base board. The minimum distance is 5mm.

The height of the parts mounted on the bottom side of the module does not exceed 2.5mm. The height of the parts mounted on the top side of the modules does not exceed 5mm if X3 is not populated, or 14 mm if X3 is populated.

ConnectCore 3G 9P 9215:

The module size is 50 x 70mm.

Two board-to-board connectors are used on the module. The distance between the module and the base board depends on the counterpart on the base board. The minimum distance is 5mm.

The height of the parts mounted on the bottom side of the module does not exceed 2.5mm. The height of the parts mounted on the top side of the modules does not exceed 10mm including the cellular module.

Network Interface

Ethernet

- Standard: IEEE 802.3
- Physical layer: 10/100Base-T
- Data rate: 10/100 Mbps
- Mode: Full or half duplex

WLAN Interface

Note: This WLAN Interface information applies to the ConnectCore Wi-9P 9215 module only.

- Standard: IEEE802.11a/b/g
- Frequency: 2.412GHz - 5.875GHz
- Data Rates Supported
  - 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, 54 Mbps
- Media Access Protocol
  - Carrier-Sense Multiple Access with Collision Avoidance (CSMA/CA)
- Wireless Medium
  - 802.11b/g: Direct Sequence-Spread Spectrum (DSSS) and Orthogonal Frequency Divisional Multiplexing (OFDM)
  - 802.11a: OFDM
- DFS Client
  - This module supports the DFS Client only between the 5.25 and 5.35GHz bands. It does not support being a DFS Master, nor can it be connected to an ad hoc network in these bands.
- Modulation

  DSSS
  - Differential Binary Phase Shift Keying (DBPSK) @ 1 Mbps

- Differential Quadrature Phase Shift Keying (DQPSK) @ 2 Mbps
- Complementary Code Keying (CCK) @ 5.5 and 11 Mbps OFDM
- BPSK @ 6 and 9 Mbps
- QPSK @ 12 and 18 Mbps
- 16-Quadrature Amplitude Modulation (QAM) @ 24 and 36 Mbps
- 64-QAM @ 48 and 54 Mbps

- Frequency Bands
  - 2.412 to 2.472 GHz (ETSI)
  - 2.412 to 2.462 GHz (FCC)
  - 5.150 to 5.250 GHz (ETSI)
  - 5.250 to 5.350 GHz (ETSI) excluding TPC and DFS Client
  - 5.470 to 5.725 GHz (ETSI) excluding TPC and DFS Client
  - 5.725 to 5.875 GHz (ETSI) excluding TPC and DFS Client
  - 5.15 to 5.350 GHz (FCC UNII1 and UNII2)
  - 5.470 to 5.725 GHz
  - 5.725 to 5.850 GHz (FCC)
- Receive Sensitivity 802.11a (typical @ 25°C)

CH	5200	5500	5785
6 Mbps	-85	-85	-85
54 Mbps	-65	-65	-65

- Receive Sensitivity 802.11g (typical 25°C)
  - -84 dBm @ 6 Mbps
  - -81 dBm @ 9 Mbps
  - -80 dBm @ 12 Mbps
  - -80 dBm @ 18 Mbps
  - -78 dBm @ 24 Mbps
  - -76 dBm @ 36 Mbps
  - -70 dBm @ 48 Mbps
  - -68 dBm @ 54 Mbps
- Receive Sensitivity 802.11b (typical 25°C)
  - -86 dBm @ 1 Mbps
  - -86 dBm @ 2 Mbps
  - -84 dBm @ 5.5 Mbps

- -80 dBm @ 11 Mbps

- Available Transmit Power Settings
  (Maximum power setting will vary according to individual country regulations.)
  Typical (± 2 dBm) 25°C

  802.11b/g:

  - 14 dBm (~25 mW) @ 1, 2, 5.5, and 11 Mbps
  - 12 dBm (~16 mW) @ 6,12, 18, 24, 36, 48, and 54 Mbps
  - 6 dBm (~4 mW) @ 6,12, 18, 24, 36, 48, and 54 Mbps

Note: During manufacturing, EVM values are verified up to -23 dBm rms for band A

- Available Transmit Power Settings (Typical (± 2 dBm) @ 25°C)

Note: Maximum power setting will vary according to individual country regulations.

- Connector: 2 x U.FL

Note: Please use HIROSE U.FL-LP-N-2 extraction tool for removing a U.FL cable from the ConnectCore Wi-9P 9215 or ConnectCore 3G 9P 9215modules. .

WWAN Interface

Note: This WWAN Interface information applies to the ConnectCore 3G 9P 9215 module only.

2G/3G celluar connectivity based on Qualcomm Gobi 2000:

Technology	Bands	Receive Diversity Option
1xEV-DO Rev A 1xRTT Rev 0	BC0 - 800 MHz - US cell	D
	BC1 - 1900MHz - US PCS	D
	BC4 - 1800 MHz - KPCS	
	BC6 - 2100 MHz - IMT	
UMTS/HSDPA/HSUPA	B9 - 1700 MHz - Japan 1700 MHz	
	B8 - 900 MHz	
	B6 - 900 MHz - Japan 800 MHz	
	B4 - 1700/2100 - AWS	
	B5 - 850 MHz - US Cell	D
	B3 - 1800 MHz - KPCS	
	B2 - 1900 MHz - US PCS	D

Technology	Bands	Receive Diversity Option
GSM/GPRS/EDGE	850 MHz	X
	900 MHz	X
	1800 MHz	X
	1900 MHz	X
Simultaneous GPS		Standalone on diversity path

Note: D = Rx diversity supported
X = band class supported without Rx diversity
blank = band class not supported

Supported Data Rates:

Gobi Operating Mode	Peak FL Data Rate	Peak RL Data Rate
CDMA 1xRTT	153 kbps	153 kbps
CDMA 1xEV-DO	3.1 Mbps	1.8 Mbps
WCDMA	384 kbps	384 kbps
HSDPA/HSUPA	7.2 Mbps	2.0 Mbps
GSM	14.1 kbps	14.1 kbps
GPRS	115 kbps	115 kbps
EDGE	384 kbps	384 kbps

Environmental Information

The module board assemblies meet all functional requirements when operating in this environments provided below.

Note: Please refer to the thermal specifications in this manual for additional information about operating temperature conditions

ConnectCore 9P 9215

- Operating temperature: -40°C to +85°C max
- Storage temperature: -40°C to +125°C
- Relative humidity: 5% to 95%, non-condensing
- Altitude: 0 to 12,000 feet

ConnectCore Wi-9P 9215 & ConnectCore 3G 9P 9215 (digital part)

- Operating temperature: -40°C to +85°C max
- Storage temperature: -40°C to +125°C
- Relative humidity: 5% to 95%, non-condensing
- Altitude: 0 to 12,000 feet
- Qualcom Gobi2000 operating temperature: -30°C to +70°C
- Qualcom Gobi2000 storage temperature: -55°C to +100°C
- Qualcom Gobi2000 relative humidity: 10% to 90%, non-condensing

Thermal Specifications

The table below shows the specific standard operating temperature ranges for the entire ConnectCore 9P 9215 embedded core module family.

Standard Operating Temperature Ranges

Product	Operating Temperature Range
ConnectCore 9P 9215	-40 to +85°C
ConnectCore Wi-9P 9215	-40 to +65°C @ 100% Duty Cycle (WLAN) -40 to +85°C @ 33% Duty Cycle (WLAN)
ConnectCore 3G 9P 9215	-30 to +70°C

The lower standard operating temperature range is specified without restrictions, except condensation must not occur.

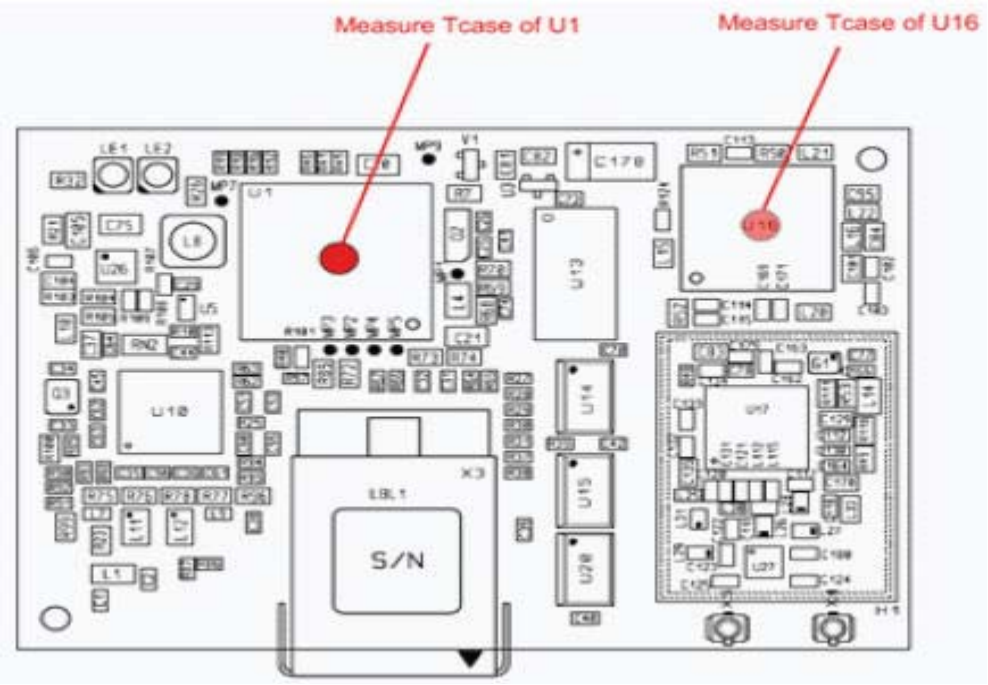
The upper operating temperature limit depends on the host PCB layout and surrounding environmental conditions. To simplify the customer's design process, a maximum component case temperature has been specified.

Maximum Component Case Temperature

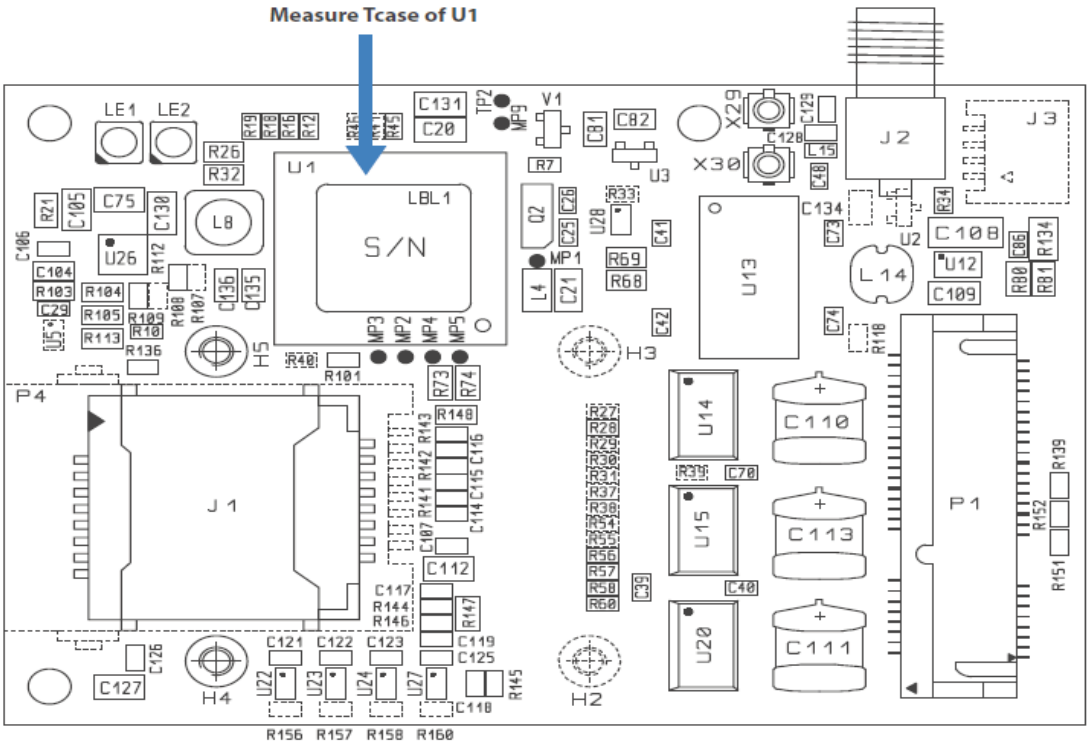
Product	Component	Maximum Case Temperature
ConnectCore 9P 9215	U1	120°C
ConnectCore W-9P 9215	U16	95°C
ConnectCore 3G 9P 9215	U1	120°C

The maximum component case temperature must remain below the maximum, measured at the locations shown in the figure below.

ConnectCore Wi-9P 9215 Module



ConnectCore 3G 9P 9215 Module



When attaching thermocouples, please the follow the guidelines below:

- Carefully remove any labels or other foreign material from the component.
- Ensure an adhesive with high thermal conductivity is used. Use as little adhesive as possible.
- Make sure the thermocouple is touching the case of the component and not "floating" in the adhesive.
- The use of precision, fine-wire K-type thermocouples is strongly recommended
  - Omega Engineering P/N 5TC-TT-K-36-72, or similar

Additional design recommendations

The following list provides additional design guidance with respect to thermal management in applications with operating temperatures at the high end or beyond the specified standard ambient temperature range.

- Providing air movement will improve heat dissipation.
- The host PCB plays a large part in dissipating the heat generated by the module. A large copper plane located will improve the heat dissipation capabilities of the PCB.
- If the design allows, added buried PCB planes will also improve heat dissipation. The copper planes create a larger surface to spread the heat into the surrounding environment.

Safety Statements

To avoid contact with electrical current:

- Never install electrical wiring during an electrical storm.
- Use a screwdriver and other tools with insulated handles.
- Wear safety glasses or goggles.
- Installation of inside wiring may bring you close to electrical wire, conduit, terminals and other electrical facilities. Extreme caution must be used to avoid electrical shock from such facilities. Avoid contact with all such facilities.
- Protectors and grounding wire placed by the service provider must not be connected to, removed, or modified by the customer.
- Do not touch or move the antenna(s) while the unit is transmitting or receiving.
- Do not hold any component containing a radio such that the antenna is very close to or touching any exposed parts of the body, especially the face or eyes, while transmitting.
- Do not operate a portable transmitter near unshielded blasting caps or in an explosive environment unless it is a type especially qualified for such use.
- Any *external* communications wiring you may install needs to be constructed to all relevant electrical codes. In the United States, this is the National Electrical Code Article 800. Contact a licensed electrician for details.

Power Requirements

ConnectCore 9P 9215

Parameter	Limits		
Input voltage (Vcc)	3.3V±10% (3.00V to 3.60V)		
Input current	660mA max		
Input low voltage	0.0V	<V_{IL}	<0.3*Vcc
Input high voltage	0.7*Vcc	<V_{IH}	<Vcc
Output low voltag (@lol=100uA)	0.0V	<V_{OL}	<0.2V
Output high voltage (@loh=100uA)	Vcc-0.2V	<V_{OH}	<Vcc

ConnectCore Wi-9P 9215

Parameter	Limits		
Input voltage (Vcc)	3.3V±10% (3.00V to 3.60V)		
Input current	1A max		
Input low voltage	0.0V	<V_{IL}	<0.3*Vcc
Input high voltage	0.7*Vcc	<V_{IH}	<Vcc
Output low voltage	0.0V	<V_{OL}	<0.4V
Output high voltage	Vcc-0.4V	<V_{OH}	<Vcc

ConnectCore 3G 9P 9215

Parameter	Limits		
Input voltage (Vcc)	3.3V±10% (3.00V to 3.60V)		
Input current	1.9A max		
Input low voltage	0.0V	<V_{IL}	<0.3*Vcc
Input high voltage	0.7*Vcc	<V_{IH}	<Vcc
Output low voltage	0.0V	<V_{OL}	<0.4V
Output high voltage	Vcc-0.4V	<V_{OH}	<Vcc

IEEE802.11 a/b/g WLAN

The ConnectCore Wi-9P 9215 provides access to an IEEE802.11a/b/g WLAN interface. The whole circuitry is located on the module. The user can track WLAN activity through the WLAN-LED# signal. The user can also disable the RF power amplifier by activating the WLAN-DISABLE# signal.

Two U.FL connectors are available for dual-diversity.

The WLAN baseband controller can be reset through GPIO92. When this signal is low, the baseband controller is in reset mode. When high, the controller is active.

The interrupt signal connected to the baseband controller is GPIO_AO.

WWAN Activity

The ConnectCore3G 9P 9215 provides access to a PCIe 3G module. The whole circuitry is located on the module. The user can track WWAN activity through the WLAN-LED# signal. The user can also disable the PCIe module by activating the WLAN-DISABLE# signal.

Not including the Gobi modem there are three U.FL connectors for a WWAN antenna and a GPS antenn available on the ConnectCore 3G 9P 9215 module. Including the Gobi modem there are five U.FL connectors available.

The PCIe power supply can be controlled through GPIO0 of the onboard OXU210 USB controller. When this signal is low, the PCIe power is off.

The PCIe reset signal PCIE_RESET# is connected to GPIO_AO.

ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 Typical Power Save Current /Power Measurements

The following illustrates typical power consumption for the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules. These measurements were made using the NET+OS napsave sample application in function applicationStart( ), with module's Ethernet connected to a 100Mb network. For the ConnectCore Wi-9P 9215 module, WiFi is enabled and associated.

ConnectCore 9P 9215

	Module and Dev Board[1]	Module only[2]
Normal operational mode[3]	1.63W (496mA)	1.45W (443mA)
Full clock scaling mode[4]	.879W (267mA)	.683W (208mA)
Sleep mode[5]	.346W (105mA)	.151W (46mA)

ConnectCore Wi-9P 9215

	Module and Dev Board[1]	Module only[2]
Normal operational mode[3]	2.69W (816mA)	2.36W (716mA)
Full clock scaling mode[4]	2.01W (610mA)	1.76W (533mA)
Sleep mode[5]	0.73W (220mA)	0.46W (138mA)

[1] This measurement was taken from the R80 current sense resistor (0.025 ohm) on the JumpStart Kit development board.

[2] This measurement represents only the current of the VLIO and +3.3V inputs to the module, measured from the two current sense resistors R81 and R94 (0.025 ohm) located on the JumpStart Kit development board.

[3] This is the default power consumption mode when entering application Start(), as measured with the napsave sample application. The value of the NS9215 Clock Configuration register (A090017C) is 02012015 hexadecimal. (Note 02012015 enables USART B, UART D, the Ethernet MAC, the I/O Hub, and Memory Clock 0).

[4] This measurement was produced by selecting the “Clock Scale” menu option in the napsave sample application. For the ConnectCore Wi-9P 9215, the clock scaling is divided by 4, for the ConnectCore 9P 9215, the clock scaling is divided by 16.

[5] This measurement was produced by selecting the “Deep Sleep/Wakeup with an External IRQ” menu option in the napsave sample application.

ConnectCore 3G 9P 9215 Typical Power Save Current /Power Measurements

The following illustrates typical power consumption for the ConnectCore 3G 9P 9215 module. These measurements were made using a Python application, which made a call into digipowercontrol.system_power_set(0), which placed the module into a deep sleep mode.

ConnectCore 3G 9P 9215

	Module and Dev Board[1]	Module only[2]
Normal operational mode[4]	2.60W (800mA)	2.30W (708mA)
Sleep mode[3, 4]	0.61W (184mA)	0.463W (140mA)

[1] This measurement was taken from the R80 current sense resistor (0.025 ohm) on the JumpStart Kit development board.

[2] This measurement represents only the current of the VLIO and +3.3V inputs to the module, measured from the two current sense resistors R81 and R94 (0.025 ohm) located on the JumpStart Kit development board.

[3] This measurement was made using the Python digipowercontrol.system_power_set(0) API, which places the module into a deep sleep mode.

[4] These measurements were made with an ethernet cable plugged in and no external USB devices connected.

Typical Module Current / Power Measurements

The following illustrates typical power consumption using various NS9215 power management mechanisms. These measurements were taken with all NS9215 I/O clocks disabled except UART B, UART D, Ethernet MAC, I/O Hub, and the Memory Clock; the Ethernet connected to a 100Mb network and the WLAN interface associated with an access point, using a standard module plugged into a JumpStart Kit board, with nominal voltage applied.

ConnectCore 9P 9215

	VLIO[1]	+3.3V[1]	Total Power
With FIMs (DRPIC) enabled [4]	1.27W (384mA @ 3.3V)	.561W (170mA @ 3.3V)	1.83W
Full clock scaling mode[4]	.904W (274mA @ 3.3V)	.561W (170mA @ 3.3V)	1.47W

ConnectCore Wi-9P 9215

	VLIO[1]	+3.3V[1]	Total Power
With all clocks enabled [2, 4]	1.43W (432mA @ 3.3V)	1.17W (354mA @ 3.3V)	2.6W
Default configuration [3, 4]	1.13W (343mA @ 3.3V)	1.17W (354mA @ 3.3V)	2.30W

[1] VLIO is supplying the core voltage regulator. This typical measurement was made with VLIO and +3.3V set to 3.3V. VLIO can vary between 2.5V to 5.0V. +3.3V can vary between 3.1V to 3.6V.

[2] This is power consumption with all clocks on, NS9215 Clock Configuration register (A090017C) set to 02013BFF hexadecimal.

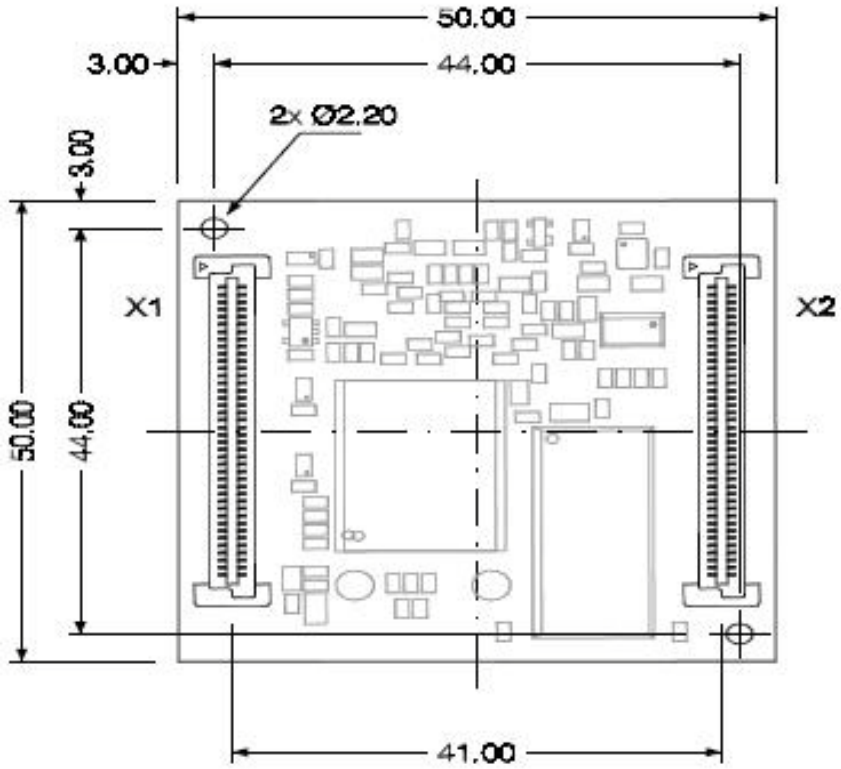
[3] This is the default power consumption. Note the default value of the NS9215 Clock Configuration register (A090017C) is 02012015 hexadecimal.

[4] FIM is the Flexible Interface Module. DRPIC is a high performance 8-bit RISC Microcontroller.

ConnectCore 9P 9215 Module Mechanical Details

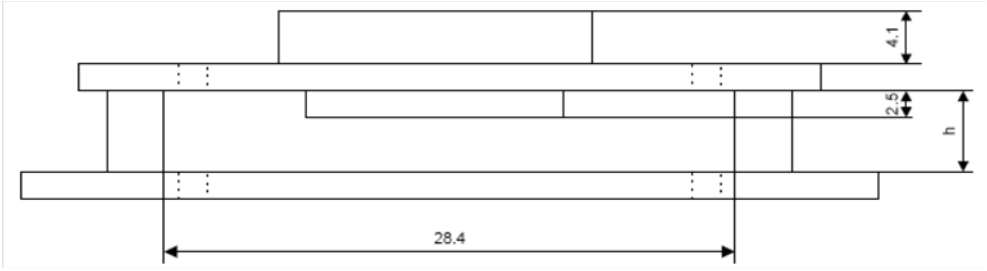
Top view

Note: Measurements are in millimeters.

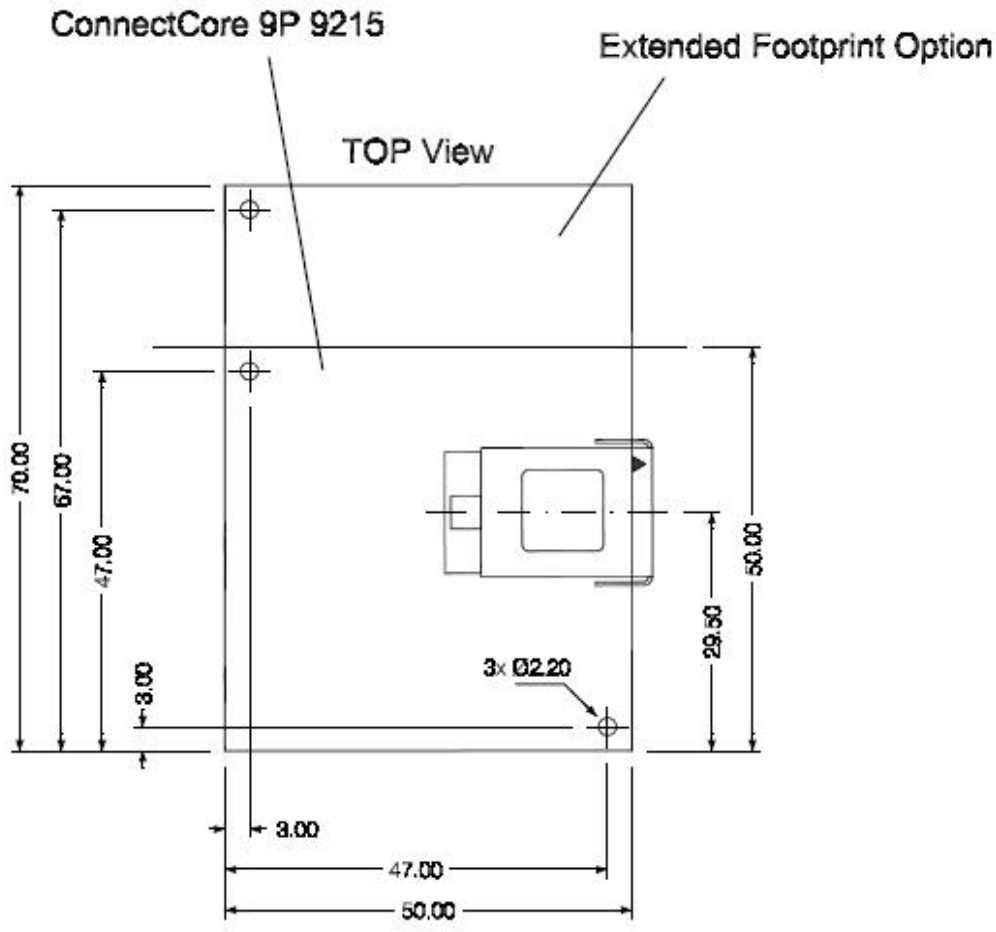


Side view

Note: Measurements are in millimeters.



Extended Footprint Option

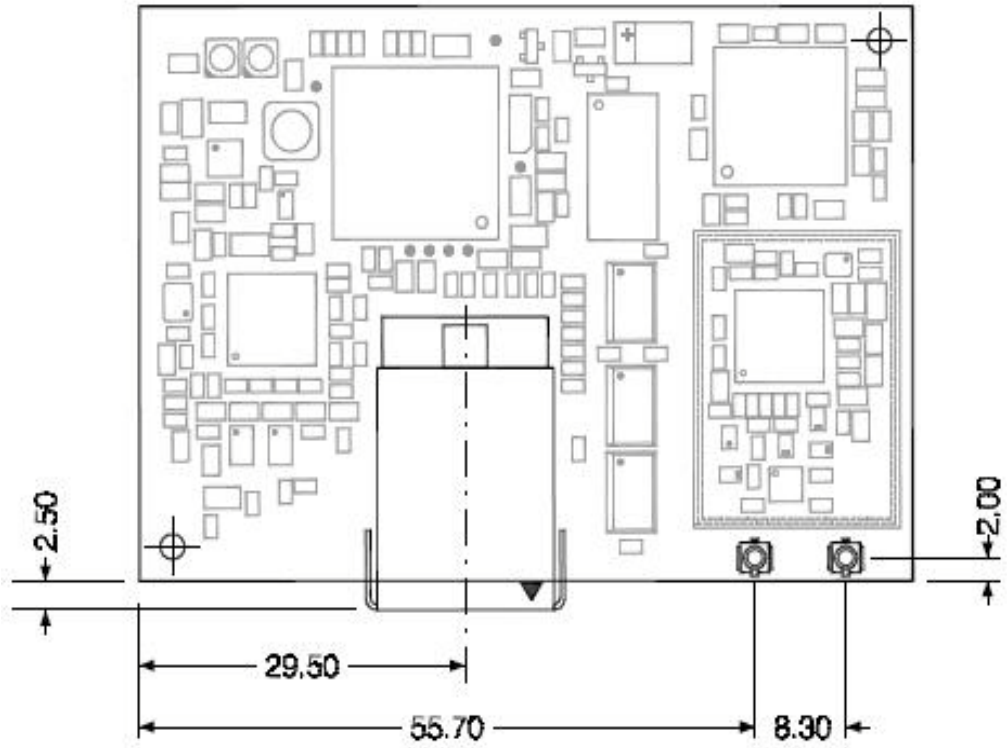


Device	Berg/FCI connector
ConnectCore 9P 9215 module	61082-081409LF
ConnectCore 9P 9215 JumpStart board (mating connector on the base board)	61083-084409LF

ConnectCore Wi-9P 9215 Module Mechanical Details

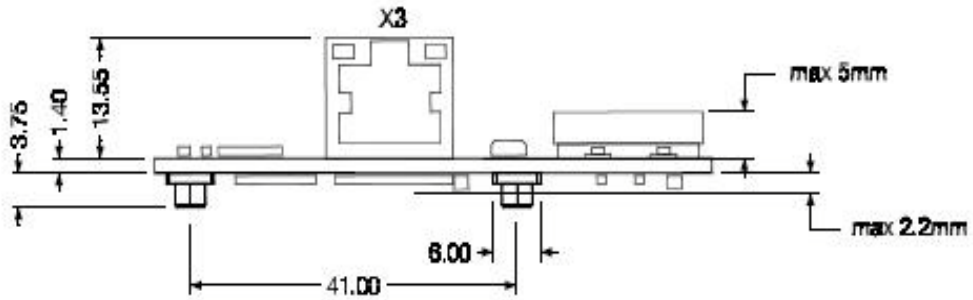
Top view

Note: Measurements are in millimeters.



Side view

Note: Measurements are in millimeters.

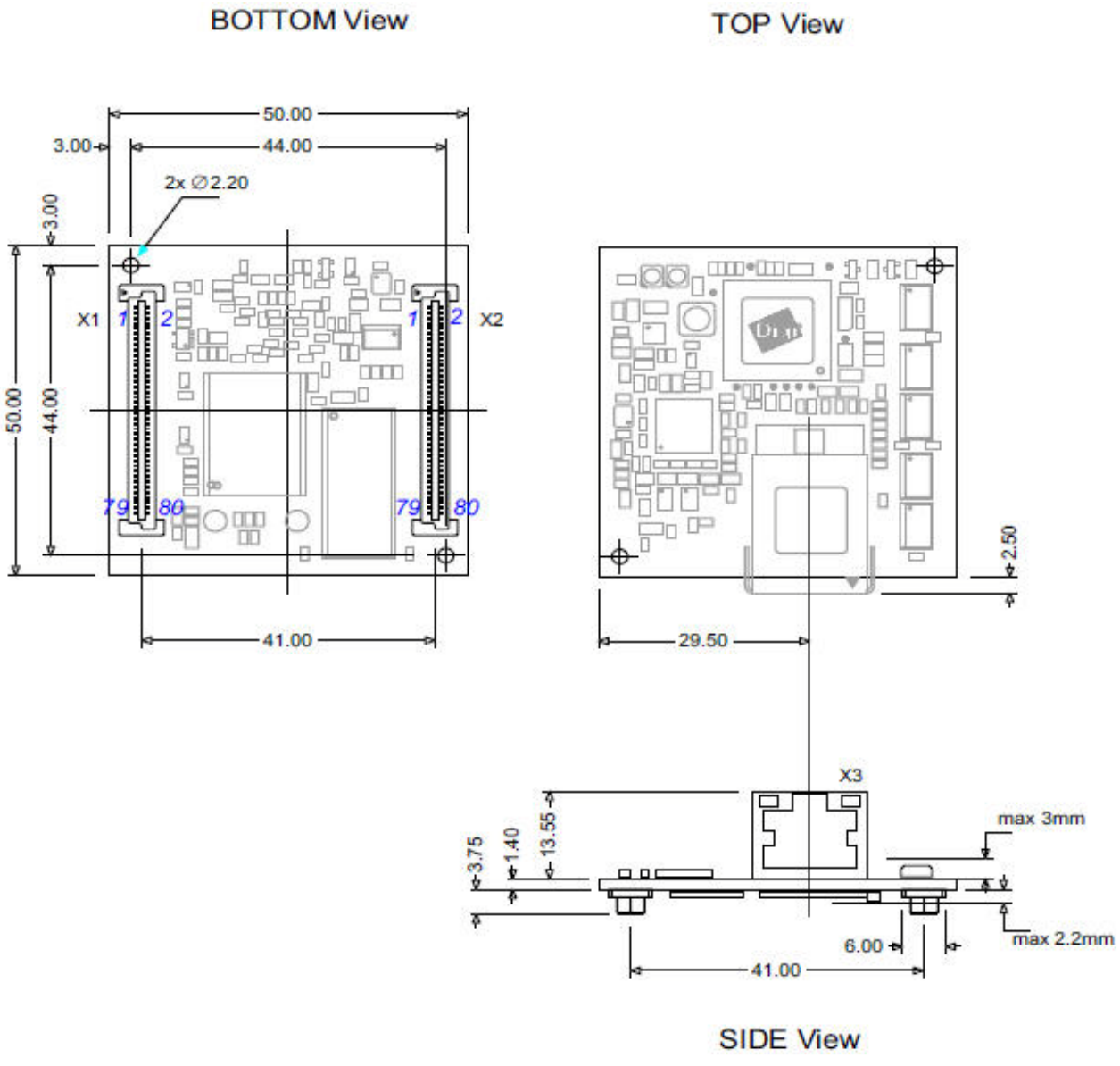


Layout Recommendation

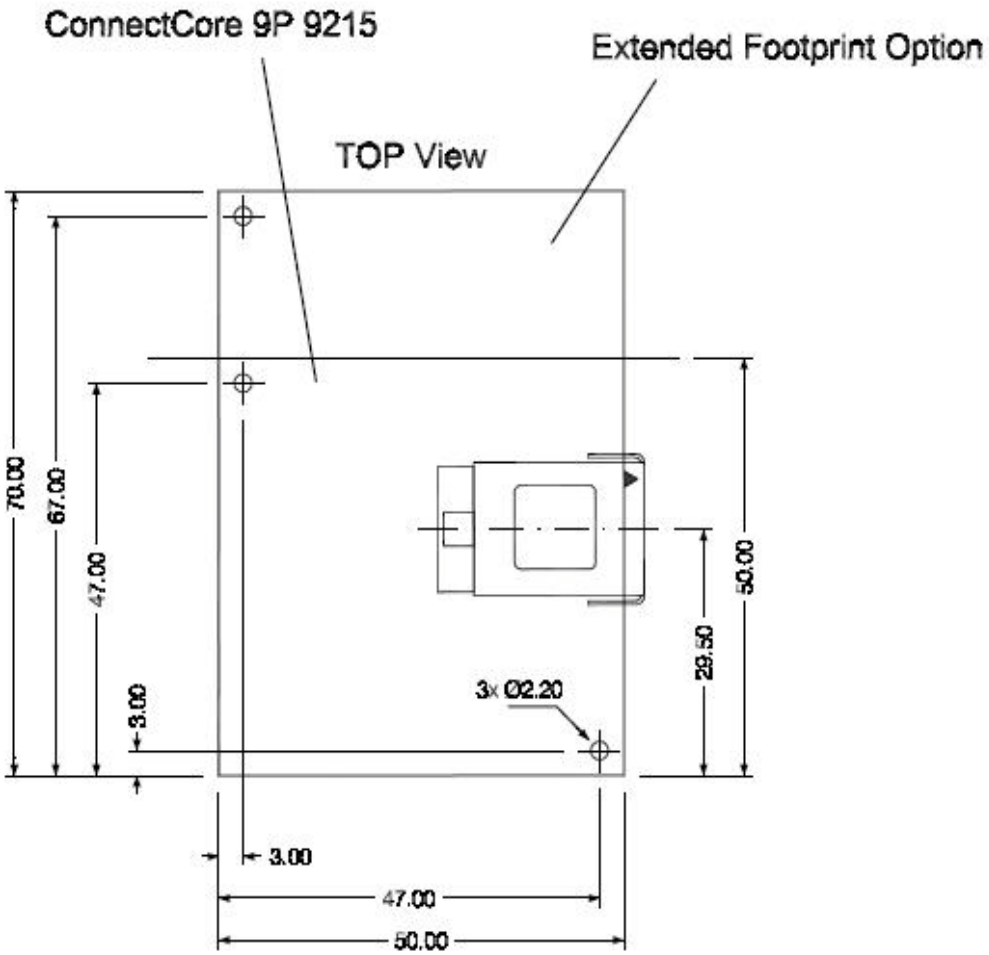
Below are the mechanical dimensions of the ConnectCore 9P 9215 module.

The layout of the JumpStart board is consistent with the recommendations from Berg/FCI for the mating connector (Berg/FCI 61083-084409LF). There is a 41mm separation between the two module connectors. Drawing number 61083 on the FCI web page: www.fciconnect.com shows the manufacturer recommended layout.

ConnectCore 9P 9215



Extended Footprint Option



Device	Berg/FCI connector
ConnectCore 9P 9215 module	61082-081409LF
ConnectCore 9P 9215 JumpStart board (mating connector on the base board)	61083-084409LF

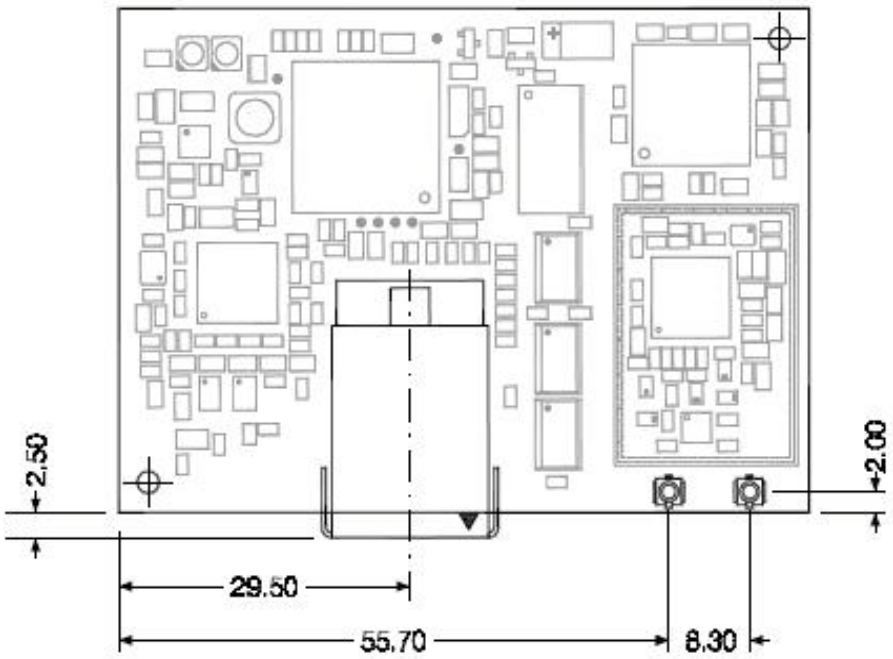
Device	Berg/FCI connector
ConnectCore 9P 9215 - Wi-9P 9215 module	61082-081409LF
ConnectCore Wi-9P 9215 JumpStart board (mating ConnectCore 9P 9215 - Wi-9P 9215 JumpStart board)	61083-084409LF

ConnectCore Wi-9P 9215

Below are the mechanical dimensions of the ConnectCore Wi- 9P 9215 module.

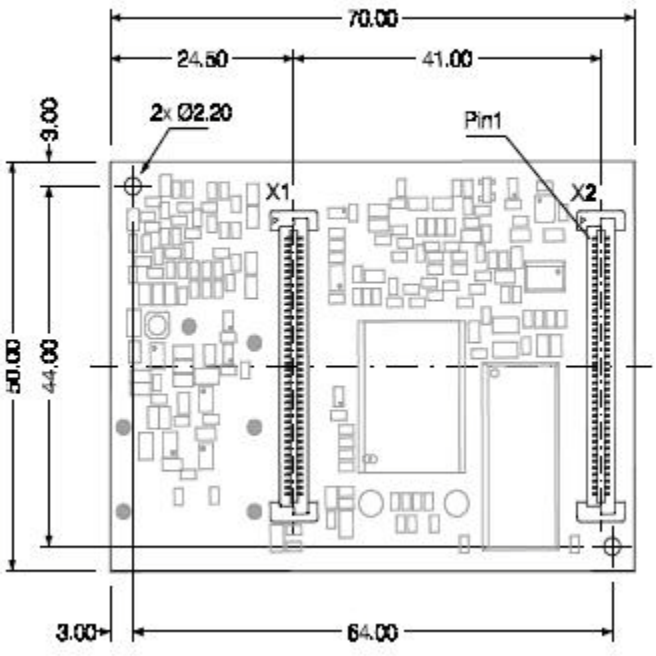
TOP View.

TOP View

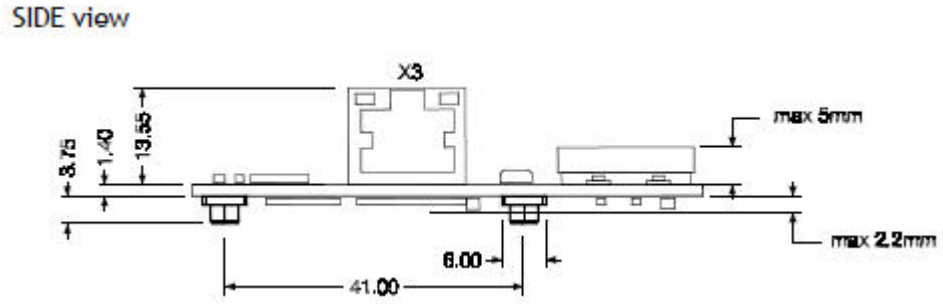


BOTTOM View

BOTTOM View



SIDE view

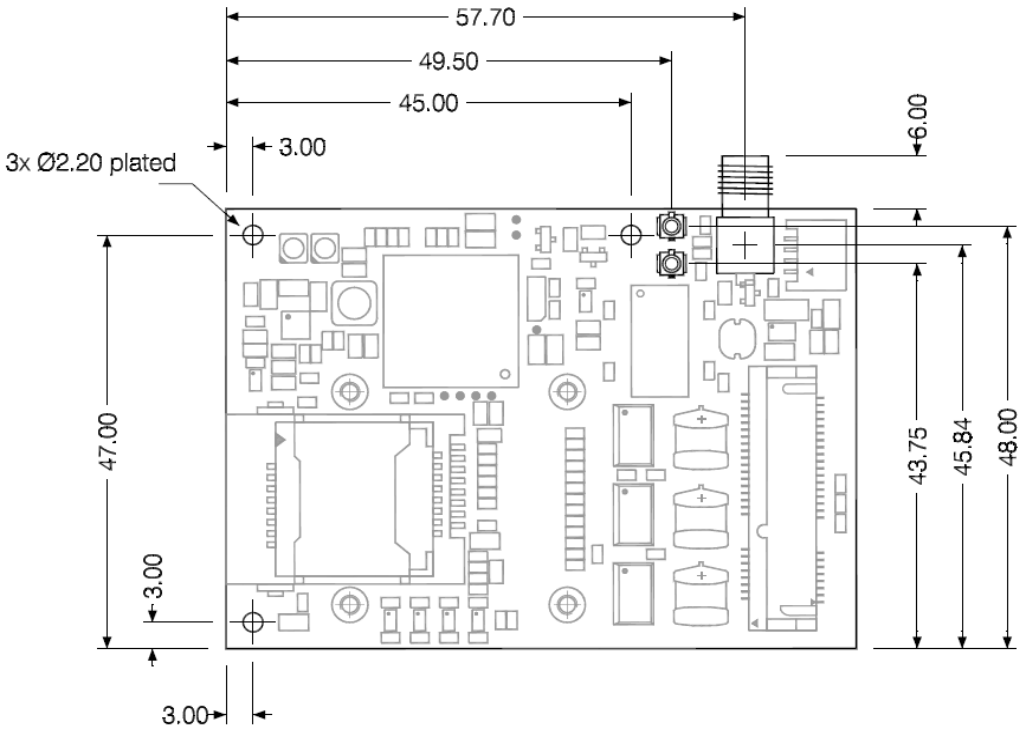


Device	Berg/FCI connector
ConnectCore Wi-9P 9215	61082-081409LF
ConnectCore Wi-9P 9215 Development board (mating ConnectCore 9P 9215 - Wi-9P 9215 JumpStart board)	61083-084409LF

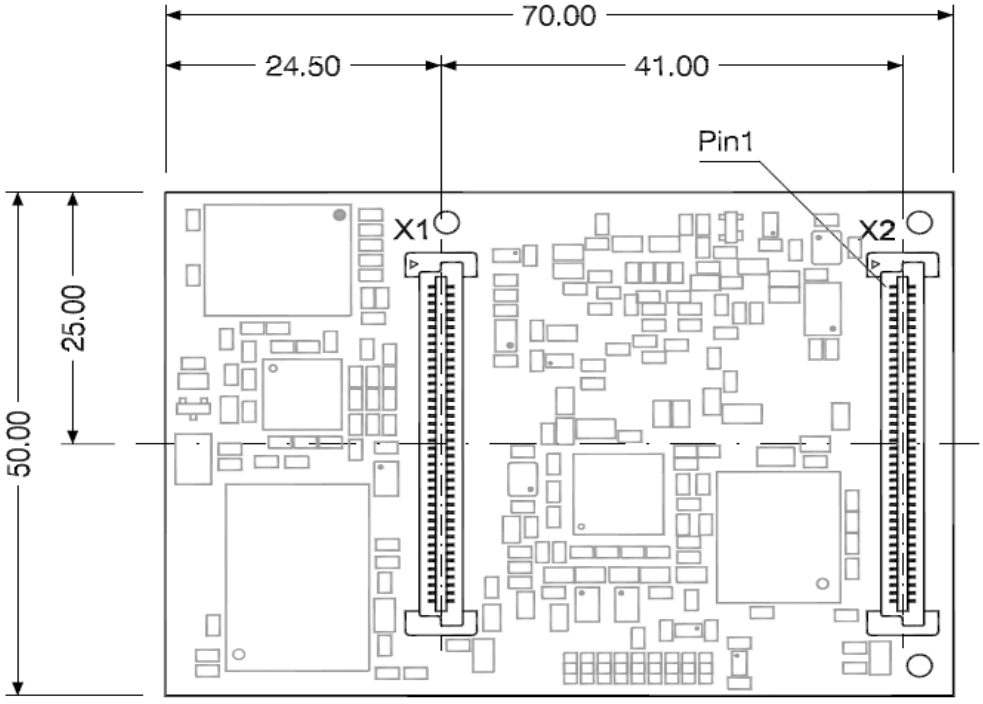
ConnectCore 3G 9P 9215

Below are the mechanical dimensions of the ConnectCore 3G 9P 9215 module.

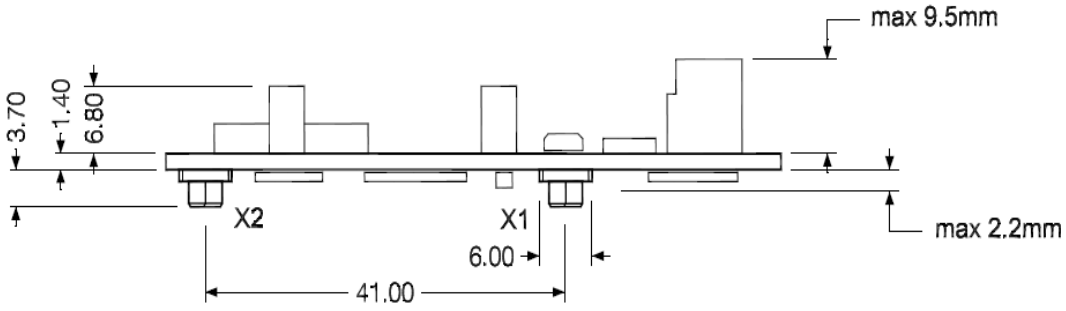
TOP View



BOTTOM View



SIDE view

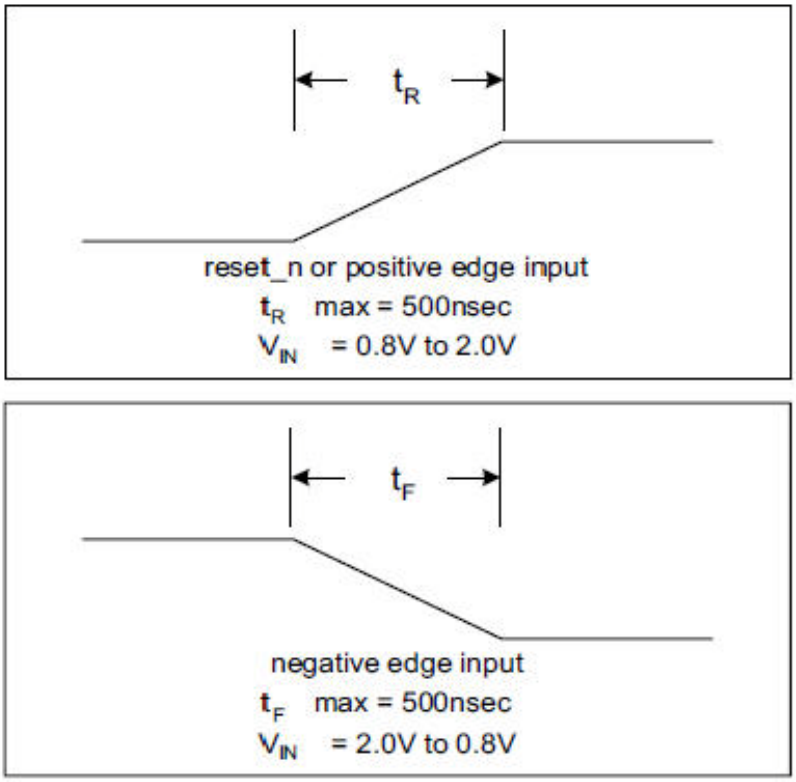


Device	Berg/FCI connector
ConnectCore 3G 9P 9215	61082-081409LF
ConnectCore 3G 9P 9215 Development board (mating ConnectCore 9P 9215 - Wi-9P 9215 JumpStart board)	61083-084409LF

Reset and Edge Sensitive Input Timing Requirements

The ConnectCore 9P family of modules critical timing requirement is the rise and fall time of the input. If the rise time is too slow for the reset input, the hardware strapping options may be registered incorrectly. If the rise time of a positive-edge-triggered external interrupt is too slow, then an interrupt may be detected on both the rising and falling edge of the input signal.

A maximum rise and fall time must be met to ensure that reset and edge sensitive inputs are handled correctly. With Digi processors, the maximum is 500 nanoseconds as shown:



On the ConnectCore 9P 9215 Development Board there was a measurement of 220ns rise time and 10ns fall time.

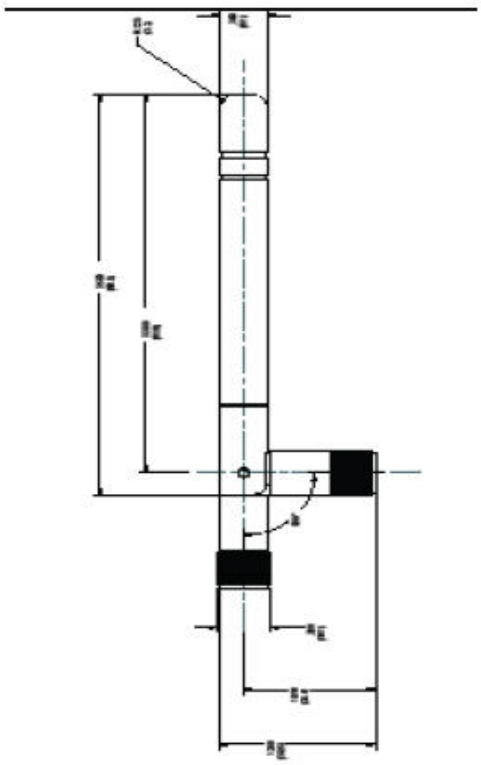
ConnectCore Wi-9P 9215 Antenna Specifications: 2 dBi Dipole

Attributes

Attribute	Property
Frequency	2.4~2.5 GHz
Power output	2W
DB gain	2 dBi
VSWR	< or = 2.0
Dimension	108.5 mm x 10.0 mm
Weight	10.5g
Temperature rating	-40°–+80° C
Part number	DG-ANT-20DP-BG

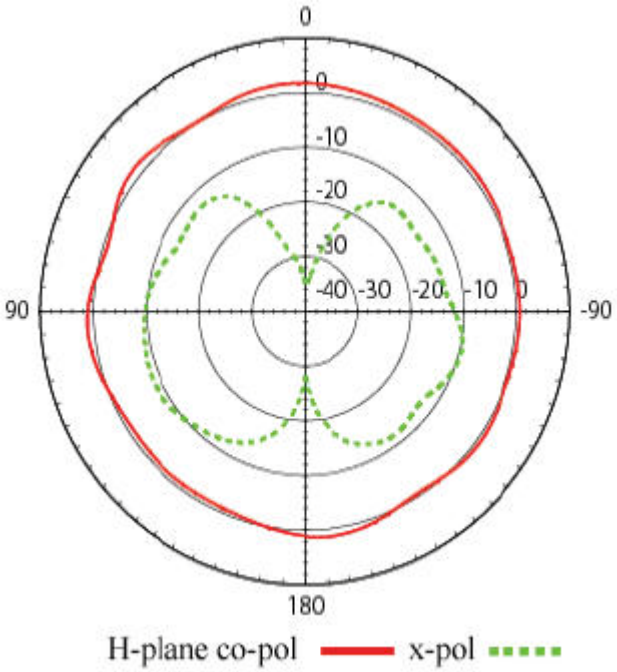
Dimensions

Note: Dimensions are provided for reference purposes only. The actual antenna might vary.



Antenna strength (radiation pattern) diagram

This diagram shows the strength of the signal received by the whip antenna on both a horizontal and vertical plane. The diagram shows the magnetic field when the antenna is in a vertical position. The red solid line represents the horizontal plane and the green dotted line represents the vertical plane. You can see in the illustration that at 90 degrees, the signal strength is 0 (as expected).



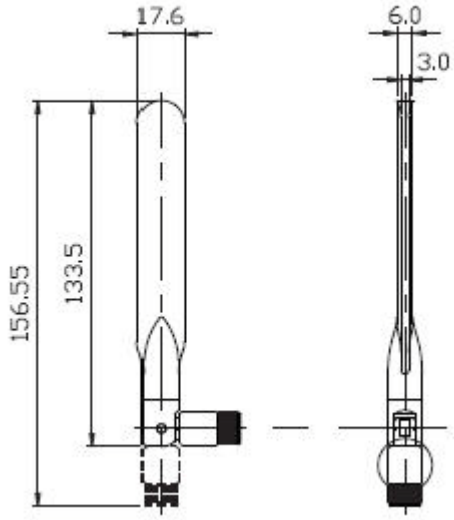
ConnectCore Wi-9P 9215 Antenna Specifications: 5.5 dBi Dipoles

Attributes

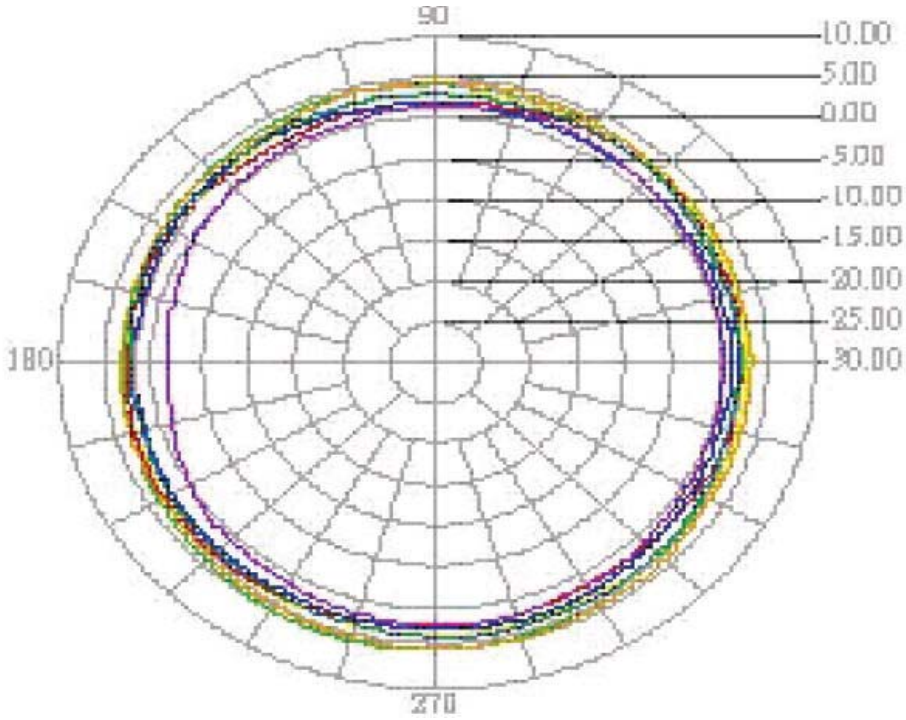
Attributes	Band 1	Band 2
Frequency	2.4~2.5 GHz	5.15~5.35 GHz 5.725~5.85 GHz
VSWR	2.0 max	
Return loss	-10 dB max	
DB gain	5 dBi (Typ)	
Polarization	Linear	
Power output	1W	
Dimension	See measurements in the drawing after the table	
Operating temperature	-20°–+65°C	
Storage temperature	-20°–+65°C	
Part number	DG-ANT-50DP-AG	

Dimensions

Note: Dimensions are provided for reference purposes only. The actual antenna might vary.

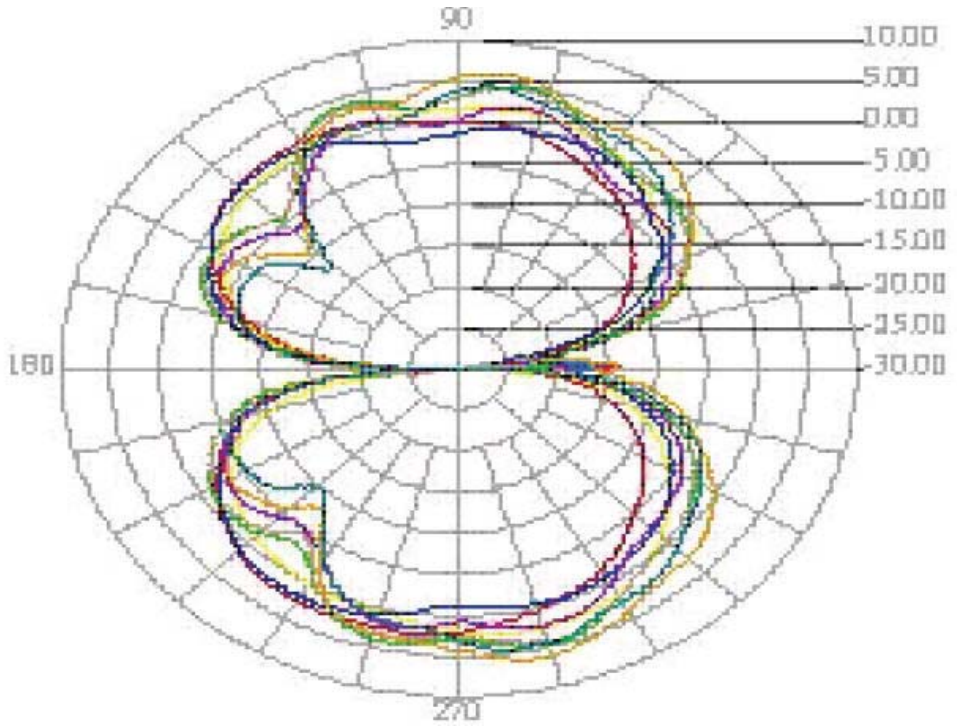


Radiation pattern: H-Plane (2.0 and 5.0 GHz)



Color	Freq (MHz)	Peak (dBi)	Angle (o)	Avg (dBi)
Yellow	2400.0	3.39	257.68	2.98
Red	2450.00	3.17	214.74	2.37
Blue	2500.00	2.79	288.0	1.96
Purple	5150.00	2.25	280.42	0.82
Green	5200.00	5.23	252.63	2.71
Light brown	5250.00	4.51	272.84	3.16
Orange	5750.00	5.03	267.79	3.88
Aqua	5850.00	3.83	276.63	2.74

Radiation pattern: E-plane (2.0 and 5.0 GHz)



Color	Freq (MHz)	Peak (dBi)	Angle (o)	Avg (dBi)
Yellow	2400.0	2.60	283.22	-1.10
Red	2450.00	2.57	240.42	-1.36
Blue	2500.00	1.92	237.27	-1.78
Purple	5150.00	2.37	78.67	-1.91
Green	5200.00	4.80	79.30	0.32
Light brown	5250.00	4.49	79.93	-0.01
Orange	5750.00	6.34	283.85	1.08
Aqua	5850.00	4.67	283.22	-0.46

ConnectCore 3G 9P 9215 TG-09 Penta-band GSM Hinged R/A SMA antenna

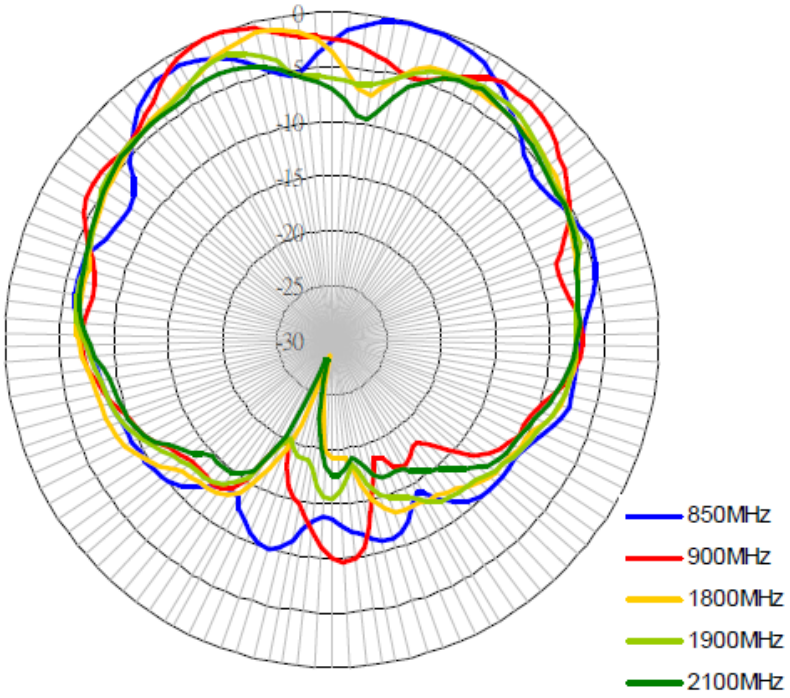
The TG-09 Penta-band GSM Hinged R/A SMA antenna is a quality antenna with high level electrical performance. The unique hinge design let the user able to rotate the antenna 180° for an optimal GSM signal reception. With the environmental harden casing, this antenna is the ideal GSM antenna for vehicle tracking device.

Attributes

- Part number - TG.09.0113
- Product name - Penta-band GSM Hinged R/A SMA Male Dipole
- Features:
  - 180° rotatable hinged design for optimal reception
  - Top quality housing with brass hinge and connector
  - Extended operation temperature range
  - RoHS compliant

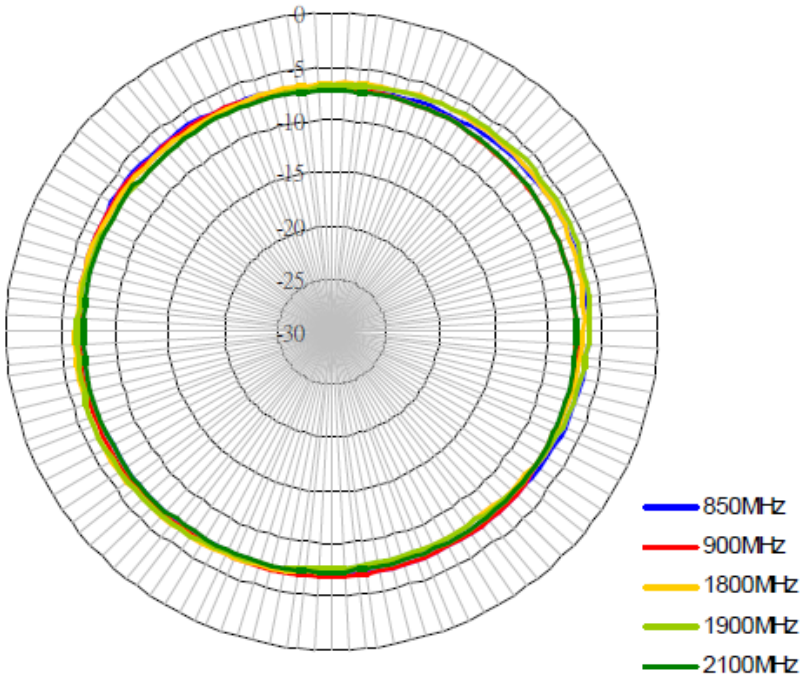
Communication System	Penta-band Cellular				
	AMPS	GSM	DCS	PCS	UMTS
Frequency (MHz)	824 ~ 896	880 ~ 960	1710 ~ 1880	1850 ~ 1990	1710 ~ 2170
Average Efficiency	19%	21%	27%	24%	23%
Peak Gain (dBi)	1.4	1.4	0.1	-1.0	-0.1
Average Efficiency	22%	23%	23%	22%	22%
Peak Gain (dBi)	1.7	1.6	-0.2	-20.	-0.2
Impedance	50 Ohm				
Radiation Pattern	Omni-directional				
Polarization	Linear				
Power Rating	10W				
Connector	ipex				
Cable	ψ 1.13				
Cable Length	50 mm				
Operation Temperature	-40° C ~ +85° C				
Storage Temperature	-40° C ~ +105° C				

E-Plane Radiation Pattern Straight



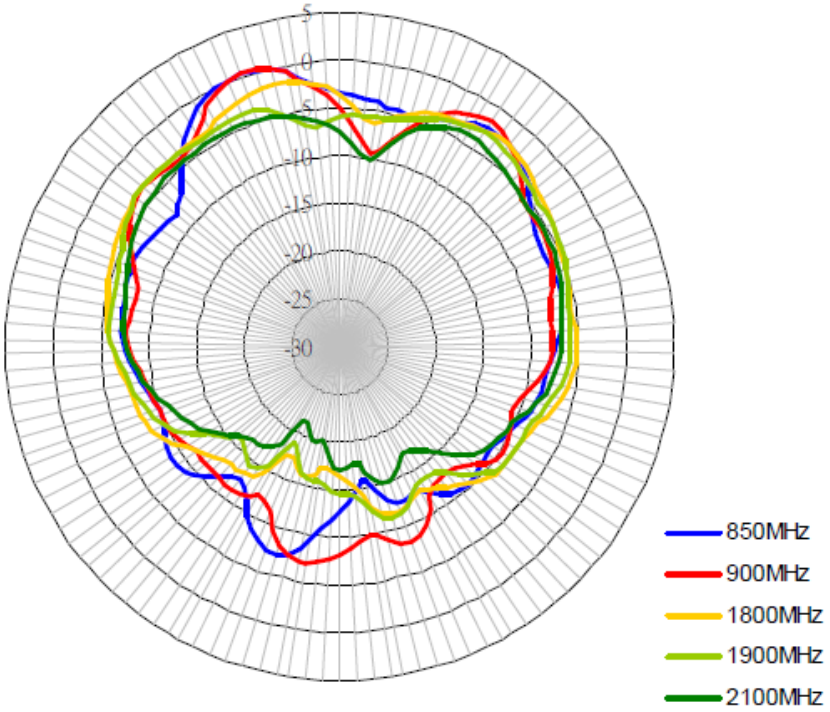
E-plane radiation pattern of TG.09 straight.

H-Plane Radiation Pattern Straight



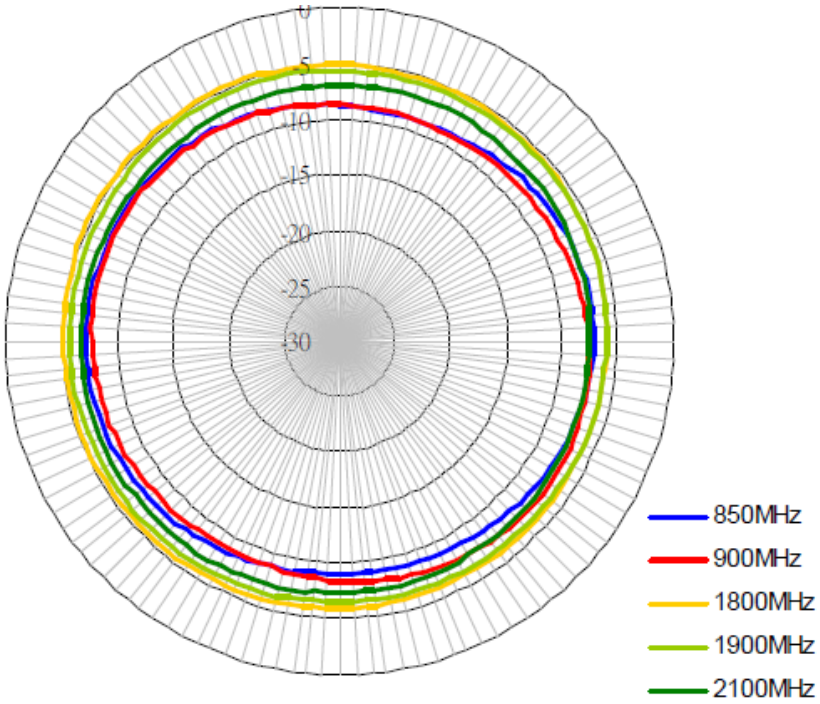
H-plane radiation pattern of TG.09 straight.

E-Plane Radiation Pattern 90° Bend



E-plane radiation pattern of TG.09 with 90° bend

H-Plane Radiation Pattern 90° Bend



H-plane radiation pattern of TG.09 with 90° bend

ConnectCore 3G 9P 9215 GPS Antenna GPS-X-02021

Mechanical Data

Parameter	Specification
Weight	≤ 105 grams
Size	48 x 40 x 13 mm
Cable	5m RG 174 standard
Connector	SMA, SMB, MCX
Mounting	Magnetic base
Housing color	Black

Electrical Specification

Parameter	Specification
Frequency	1575 ± 3 MHz
VSWR	max. 2
Bandwidth	min. 10 MHz
Impedance	50 Ω
Peak Gain	4 dBic min. (on 70cm x 7cm ground plate)
Gain Coverage	≥ -4 dBic at -90° ≤ ≤ 90° (over 75% volume)
Power handling	1 watt
Polarization	RHCP
Amplifier Gain	typ. 27 dB (without cable)
Noise Figure	typ. 1.5 dB
Output VSWR	max 2.0
Filtering	-35 dB (± 100 MHz)
DC Voltage	2.7 to 6.0 VDC
DC Current	typ. 8.5 mA, ± 4.5 mA

Environmental Specification

Parameter	Specification
Operating Temperature	-40° C ~ +85° C
Storage Temperature	-40° C ~ +85° C
Vibration	Sine sweep, 1G (0-P), 10-150-10Hz each axis
Humidity	95% ~ 100% RH

Appendix B:Certifications

The ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 products comply with the standards cited in this section.

FCC Part 15 Class B

Radio Frequency Interface (RFI) (FCC 15.105)

The ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 modules have been tested and found to comply with the limits for Class B digital devices pursuant to Part 15 Subpart B, of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try and correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Labeling Requirements (FCC 15.19)

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

If the FCC ID is not visible when installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module FCC ID. THis exterior label can use wording such as the following: “Contains Transmitter Module FCC ID: MCQ-50M1589/ IC: 1846A-50M1589”.

RF Exposure

RF exposure considerations require that a 20 cm separation distance between users and the installed antenna location shall be maintained at all times when the module is energized. OEM installers must consider suitable module and antenna installation locations in order to assure this 20 cm separation, and end users must be also be advised of the requirement.

Modifications (FCC 15.21)

Changes or modifications to this equipment not expressly approved by Digi may void the user’s authority to operate this equipment.

Industry Canada

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le present appareil numerique n’emet pas de bruits radioelectriques depassant les limites applicables aux appareils numeriques de la class B prescrites dans le Reglement sur le brouillage radioelectrique edicte par le ministere des Communications du Canada.

The maximum antenna gain permitted in the bands 5250-5350 MHz and 5470-5725 MHz to comply with the e.i.r.p. limit is, according to RSS-210 section A9.2(2) :

- 250mW conducted power
- 1.0W max EIRP

This limit is met with the highest gain antenna listed, World Products Inc WPANTE3.

The maximum antenna gain permitted in the band 5725-5825 MHz to comply with the e.i.r.p. limit specified for non point-to-point operation is, according to RSS-210 section A9.2(3):

- 1W conducted power.
- 4.0W max EIRP.

This limit is met with the highest gain antenna listed, World Products Inc WPANTE3.

OEM installers and users are cautioned to take note that high-power radars are allocated as primary users (meaning they have priority) of the bands 5250-5350 MHz and 5650-5850 MHz and these radars could cause interference and/or damage to devices operating in these frequency bands.

Indoor/Outdoor

When the ConnectCore Wi-9P 9215 module is installed in devices that can be used outdoors, the channels in the band 5150-5250 MHz must be disabled to comply with US and Canadian regulatory requirements. The OEM users are encouraged to inform end users of this restriction as well.

Declaration of Conformity

(In accordance with FCC Dockets 96-208 and 95-19)

Manufacturer's Name:	Digi International
Corporate Headquarters:	11001 Bren Road East Minnetonka MN 55343
Manufacturing Headquarters:	10000 West 76th Street Eden Prairie MN 55344

Digi International declares that the product:

Product Name	ConnectCore 9P 9215
Model Numbers:	FS-3029 FS-3038

and the product:

Product Name	ConnectCore Wi- 9P 9215
Model Numbers:	FS-3044

to which this declaration relates, meet the requirements specified by the Federal Communications Commission as detailed in the following specifications:

- Part 15, Subpart B, for Class B equipment
- FCC Docket 96-208 as it applies to Class B personal
- Personal computers and peripherals

The product listed above has been tested at an External Test Laboratory certified per FCC rules and has been found to meet the FCC, Part 15, Class B, Emission Limits. Documentation is on file and available from the Digi International Homologation Department.

ConnectCore 3G 9P 9215:

Qualcomm Gobi 2000 Module Certifications

- TIA/EIA IS-98E (CDMA2000)
- TIA/EIA IS-866 (1xEV-DO)
- TS 25.101 (UMTS)
- TS 45.005 (GSM)
- CTIA/GCF/PTCRB
- FCC
  - 47 CFR Part 1, RF radiation exposure limits
  - 47 CFR Part 2, equipment authorization
  - 47 CFR Part 15, unintentional radiators
  - 47 CFR Part 22, cellular
  - 47 CFR Part 24, PCS
- CE
  - EMC protection requirements
    - EN 301 489-1, common technical requirements
    - EN 301 489-7, GSM and DCS
    - EN 301 489-24, WCDMA 2100
    - EN 301 489-25, CDMA2000
  - Effective use of spectrum to aviod unwanted interference requirements
    - EN 301 908-1, general requirements
    - EN 301 908-2, WCDMA 2100
    - EN 301 908-4, CDMA2000
    - EN 301 511 GSM900/1800
    - EN 301 607-1 GSM900/1800
- UICC: TS 51.101 & IEC-6801-3
  - Compliance dependent on platform characteristics
- USB 2.0 High Speed

  - Compliance dependent on platform characteristics
- Safety: EN 50360/61 full carrier certification
- Microsoft WHQL certification
- ROHS compliance

International EMC Standards

The ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 meet the following standards:

Standards	ConnectCore 9P 9215
Emissions	FCC Part 15 Subpart B ICES-003
Immunity	EN 55022 EN 55024
Safety	UL 60950-1 CSA C22.2, No. 60950-1 EN60950-1

Appendix C: ConnectCore 3G 9P 9215 Strapping

This Appendix discusses strapping options for the ConnectCore 3G 9P 9215 module.

Digi Plug-and-Play firmware based products allow for customization of the software to allow for different baseboard designs. Strapping options allow the user to select the number of serial ports that the Plug-and-Play uses.

Strapping Options

The ConnectCore 3G 9P 9215 module can be strapped to include zero to three serial ports. The fewer serial ports enabled, the more GPIOs available for a Python application. The strapping is defined by the SW_CONF0, SW_CONF1, SW_CONF2 and SW_CONF3 switch settings on S4 "Configuration Switches," which is next to the JTAG connector. The default is to have two serial ports enabled (all switches off).

The strapping is defined as:

Number of Serial Ports	SW_CONF0	SW_CONF1	SW_CONF2	SW_CONF3
0	OFF	ON	ON	ON
1	ON	OFF	ON	ON
2	ON	ON	ON	ON
3	OFF	OFF	ON	ON

The serial ports on the developement board are labeled D, B and A. They are enabled according to the S4 Configuration Switch settings:

Number of Serial Ports Enabled	Port(s) Enabled on the Development Board
1	B
2	B and D
3	B, D and A

Appendix D: ConnectCore 3G 9P 9215 GPIO

This appendix describes the GPIOs available on the ConnectCore 3G 9P 9215 module. These pins are accessible through the GPIO Python API.

The table below shows the available GPIOs.

The first column in the table lists the pin on the module connector. The second column lists the GPIO available when configured for zero serial ports. The third column for one port, and so on.

Some pins have dual purpose, such as GPIO68, which could also be used for EXT_SIM_VCC. So if the external SIM function is being used, GPIO68 is not available.

A description of the Python API can be found here:

http://www.digi.com/wiki/developer/index.php/Digihw

Note: The information in this section of the document applies to Digi Plug-and-Play firmware variants of the ConnectCore 3G 9P 9215 module only.

GPIO

Module Pin (Python Name)	0001 (0 Serial Ports)	0010 (1 Serial Port)	0000 (2 Serial Ports)	0011 (3 Serial Ports)	Comments
X2_3	GPIO0	GPIO0	GPIO0	DCD2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_ON_SLEEP
X2_4	GPIO1	GPIO1	GPIO1	CTS2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_CTS
X2_5	GPIO2	GPIO2	GPIO2	DSR2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_RESET
X2_6	GPIO3	GPIO3	GPIO3	RXD2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_DOUT
X2_7	GPIO4	GPIO4	GPIO4	RI2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_LINKACT
X2_8	GPIO5	GPIO5	GPIO5	RTS2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_RTS
X2_9	GPIO6	GPIO6	GPIO6	DTR2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_DTR
X2_10	GPIO7	GPIO7	GPIO7	TXD2	If XBEE is enabled this signal is not available. Instead it is used as XBEE_DIN
X2_19	GPIO51	DCD0	DCD0	DCD0	
X2_20	GPIO52	CTS0	CTS0	CTS0	
X2_21	GPIO53	DSR0	DSR0	DSR0	
X2_22	GPIO54	RXD0	RXD0	RXD0	
X2_23	GPIO55	RI0	RI0	RI0	
X2_24	GPIO56	RTS0	RTS0	RTS0	
X2_25	GPIO57	DTR0	DTR0	DTR0	
X2_26	GPIO58	TXD0	TXD0	TXD0	
X2_27	GPIO59	GPIO59	DCD1	DCD1	
X2_28	GPIO60	GPIO60	CTS1	CTS1	
X2_29	GPIO61	GPIO61	DSR1	DSR1	
X2_30	GPIO62	GPIO62	RXD1	RXD1	
X2_31	GPIO63	GPIO63	RI1	RI1	
X2_32	GPIO64	GPIO64	RTS1	RTS1	
X2_33	GPIO65	GPIO65	DTR1	DTR1	
X2_34	GPIO66	GPIO66	TXD1	TXD1	

Module Pin (Python Name)	0001 (0 Serial Ports)	0010 (1 Serial Port)	0000 (2 Serial Ports)	0011 (3 Serial Ports)	Comments
X2_35	GPIO67	GPIO67	GPIO67	GPIO67	
X2_36	GPIO68	GPIO68	GPIO68	GPIO68	For the external SIM variant, this signal is not available. Instead it is used as EXT_SIM_VCC
X2_37	GPIO69	GPIO69	GPIO69	GPIO69	
X2_38	GPIO70	GPIO70	GPIO70	GPIO70	For the external SIM variant, this signal is not available. Instead it is used as EXT_SIM_DATA
X2_39	GPIO71	GPIO71	GPIO71	GPIO71	
X2_40	GPIO72	GPIO72	GPIO72	GPIO72	For the external SIM variant, this signal is not available. Instead it is used as EXT_SIM_CLK
X2_41	GPIO73	GPIO73	GPIO73	GPIO73	
X2_42	GPIO74	GPIO74	GPIO74	GPIO74	For the external SIM variant, this signal is not available. Instead it is used as EXT_SIM_RST
X2_43	GPIO75	GPIO75	GPIO75	GPIO75	
X2_44	GPIO76	GPIO76	GPIO76	GPIO76	
X2_45	GPIO77	GPIO77	GPIO77	GPIO77	
X2_46	GPIO78	GPIO78	GPIO78	GPIO78	
X2_47	GPIO79	GPIO79	GPIO79	GPIO79	
X2_48	GPIO80	GPIO80	GPIO80	GPIO80	
X2_50	GPIO82	GPIO82	GPIO82	GPIO82	User LED1
X2_52	GPIO84	GPIO84	GPIO84	GPIO84	User button 2
X2_63	GPIO100	GPIO100	GPIO100	GPIO100	For the external SIM variant, this signal is not available. Instead it is used as EXT_SIMDETECT
X2_64	GPIO101	GPIO101	GPIO101	GPIO101	

Appendix E: Change Log

The following changes were made to this document in revisions listed below.

Revison B

1. Deleted the following non-applicable text: “Onboard flash: The module has 8Mx16 NOR by 2Mx16 NOR flash onboard. Greater sizes can optionally be populated, if available. “
2. Replaced “Current measurements with FIM (DRPIC) enabled” and “Current measurements with FIM (DRPIC) disabled” with “Typical module current / power measurements” and “Typical power save module / JumpStart board current / power consumption measurements.”

Revision C

1. On page 9 updated Digi information.
2. On page 43 within Serial Port B MEI configuration switches table, deleted no applicable reference to RS422/RS485 regarding S1.1.
3. On page 48 corrected Serial UART ports figure callout arrows.
4. On page 60 regarding POWE_GND, corrected from X24 to X26.4 and X26.5.
5. On page 72 corrected figure of module top.

Revision D

1. Made additions necessary to accomodate additional device, CCWi-9P 9215.

Revision E

1 Made corrections to current draw information.

Revision F

1 Minor data corrections were made and Canadian certifications information was expanded.

Revision G

1 On page 92, corrected FCC ID number.

Revision H

1 On page 87, corrected the 5.5 dBi Dipoles antenna's part number within the attributes table.

Revision I

1 Removed "5V tolerant" from the I^2C digital I/O expansion section.

Revision J

1 Revised the WLAN Interface section of Appendix A.

Revision K

1 Added ConnectCore 3G 9P 9215 information to the manual.

Revsion L

1 Revised the Strapping Options table in Appendix C.

2 Revised the Configuration Pins section text of Chapter 1.

3 Revised the User Interface section of Chapter 2.

4 Added text describing the WWAN Interface section of Chapter 2.

5 Renamed the Typical Power Save Current /Power Measurements section ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 Typical Power Save Current/ Power Measurements in Appendix A. Also, added the ConnectCore 3G 9P 9215 Typical Power Save Current/ Power Measurements section to Appendix A.

6 Revised the Typical Module Current/ Power Measurements section ofAppendix A.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