

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.10
Q_g (Max.) (nC)	25	
Q_{gs} (nC)	5.8	
Q_{gd} (nC)	11	
Configuration	Single	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Advanced Process Technology
- Surface Mount (IRFZ24S, SiHFZ24S)
- Low-Profile Through-Hole (IRFZ24L, SiHFZ24L)
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



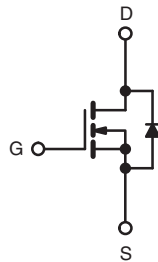
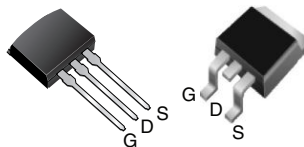
RoHS*
COMPLIANT
HALOGEN FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRFZ24L, SiHFZ24L) is available for low-profile applications.

I²PAK (TO-262) D²PAK (TO-263)



N-Channel MOSFET

ORDERING INFORMATION			
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFZ24S-GE3	SiHFZ24STRR-GE3	-
Lead (Pb)-free	IRFZ24SPbF	-	IRFZ24LPbF
	SiHFZ24S-E3	-	SiHFZ24L-E3

Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	I_D	17	A
		$T_C = 100$ °C		12	
Pulsed Drain Current ^{a, e}			I_{DM}	68	
Linear Derating Factor				0.40	W/°C
Single Pulse Avalanche Energy ^{b, e}			E_{AS}	100	mJ
Maximum Power Dissipation	$T_C = 25$ °C		P_D	60	W
	$T_A = 25$ °C			3.7	
Peak Diode Recovery dV/dt ^{c, e}			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 400$ μ H, $R_g = 25$ Ω , $I_{AS} = 17$ A (see fig. 12).
- $I_{SD} \leq 17$ A, $di/dt \leq 140$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.
- Uses IRFZ24, SiHFZ24 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, Steady-State) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^c$	-	0.061	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 10\text{ A}^b$	-	-	0.10	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 10\text{ A}^d$	5.5	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 ^d	-	640	-	pF
Output Capacitance	C_{oss}		-	360	-	
Reverse Transfer Capacitance	C_{rss}		-	79	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$ $I_D = 17\text{ A}, V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^{b, c}	-	-	25	nC
Gate-Source Charge	Q_{gs}		-	-	5.8	
Gate-Drain Charge	Q_{gd}		-	-	11	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 17\text{ A}, R_g = 18\text{ }\Omega, R_D = 1.7\text{ }\Omega$, see fig. 10 ^{b, c}	-	13	-	ns
Rise Time	t_r		-	58	-	
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	
Fall Time	t_f		-	42	-	
Internal Source Inductance	L_S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	17	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	68	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b, c$	-	88	180	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	290	640	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. Uses IRFZ24/SiHFZ24 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

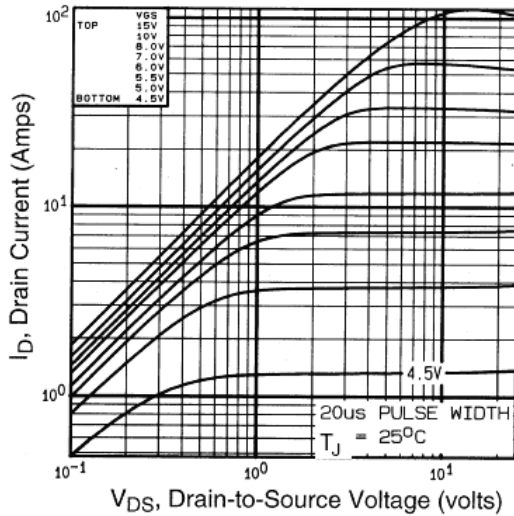


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

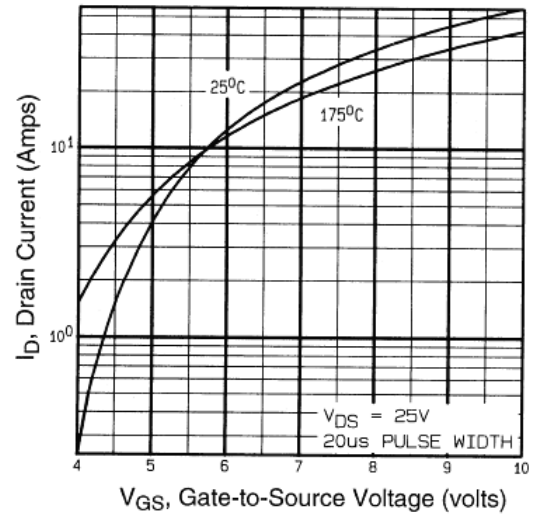


Fig. 3 - Typical Transfer Characteristics

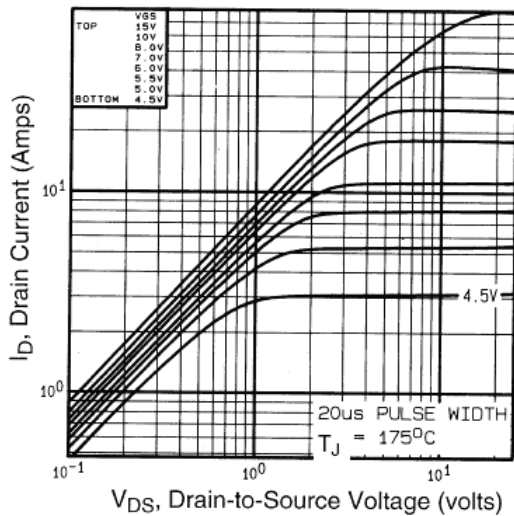


Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$

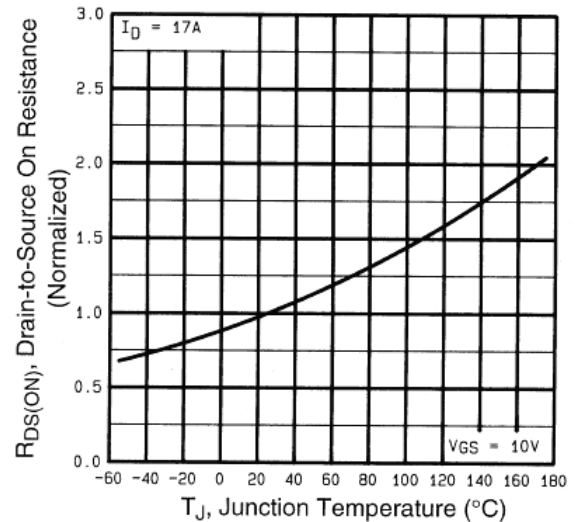


Fig. 4 - Normalized On-Resistance vs. Temperature

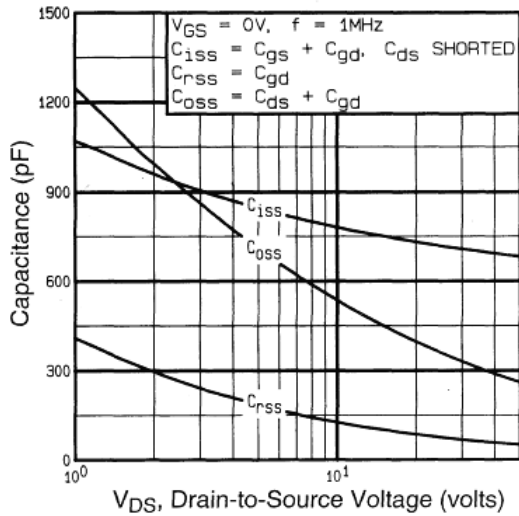


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

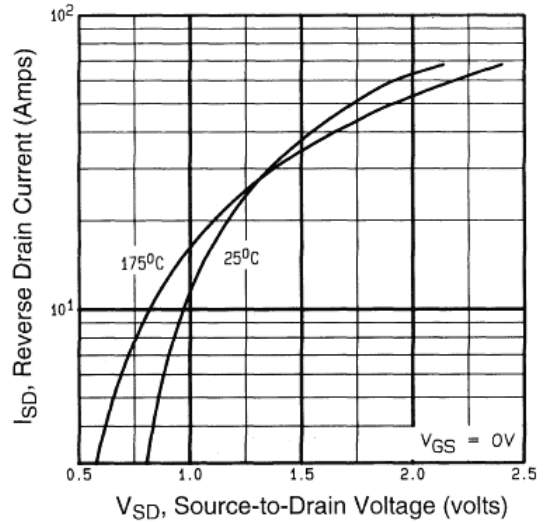


Fig. 7 - Typical Source-Drain Diode Forward Voltage

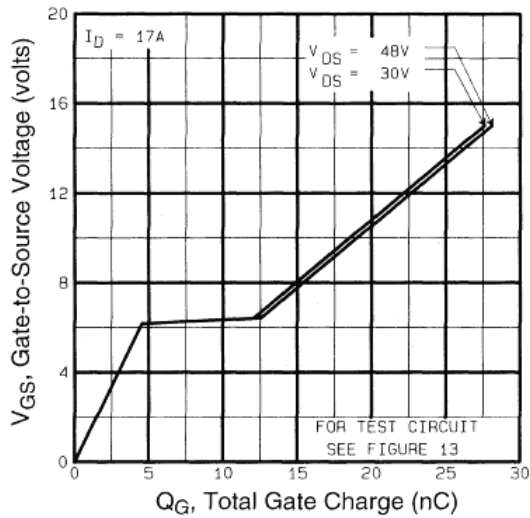


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

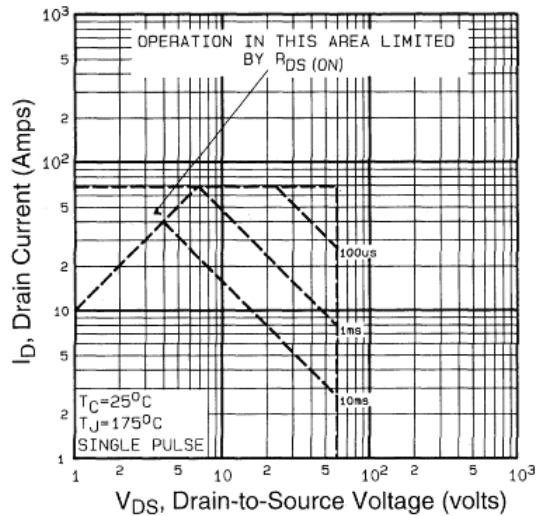


Fig. 8 - Maximum Safe Operating Area

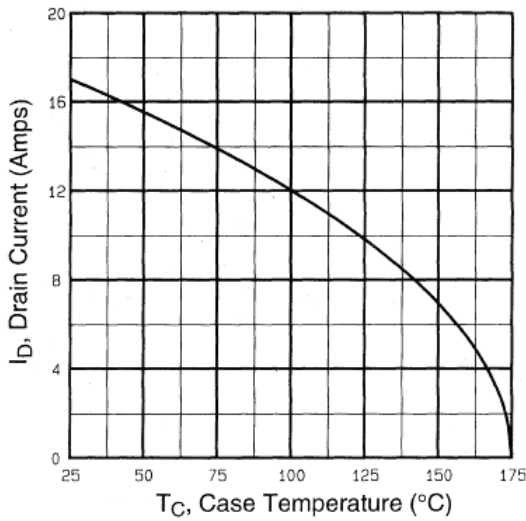


Fig. 9 - Maximum Drain Current vs. Case Temperature

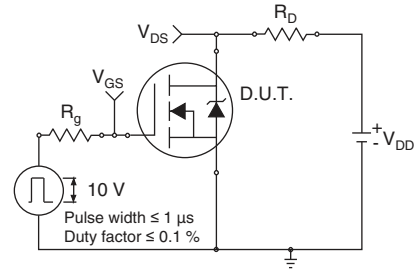


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

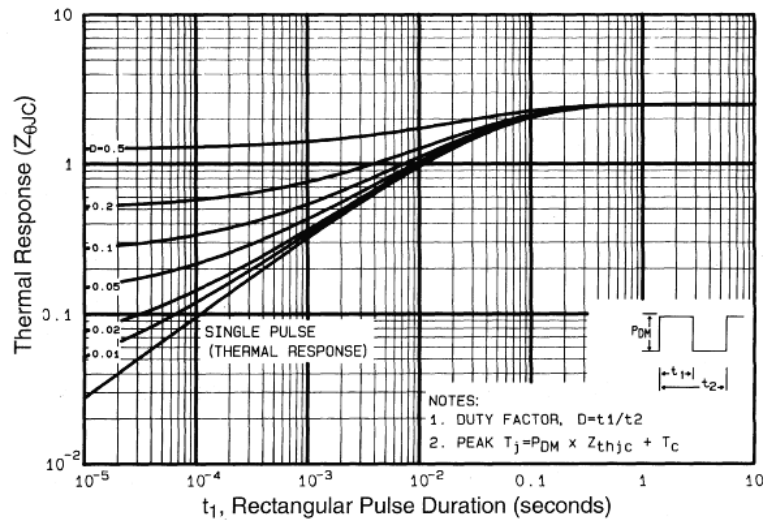


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

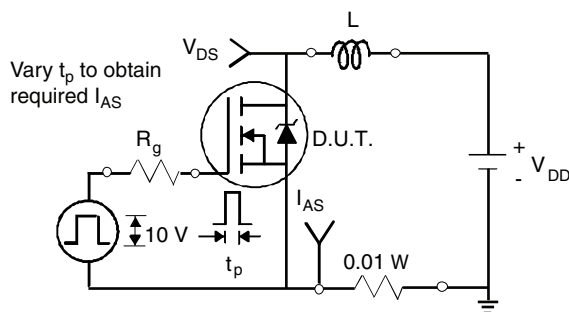


Fig. 12a - Unclamped Inductive Test Circuit

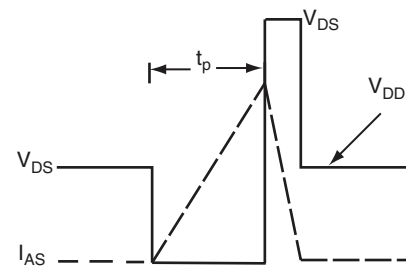


Fig. 12b - Unclamped Inductive Waveforms

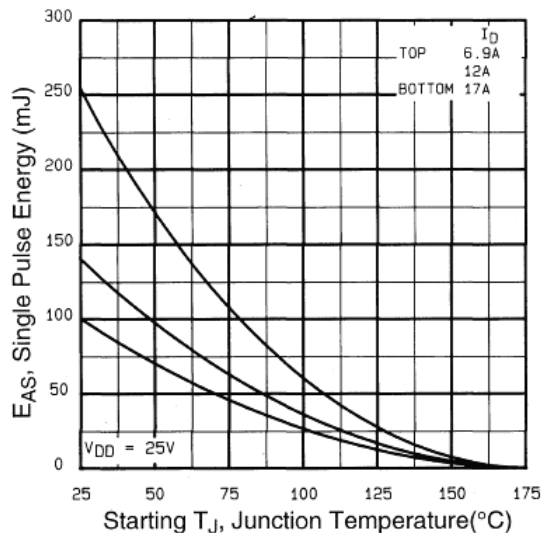


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

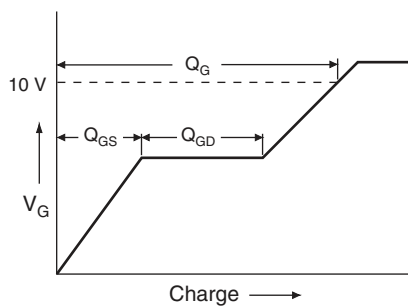


Fig. 13a - Basic Gate Charge Waveform

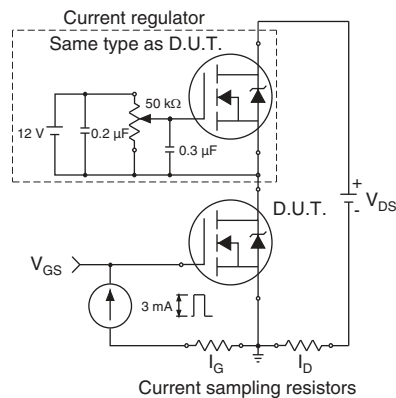


Fig. 13b - Gate Charge Test Circuit



Note

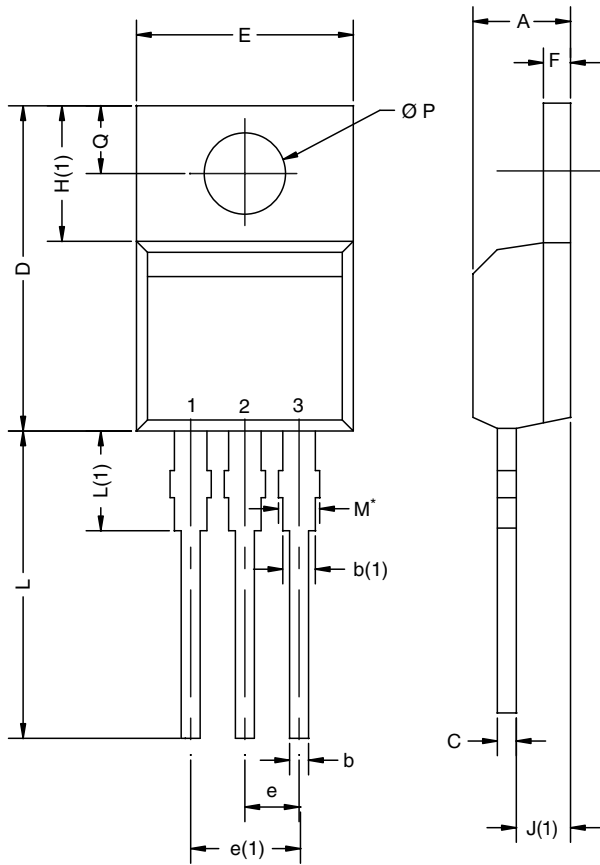
a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T13-0724-Rev. O, 14-Oct-13
DWG: 5471

Note

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM



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