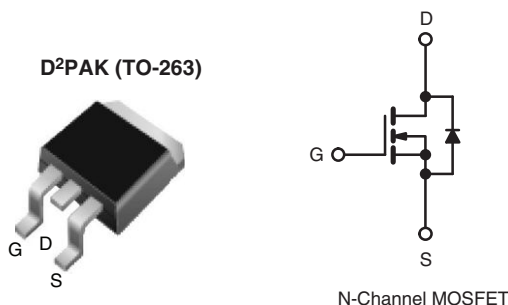


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0$ V	0.028
Q_g (Max.) (nC)	66	
Q_{gs} (nC)	12	
Q_{gd} (nC)	43	
Configuration	Single	



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4$ V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D2PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D2PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

Package	D2PAK (TO-263)	D2PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHLZ44S-GE3	SiHLZ44STRR-GE3 ^a
Lead (Pb)-free	IRLZ44SPbF	IRLZ44STRRPbF ^a
	SiHLZ44S-E3	SiHLZ44STR-E3 ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 10	
Continuous Drain Current ^f	I_D	$T_C = 25$ °C	A
Continuous Drain Current		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	200	
Linear Derating Factor		1.0	W/°C
Linear Derating Factor (PCB Mount) ^e		0.025	
Single Pulse Avalanche Energy ^b	E_{AS}	400	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
Maximum Power Dissipation (PCB Mount) ^e		$T_A = 25$ °C	
Peak Diode Recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 179$ μ H, $R_g = 25$ Ω , $I_{AS} = 51$ A (see fig. 12).
- $I_{SD} \leq 51$ A, $dI/dt \leq 250$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).
- Current limited by the package, (die current = 51 A).

* Pb containing terminations are not RoHS compliant, exemptions may apply

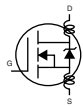
THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

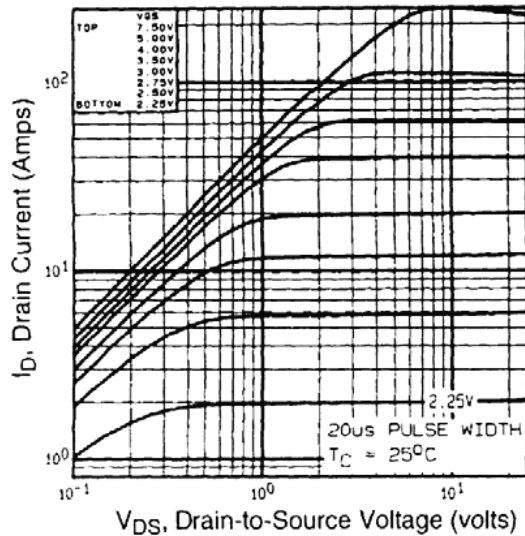
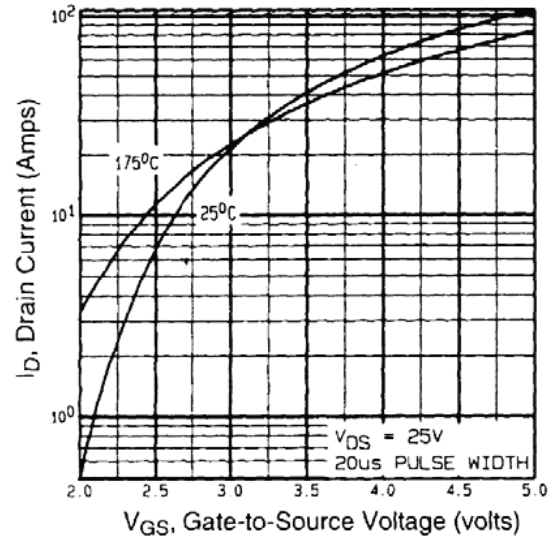
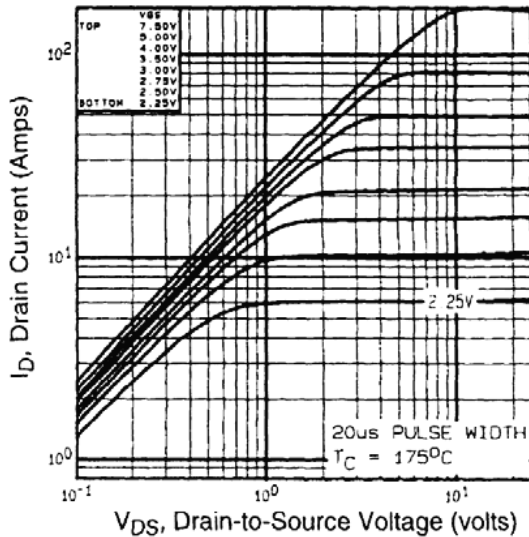
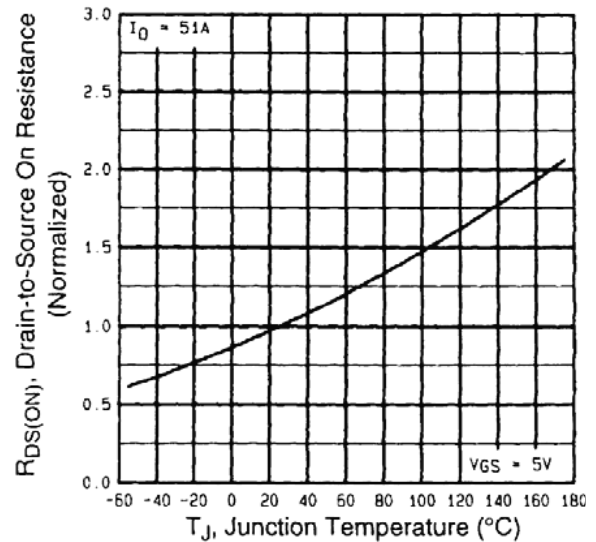
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.070	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	2.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 5.0 V	I _D = 31 A ^b	-	-	0.028	Ω
		V _{GS} = 4.0 V	I _D = 25 A ^b	-	-	0.039	
Forward Transconductance	g _{fs}	V _{DS} = 25 V, I _D = 31 A ^b		23	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	3300	-	pF
Output Capacitance	C _{oss}			-	1200	-	
Reverse Transfer Capacitance	C _{rss}			-	200	-	
Total Gate Charge	Q _g	V _{GS} = 5.0 V	I _D = 51 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	66	nC
Gate-Source Charge	Q _{gs}			-	-	12	
Gate-Drain Charge	Q _{gd}			-	-	43	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 51 A, R _g = 4.6 Ω, R _D = 0.56 Ω, see fig. 10 ^b		-	17	-	ns
Rise Time	t _r			-	230	-	
Turn-Off Delay Time	t _{d(off)}			-	42	-	
Fall Time	t _f			-	110	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	50°	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	200	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 51 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 51 A, dI/dt = 100 A/μs ^b		-	130	180	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.84	1.3	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. Current limited by the package, (Die Current = 51 A).

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

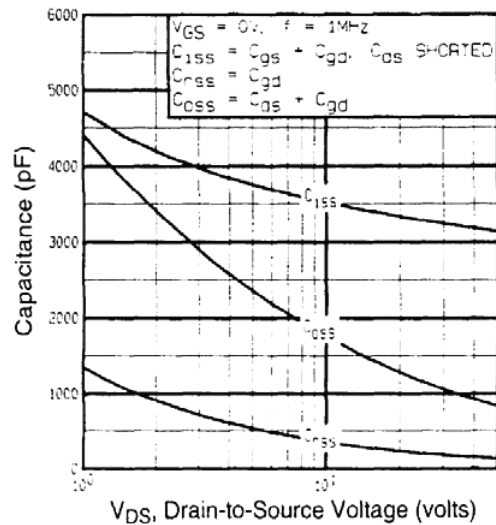


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

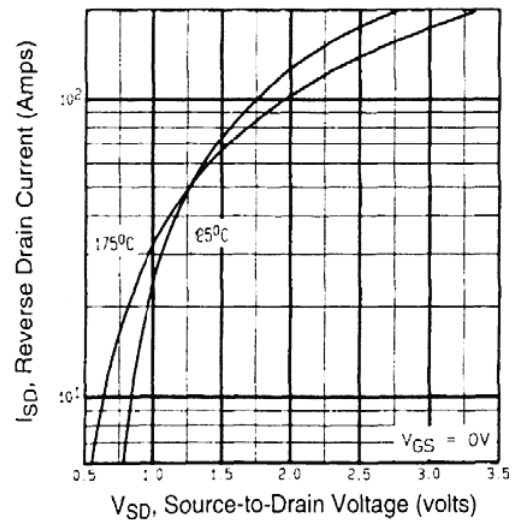


Fig. 7 - Typical Source-Drain Diode Forward Voltage

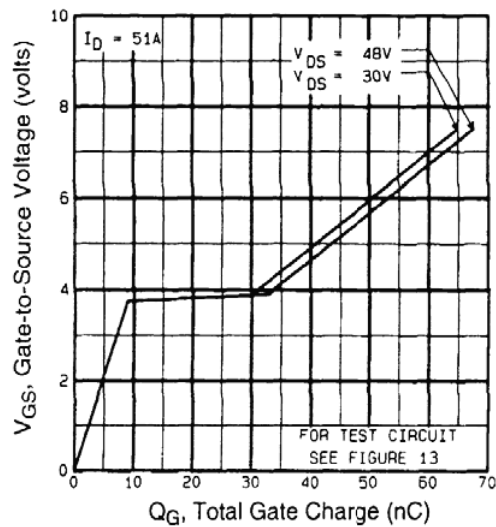


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

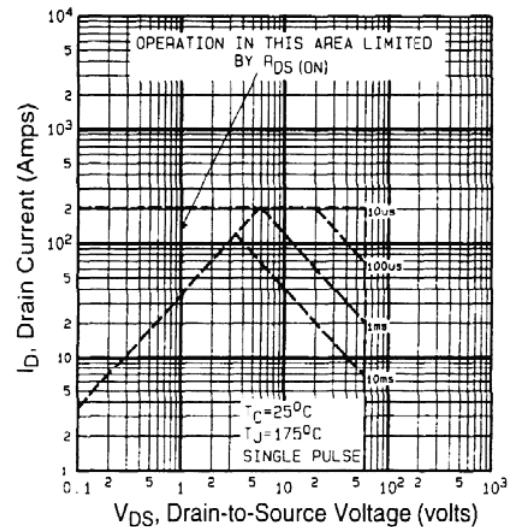
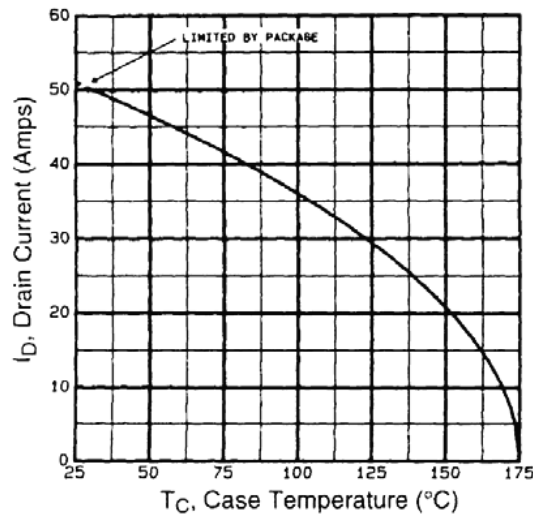
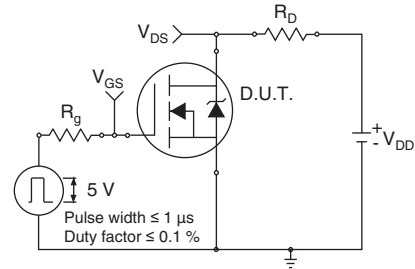
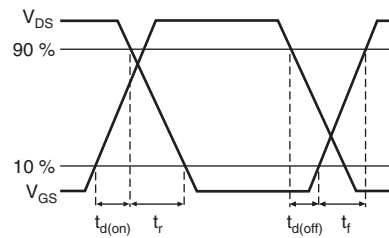
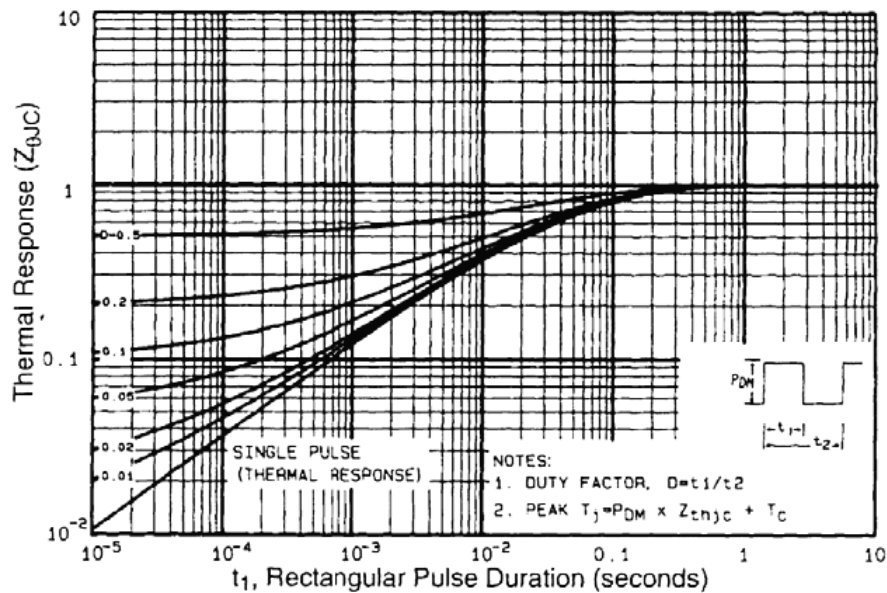


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

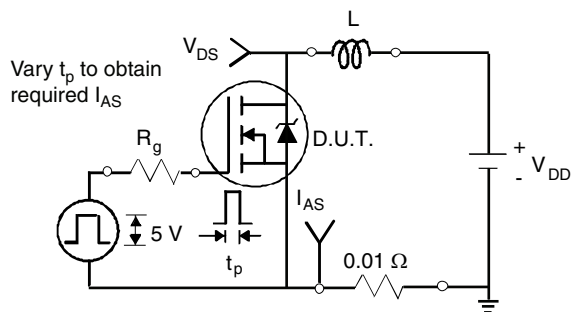


Fig. 12a - Unclamped Inductive Test Circuit

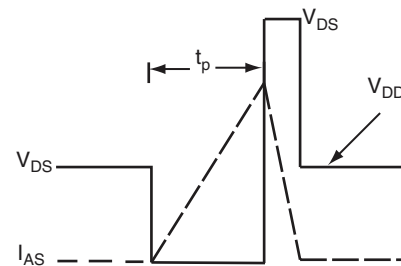


Fig. 12b - Unclamped Inductive Waveforms

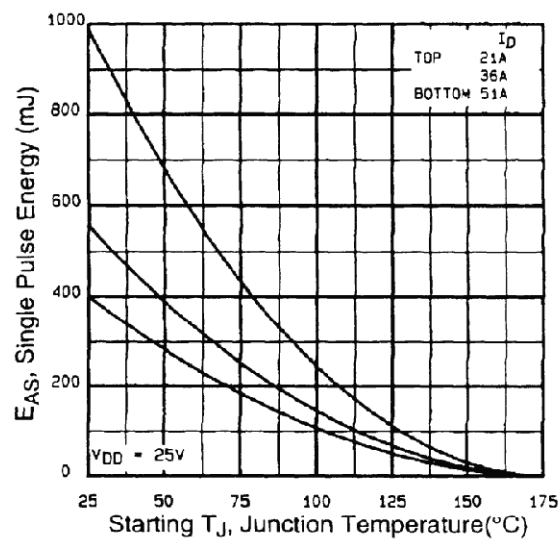


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

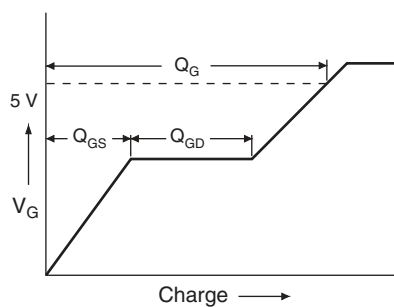


Fig. 13a - Basic Gate Charge Waveform

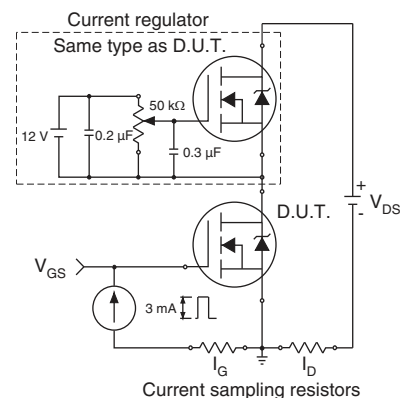
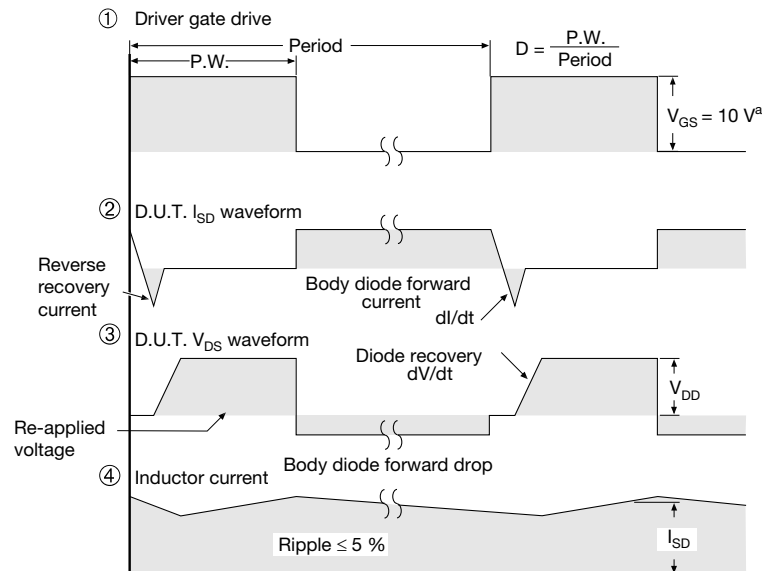
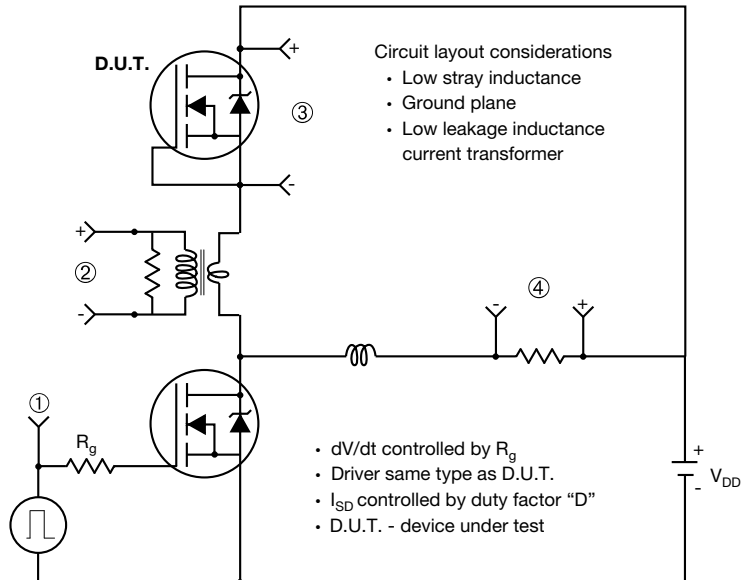


Fig. 13b - Gate Charge Test Circuit

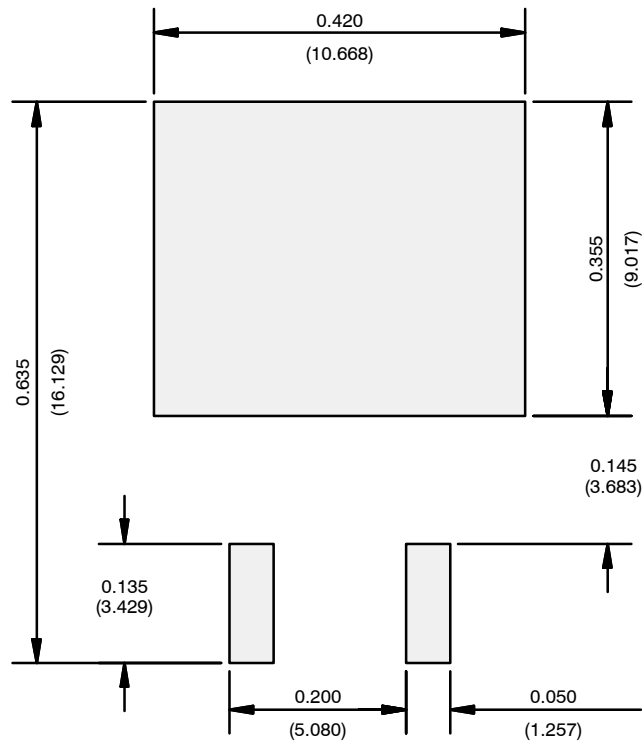
Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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