Preliminary - Source Control Drawing

Part Description:	**3*3*0.9 mm Ultra Low Power RTC IC User's Guide**
Customer Part Number:	
Abracon Part Number:	**AB18XX**

Customer Approval

(Please return this copy as a certification of your approval)

Approved by:	
Approval Date:	

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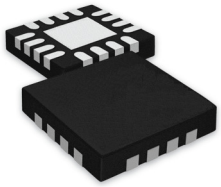
Internal Use Only	
	500192

Revision History

Revision	ECO	Description	Date	Prep'd By	Ck'd By	Ck'd By	Appr'd By
		Preliminary Release	10/25/2012	SR	YH	CB	JE
A		Initial Release	02/24/2013	SR	YH	CB	JE

AB18XX Features

- Ultra-low supply current (all at 3V):
  - 14 nA with RC oscillator
  - 18 nA with RC oscillator and autocalibration
  - 50 nA with crystal oscillator
- Baseline timekeeping features:
  - 32 kHz crystal oscillator with integrated load capacitor/resistor
  - Counters for hundredths, seconds, minutes, hours, date, month, year, century, and weekday
  - Alarm capability on all counters
  - Programmable output clock generation (32 kHz to 1/year)
  - Countdown timer with repeat function
  - Automatic leap year calculation
- Advanced timekeeping features:
  - Integrated power optimized RC oscillator
  - Advanced crystal calibration to ± 2 ppm
  - Advanced RC calibration to ± 16 ppm
  - Automatic calibration of RC oscillator to crystal oscillator
  - Watchdog timer with hardware reset
  - Up to 256 bytes of general purpose RAM
- Power management features:
  - Integrated ~1Ω power switch for off-chip components such as a host MCU
  - System sleep manager for managing host processor wake/sleep states
  - External interrupt monitor
  - External reset signal monitor
  - Reset output generator
  - Automatic switchover to VBAT
  - Supercapacitor trickle charger with programmable charging current
  - Programmable brown out detection
  - Programmable analog voltage comparator
- I^2C (up to 400 kHz) and 3-wire or 4-wire SPI (up to 2 MHz) serial interfaces available
- Operating voltage 1.7-3.6 V
- Clock and RAM retention voltage 1.5-3.6 V
- Operating temperature –40 to 85 °C
- All inputs include Schmitt Triggers
- 3x3 mm QFN-16 package



Applications

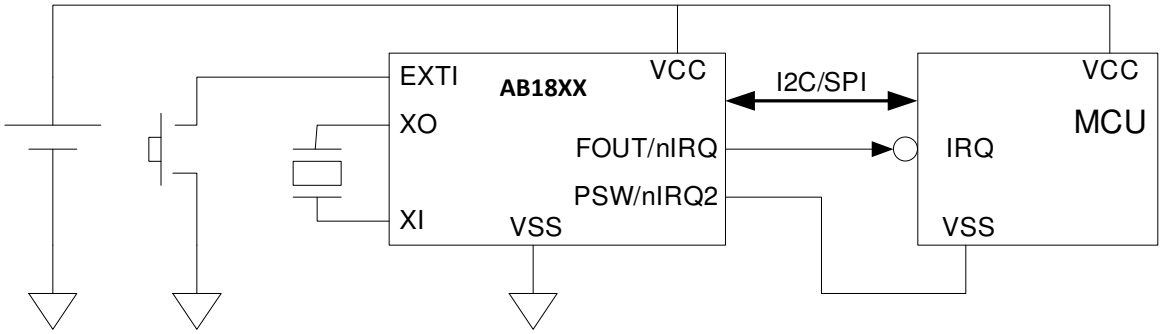
- Smart cards
- Wireless sensors and tags
- Medical electronics
- Utility meters
- Data loggers
- Appliances
- Handsets
- Consumer electronics
- Communications equipment

Description

ABRACON's AB18XX Real Time Clock with Power Management family provides a groundbreaking combination of ultra-low power coupled with a highly sophisticated feature set. With power requirements significantly lower than any other industry RTC (as low as 14 nA), these are the first semiconductors based on Innovative SPOT (Subthreshold Power Optimized Technology) CMOS platform. The AB18XX includes on-chip oscillators to provide minimum power consumption, full RTC functions including battery backup and programmable counters and alarms for timer and watchdog functions, and either an I^2C or SPI serial interface for communication with a host controller. An integrated power switch and a sophisticated system sleep manager with counter, timer, alarm, and interrupt capabilities allows the AB18XX to be used as a supervisory component in a host microcontroller-based system.

Disclaimer: AB18XX series of devices are based on Innovative SPOT technology, proprietary to Ambiq Micro.

Typical AB18XX Application Circuit



Recommended Tuning Fork Crystal:

ABS07-120-32.768kHz-T

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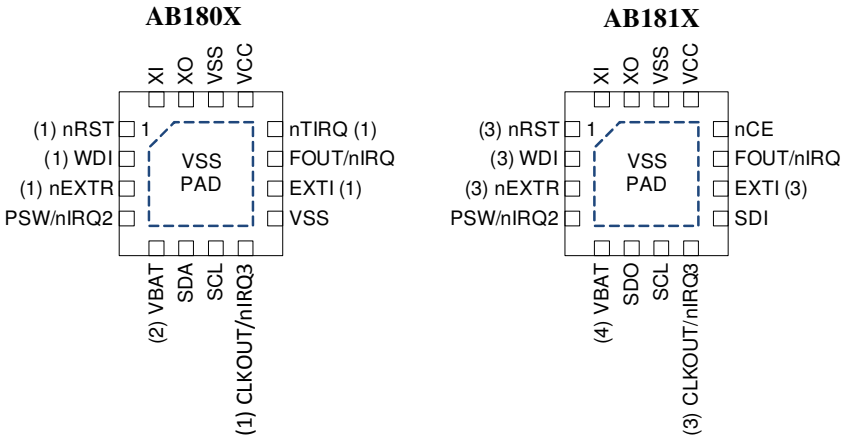
1. Family Summary

The AB18XX family consists of several members. All devices are supplied in a standard 3x3 mm QFN-16 package. Members of the software and pin compatible AB08XX RTC family are also listed.

Part #	Baseline Timekeeping		Advanced Timekeeping				Power Management				Interface
	XT Osc	Number of GP Outputs	RC Osc	Calib/ Auto-calib	Watch-dog	RAM (B)	VBAT Switch	Reset Mgmt	Ext Int	Power Switch and Sleep FSM	
AB1801	■	2	■	■		0				■	I^2C
AB1803	■	2	■	■		64	■			■	I^2C
AB1804	■	4	■	■	■	256		■	■	■	I^2C
AB1805	■	4	■	■	■	256	■	■	■	■	I^2C
AB1811	■	2	■	■		0				■	SPI
AB1813	■	2	■	■		64	■			■	SPI
AB1814	■	3	■	■	■	256		■	■	■	SPI
AB1815	■	3	■	■	■	256	■	■	■	■	SPI
Software and Pin Compatible AB08XX Family Components											
AB0801	■	2	■	■		0					I2C
AB0803	■	2	■	■		64	■				I2C
AB0804	■	4	■	■	■	256			■		I2C
AB0805	■	4	■	■	■	256	■		■		I2C
AB0811	■	2	■	■		0					SPI
AB0813	■	2	■	■		64	■				SPI
AB0814	■	3	■	■	■	256			■		SPI
AB0815	■	3	■	■	■	256	■		■		SPI

2. AB18XX Pin Descriptions

The AB18XX family includes a variety of packaged versions. Figure 1 and Table 1 show the QFN-16 pin configurations for the AB18XX parts. Pins labeled NC must be left unconnected. The thermal pad on the QFN-16 packages must be connected to VSS.



(1) Available in AB1804 & AB1805 **only**, else No Connect
(2) Available in AB1803 & AB1805 **only**, else VSS
(3) Available in AB1814 & AB1815 **only**, else No Connect
(4) Available in AB1813 & AB1815 **only**, else VSS

Figure 1 – AB18XX Production Pin Configuration Diagrams

Table 1 – AB18XX Pin Connections

Pin Name	Pin Type	Function	Pin Number in AB18XX							
			01	03	04	05	11	13	14	15
VSS	Power	Ground	5, 9, 14	9, 14	5, 9, 14	9, 14	5, 14	14	5, 14	14
VCC	Power	System power supply	13	13	13	13	13	13	13	13
XI	XT	Crystal input	16	16	16	16	16	16	16	16
XO	XT	Crystal output	15	15	15	15	15	15	15	15
VBAT	Power	Battery power supply		5		5		5		5
SCL	Input	I^2C or SPI interface clock	7	7	7	7	7	7	7	7
SDO	Output	SPI data output					6	6	6	6
SDI	Input	SPI data input					9	9	9	9
nCE	Input	SPI chip select					12	12	12	12
SDA	Input	I^2C data input/output	6	6	6	6				
EXTI	Input	External interrupt input			10	10			10	10
WDI	Input	Watchdog reset input			2	2			2	2
nEXTR	Input	External reset input			3	3			3	3
FOUT/nIRQ	Output	Interrupt 1/function output	11	11	11	11	11	11	11	11
PSW/nIRQ2	Output	Interrupt 2/power switch output	4	4	4	4	4	4	4	4
CLKOUT/nIRQ3	Output	Interrupt 3/clock output			8	8			8	8
nTIRQ	Output	Timer interrupt output			12	12				
nRST	Output	Reset output			1	1			1	1

2.1 VSS

This is the ground connection of the AB18XX. In the QFN-16 packages the ground slug on the bottom of the package must be connected to VSS.

2.2 VCC

This is the primary power connection of the AB18XX. If a single power supply is used, it must be connected to VCC.

2.3 VBAT

This is the battery backup power connection of the AB18XX. If a backup battery is not present, VBAT is normally left floating or grounded, but it may also be used to provide the analog input to the internal comparator (see Section 4.12.2).

2.4 XI

This is the crystal oscillator input connection of the AB18XX.

2.5 XO

This is the crystal oscillator output connection of the AB18XX.

2.6 SCL

This is the I/O interface clock connection of the AB18XX. It provides the SCL input in both I^2C and SPI interface modes.

2.7 SDA (only available in I^2C environments)

This is the I/O interface I^2C data connection of the AB18XX.

2.8 SDO (only available in SPI environments)

This is the I/O interface SPI data output connection of the AB18XX.

2.9 SDI

This is the I/O interface SPI data input connection of the AB18XX. It must be left floating or connected to VCC in I^2C environments.

2.10 nCE (only available in SPI environments)

This is the I/O interface SPI chip select input connection of the AB18XX. It is an active low signal.

2.11 EXTI

This is the external interrupt input connection of the AB18XX. It may be used to generate an EXT1 interrupt with polarity selected by the EX1P bit if enabled by the EX1E bit. The value of the EXTI pin may be read in the EXIN register bit.

2.12 WDI

This is the Watchdog Timer reset input connection of the AB18XX. It may also be used to generate an EXT2 interrupt with polarity selected by the EX2P bit if enabled by the EX2E bit. The value of the WDI pin may be read in the WDIN register bit.

2.13 nEXTR

This is the external reset input connection of the AB18XX. If nEXTR is low and the RS1E bit is set, the nRST output will be driven to its asserted value as determined by the RSP bit.

2.14 FOUT/nIRQ

This is the primary interrupt output connection of the AB18XX. It may operate as either an open drain or push-pull output as selected by the OUTPP bit. FOUT/nIRQ may be configured to generate several signals as a function of the OUT1S field (see Section 5.3.3). FOUT/nIRQ is also asserted low on a power up until the AB18XX has exited the reset state and is accessible via the I/O interface.

1) FOUT/nIRQ can drive the value of the OUT bit.
2) FOUT/nIRQ can drive the square wave output (see Section 5.3.5) if enabled by SQWE.
3) FOUT/nIRQ can drive the inverse of the combined interrupt signal IRQ (see Section 0).
4) FOUT/nIRQ can drive the inverse of the alarm interrupt signal AIRQ (see Section 0).

2.15 PSW/nIRQ2

This is the secondary interrupt output connection of the AB18XX. It is an open drain output. PSW/nIRQ2 may be configured to generate several signals as a function of the OUT2S field (see Section 5.3.3).

1) PSW/nIRQ2 can drive the value of the OUTB bit.
2) PSW/nIRQ2 can drive the square wave output (see Section 5.3.5) if enabled by SQWE.
3) PSW/nIRQ2 can drive the inverse of the combined interrupt signal IRQ (see Section 0).
4) PSW/nIRQ2 can drive the inverse of the alarm interrupt signal AIRQ (see Section 0).
5) PSW/nIRQ2 can drive either sense of the timer interrupt signal TIRQ.
6) PSW/nIRQ2 can function as the power switch output for controlling the power of external devices (see Section 4.15).

2.16 nTIRQ (only available in I^2C environments)

This is the timer interrupt output connection of the AB18XX. It may operate as either an open drain or push-pull output as selected by the OUTPP bit. nTIRQ always drives the active low nTIRQ signal.

2.17 CLKOUT/nIRQ3

This is the Square Wave output connection of the AB18XX. It is a push-pull output, and may be configured to generate one of two signals.

1) CLKOUT/nIRQ3 can drive the value of the OUT bit.
2) CLKOUT/nIRQ3 can drive the square wave output (see Section 5.3.5) if enabled by SQWE.

2.18 nRST

This is the external reset output connection of the AB18XX. It may operate as either an open drain or push-pull output as selected by the RSTPP bit. The polarity is selected by the RSP bit. See Section 4.11.8 for details of the generation of nRST.

2.19 AB18XX Digital Architecture Summary

Figure 2 shows the overall architecture of the pin inputs and outputs of the AB18XX.

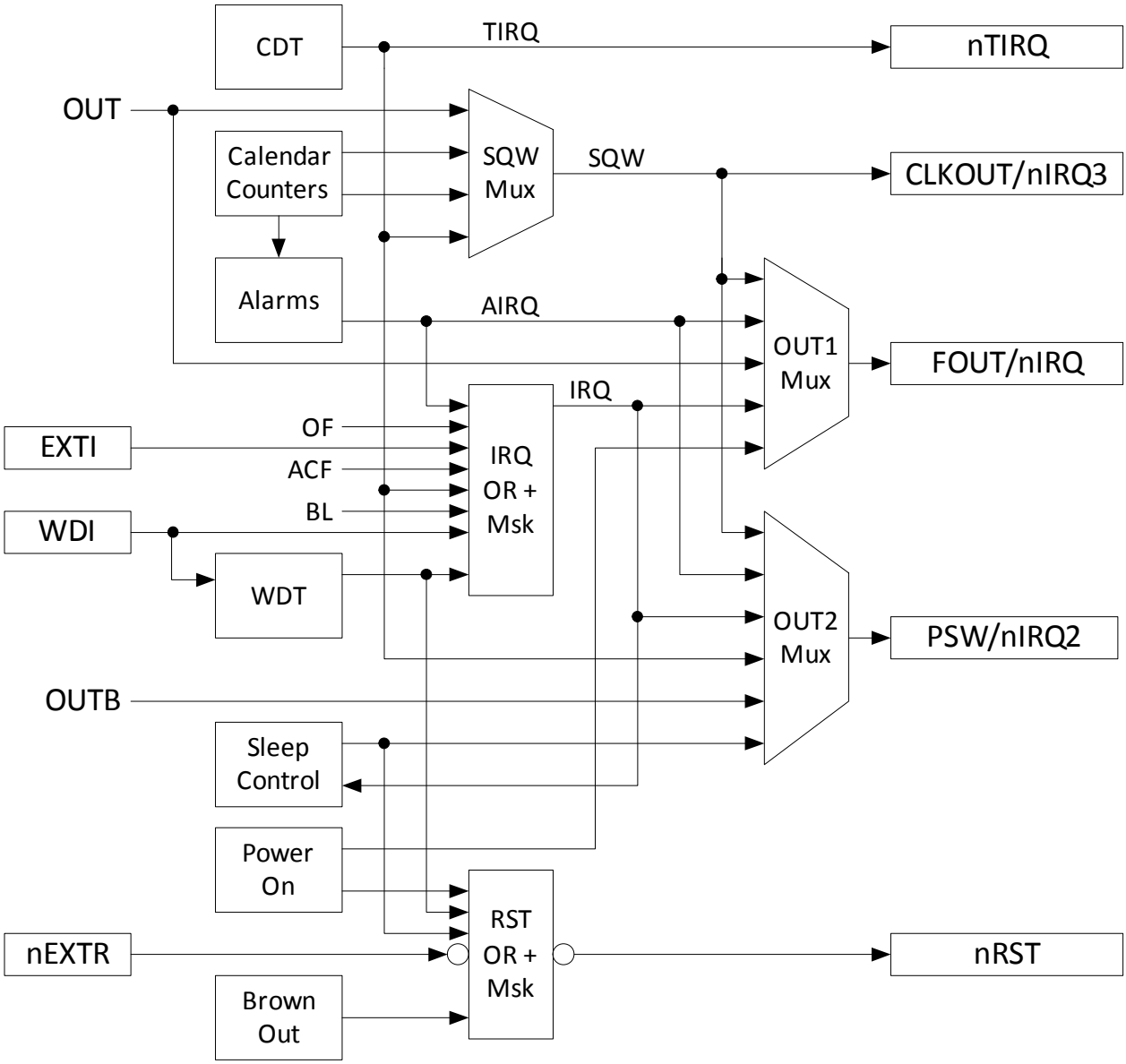


Figure 2 – AB18XX Digital Architecture Summary

3. Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings of the AB18XX are shown in Table 2.

Table 2 – Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	System Power Voltage		-0.3		3.6	V
V_{BAT}	Battery Voltage		-0.3		3.6	V
V_I	Input voltage	VCC Power state	-0.3		V_{CC}+ 0.3	V
V_I	Input voltage	VBAT Power state	-0.3		V_{BAT}+ 0.3	V
V_O	Output voltage	VCC Power state	-0.3		V_{CC}+ 0.3	V
V_O	Output voltage	VBAT Power state	-0.3		V_{BAT}+ 0.3	V
I_I	Input current		-10		10	mA
I_O	Output current		-20		20	mA
I_{OP}	PSW Output current				50	mA
V_{ESD}	ESD Voltage	CDM			±500	V
		HBM			±4000	V
I_{LU}	Latch-up Current				100	mA
T_{STG}	Storage Temperature		-65		150	℃
T_{OP}	Operating Temperature		-40		85	℃
T_{SLD}	Lead temperature	Hand soldering for 10 seconds			300	℃
T_{REF}	Reflow soldering temperature	Reflow profile per JEDEC J-STD-020D			260	℃

3.2 Power Supply Parameters

The power supply and switchover parameters of the AB18XX are shown in Table 3 and Figure 3. See Section 4.12 for a detailed description of the operations.

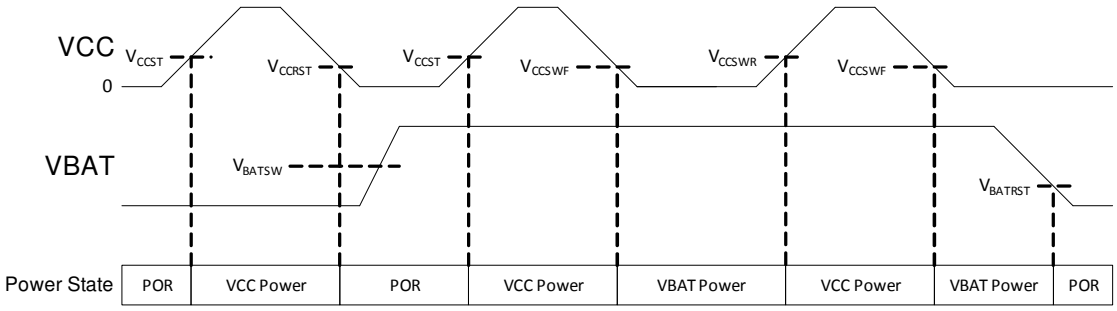


Figure 3 – Power Supply Switchover

Table 3 – Power Supply and Switchover Parameters

T_A = -40 ℃ to 85 ℃, TYP values at 25 ℃

SYMBOL	PARAMETER	PWR	TYPE	POWER STATE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	System Power Voltage	V_{CC}	Static	VCC Power	Clocks operating and RAM/registers retained	1.5		3.6	V
V_{CCIO}	V_{CC} I/O Interface Voltage	V_{CC}	Static	VCC Power	I2C or SPI operation	1.7		3.6	V
V_{CCST}	V_{CC} Start-up Voltage (1)	V_{CC}	Rising	POR -> VCC Power		1.6			V
V_{CCRST}	V_{CC} Reset Voltage	V_{CC}	Falling	VCC Power -> POR	$V_{BAT} < V_{BAT,MIN}$ or no V_{BAT}		1.3		V
V_{CCSWR}	V_{CC} Rising Switch-over Threshold Voltage	V_{CC}	Rising	VBAT Power -> VCC Power	$V_{BAT} \geq V_{BATRST}$		1.4		V
V_{CCSWF}	V_{CC} Falling Switch-over Threshold Voltage	V_{CC}	Falling	VCC Power -> VBAT Power	$V_{BAT} \geq V_{BATSW,MIN}$		1.3		V
V_{CCSWH}	V_{CC} Switchover Threshold Hysteresis (2)	V_{CC}	Hyst.	VCC Power <-> VBAT Power			120		mV
V_{CCRS}	V_{CC} Rising Slew Rate (5)	V_{CC}	Rising	VCC Power	Initial power-up from $V_{CCRST,MIN}$ to $V_{CCST,MIN}$.	TBD	2		V/s
V_{CCFS}	V_{CC} Falling Slew Rate (4)	V_{CC}	Falling	VCC Power -> VBAT Power	$V_{CC} < V_{VCCSW,MAX}$		0.5	TBD	V/ms
V_{BAT}	Battery Voltage	V_{BAT}	Static	VBAT Power		1.2		3.6	V
V_{BATSW}	Battery Switchover Voltage Range (6)	V_{BAT}	Static	VCC Power -> VBAT Power		1.6		3.6	V
V_{BATRST}	Falling Battery POR Voltage	V_{BAT}	Falling	VBAT Power -> POR	$V_{CC} < V_{VCCSWF}$		1.15		V
V_{BMRG}	V_{BAT} Margin above V_{CC} (3)	V_{BAT}	Static	VBAT Power		200			mV

(1) – V_{CC} must be above V_{CCST} to exit the POR state, independent of the V_{BAT} voltage.
(2) – Difference between V_{CCSWR} and V_{CCSWF}.
(3) – V_{BAT} must be higher than V_{CC} by at least this voltage to insure the AB18XX remains in the VBAT Power state.
(4) – Maximum V_{CC} falling slew rate to guarantee correct switchover to VBAT Power state.
(5) – Minimum V_{CC} rising slew rate to guarantee correct transition from POR to VCC Power state at initial power on.
(6) – V_{BAT} voltage to guarantee correct transition to VBAT Power state when V_{CC} falls.

3.3 Operating Parameters

The operating parameters of the AB18XX are shown in Table 4.

Table 4 – Operating Parameters

T_A = -40 ℃ to 85 ℃, TYP values at 25 ℃

SYMBOL	PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going Input Threshold Voltage		3.0V		1.5		V
			1.8V		1.1		
V_{T-}	Negative-going Input Threshold Voltage		3.0V		0.9		V
			1.8V		0.6		
I_{ILEAK}	Input leakage current		3.0V		20		pA
C_I	Input capacitance				3		pF
V_{OH}	High level output voltage on push-pull outputs		1.7V-3.6V	0.8•V_{CC}			V
V_{OL}	Low level output voltage		1.7V-3.6V			0.2•V_{CC}	V
I_{OH}	High level output current on push-pull outputs	V_{OH} = 0.8•V_{CC}	1.7V		3.8		mA
			1.8V		4.3		
			3.0V		11		
			3.6V		15		
I_{OL}	Low level output current	V_{OL} = 0.2•V_{CC}	1.7V		5.9		mA
			1.8V		6.9		
			3.0V		19		
			3.6V		20		
R_{DSON}	PSW output resistance to VSS	PSW Enabled	1.7V		1.6		Ω
			1.8V		1.5		
			3.0V		1.05		
			3.6V		1		
I_{OLEAK}	Output leakage current				20		pA

3.4 Oscillator Parameters

The oscillator parameters of the AB18XX are shown in Table 5.

Table 5 – Oscillator Parameters

T_A = -40 ℃ to 85 ℃, V_{CC} = 1.7 to 3.6V, TYP values at 25 ℃ and 3.0V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{XT}	XI and XO pin Crystal Frequency			32.768		kHz
F_{OF}	XT Oscillator failure detection frequency			8		kHz
C_{INX}	Internal XI and XO pin capacitance			1		pF
C_{EX}	External XI and XO pin PCB capacitance			<1	2	pF
OA_{XT}	XT Oscillation Allowance	At 25℃ using a 32.768kHz crystal		320		kΩ
F_{RCC}	Calibrated RC Oscillator Frequency	Factory Calibration	116	128	140	Hz
F_{RCU}	Uncalibrated RC Oscillator Frequency	Calibration Disabled (OFFSETR = 0)	110	122	134	Hz
J_{RCCC}	RC Oscillator cycle-cycle jitter	Calibration Disabled (OFFSETR = 0) – 128 Hz		2000		ppm
		Calibration Disabled (OFFSETR = 0) – 1 Hz		500		

3.5 V_{CC} Supply Current

The current supplied into the VCC power input under various conditions is shown in Table 6.

Table 6 – V_{CC} Supply Current

T_A = -40 °C to 85 °C, V_{BAT} = 0 V to 3.6 V, TYP values at 25 °C, VCC Power state

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC:I2C}$	V_{CC} supply current during I^2C burst read/write	400kHz bus speed, 10k pull-up resistors on SCL/SDA. (1)	3.6V		30		µA
			3.0V		20		
			2.4V		13		
			1.8V		10		
$I_{VCC:SPI}$	V_{CC} supply current during SPI burst read/write	2 MHz bus speed (2)	3.6V		15		µA
			3.0V		10		
			2.4V		7		
			1.8V		5		
$I_{VCC:XT}$	V_{CC} supply current in XT oscillator mode.	Time keeping mode with XT oscillator running. (3)	3.6V		59		nA
			3.0V		50		
			2.4V		48		
			1.8V		47		
			1.5V		46		
$I_{VCC:RC}$	V_{CC} supply current in RC oscillator mode.	Time keeping mode with only the RC oscillator running (XT oscillator is off). (3)	3.6V		23		nA
			3.0V		14		
			2.4V		12		
			1.8V		11		
			1.5V		11		
$I_{VCC:ACAL}$	V_{CC} supply current in autocalibrated RC oscillator mode.	Time keeping mode with only RC oscillator running and autocalibration enabled. ACP = 512 seconds. (3)	3.6V		27		nA
			3.0V		18		
			2.4V		16		
			1.8V		15		
			1.5V		14		
$I_{VCC:CK32}$	Additional V_{CC} supply current with CLKOUT at 32 kHz.	Time keeping mode with XT oscillator running, 32 kHz square wave on CLKOUT. (4)	3.6V		4.4		µA
			3.0V		3.6		
			2.4V		2.9		
			1.8V		2.2		
			1.5V		2.1		
$I_{VCC:CK128}$	Additional V_{CC} supply current with CLKOUT at 128 Hz.	All time keeping modes, 128 Hz square wave on CLKOUT. (4)	3.6V		11		nA
			3.0V		7		
			2.4V		5		
			1.8V		2.5		
			1.5V		2.3		

(1) Excluding external peripherals and pull-up resistor current. All other inputs (besides SDA and SCL) are at 0V or V_{CC}. AB080X and AB181X only.

(2) Excluding external peripheral current. All other inputs (besides SDI, nCE and SCL) are at 0V or V_{CC}. AB081X and AB181X only.
(3) All inputs and outputs are at 0V or V_{CC}.
(4) All inputs and outputs except CLKOUT are at 0V or V_{CC}.

3.6 V_{BAT} Supply Current

The current supplied into the VBAT power input under various conditions is shown in Table 7.

Table 7 – V_{BAT} Supply Current

$T_{A=}$ -40 ℃ to 85 ℃, TYP values at 25 ℃, VBAT Power state

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	V_{BAT}	MIN	TYP	MAX	UNIT
$I_{VBAT:XT}$	V_{BAT} supply current in XT oscillator mode.	Time keeping mode with XT oscillator running. (1)	< V_{CCSWF}	3.6V		59		nA
				3.0V		50		
				2.4V		48		
				1.8V		47		
				1.5V		46		
$I_{VBAT:RC}$	V_{BAT} supply current in RC oscillator mode.	Time keeping mode with only the RC oscillator running (XT oscillator is off). (1)	< V_{CCSWF}	3.6V		23		nA
				3.0V		14		
				2.4V		12		
				1.8V		11		
				1.5V		11		
$I_{VBAT:ACAL}$	V_{BAT} supply current in autocalibrated RC oscillator mode.	Time keeping mode with the RC oscillator running and autocalibration enabled. ACP = 512 seconds. (1)	< V_{CCSWF}	3.6V		27		nA
				3.0V		18		
				2.4V		16		
				1.8V		15		
				1.5V		14		
$I_{VBAT:VCC}$	V_{BAT} supply current in V_{CC} powered mode.	V_{CC} powered mode. (1)	1.7-3.6 V	3.6V		540		pA
				3.0V		290		
				2.4V		230		
				1.8V		190		
				1.2V		160		

(1) All inputs and outputs are at 0V or V_{CC}.

3.7 I²C AC Electrical Characteristics

The I²C AC characteristic parameters are taken from Figure 4 and shown in Table 8.

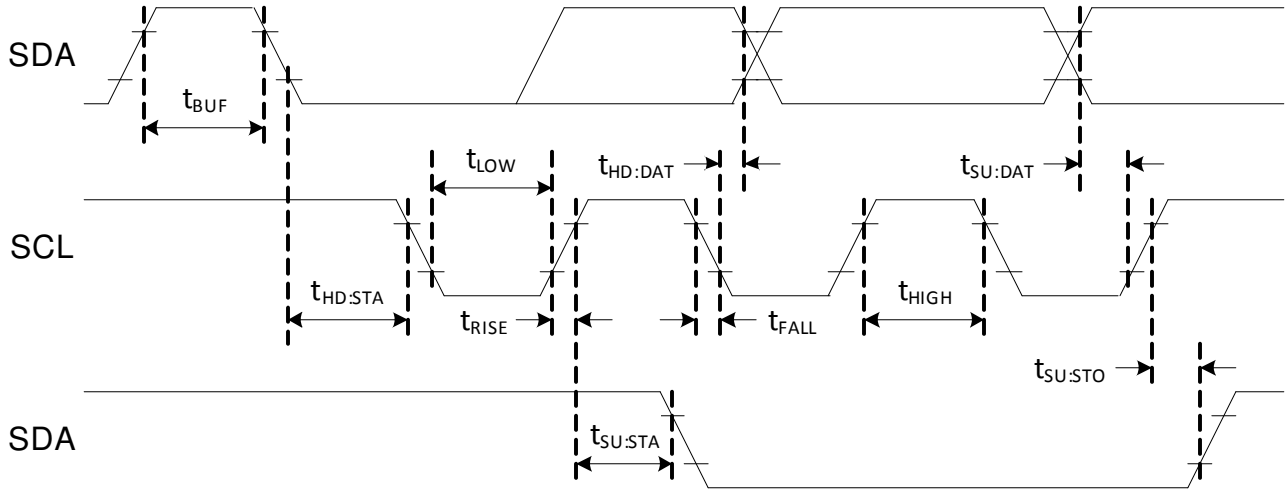


Figure 4 – I²C AC Parameter Definitions

Table 8 – I²C AC Electrical Parameters

T_A = -40 ℃ to 85 ℃, TYP values at 25 ℃

SYMBOL	PARAMETER	V_{CC}	MIN	TYP	MAX	UNIT
f_{SCL}	SCL input clock frequency	1.7V-3.6V	0		400	kHz
t_{LOW}	Low period of SCL clock	1.7V-3.6V	1.3			µs
t_{HIGH}	High period of SCL clock	1.7V-3.6V	600			ns
t_{RISE}	Rise time of SDA and SCL	1.7V-3.6V			300	ns
t_{FALL}	Fall time of SDA and SCL	1.7V-3.6V			300	ns
$t_{HD:STA}$	START condition hold time	1.7V-3.6V	600			ns
$t_{SU:STA}$	START condition setup time	1.7V-3.6V	600			ns
$t_{SU:DAT}$	SDA setup time	1.7V-3.6V	100			ns
$t_{HD:DAT}$	SDA hold time	1.7V-3.6V	0			ns
$t_{SU:STO}$	STOP condition setup time	1.7V-3.6V	600			ns
t_{BUF}	Bus free time before a new transmission	1.7V-3.6V	1.3			µs

3.8 SPI AC Electrical Characteristics

The I^2C AC characteristic parameters are taken from Figure 5 and Figure 6 and shown in Table 9.

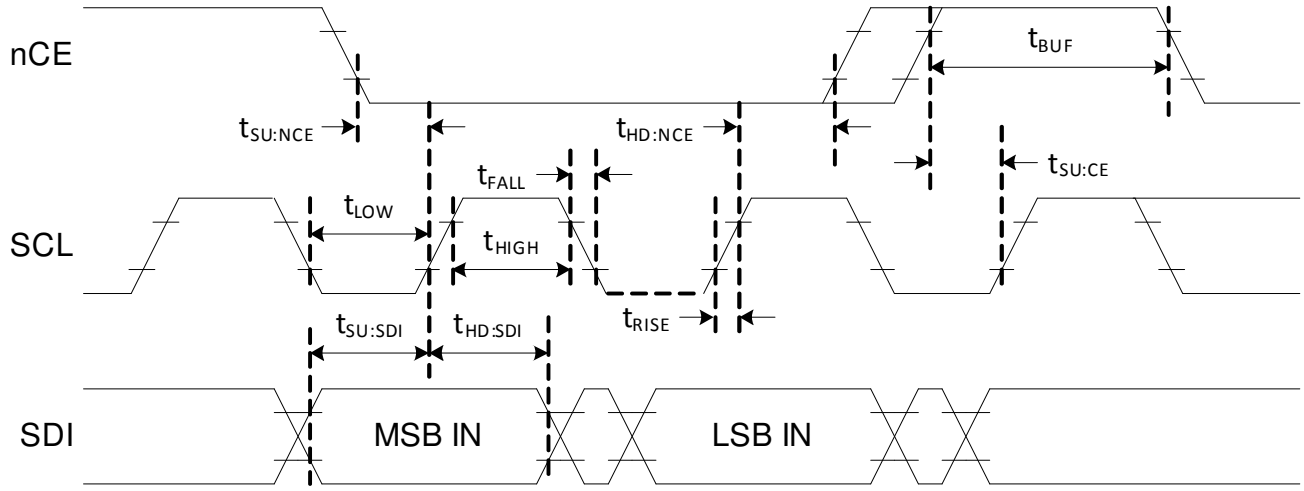


Figure 5 – SPI AC Parameter Definitions – Input

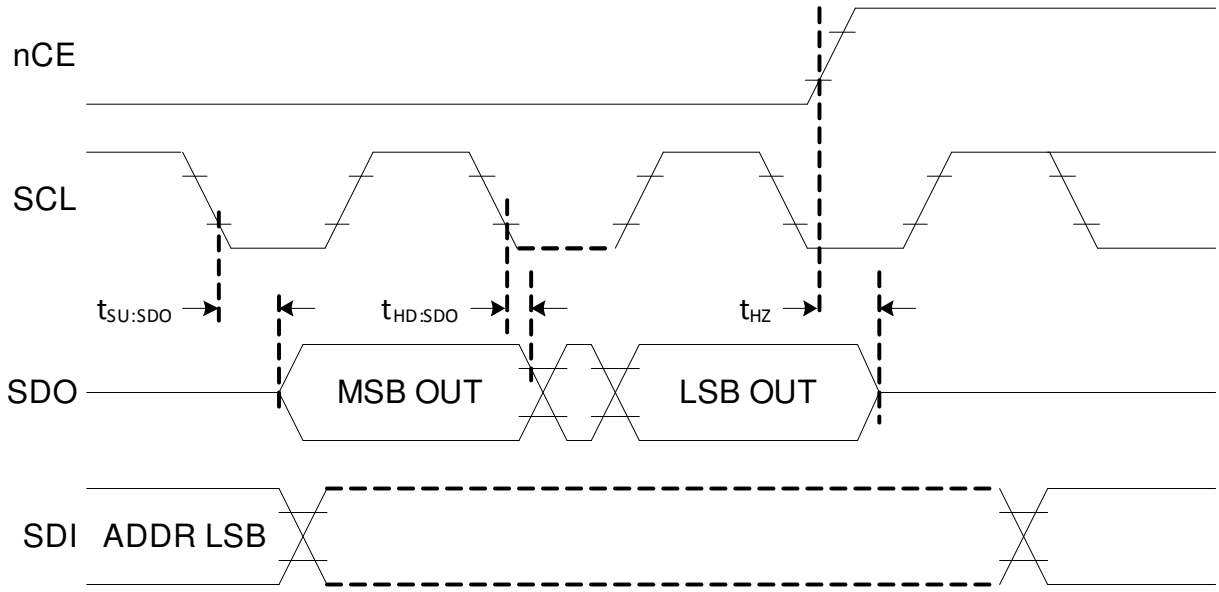


Figure 6 – SPI AC Parameter Definitions – Output

Table 9 – SPI AC Electrical Parameters

T_A = -40 ℃ to 85 ℃, TYP values at 25 ℃

SYMBOL	PARAMETER	V_{CC}	MIN	TYP	MAX	UNIT
f_{SCL}	SCL input clock frequency	1.7V-3.6V	0		2	MHz
t_{LOW}	Low period of SCL clock	1.7V-3.6V	200			ns
t_{HIGH}	High period of SCL clock	1.7V-3.6V	200			ns
t_{RISE}	Rise time of all signals	1.7V-3.6V			1	µs
t_{FALL}	Fall time of all signals	1.7V-3.6V			1	µs
$t_{SU:NCE}$	nCE low setup time to SCL	1.7V-3.6V	200			ns
$t_{HD:NCE}$	nCE hold time to SCL	1.7V-3.6V	200			ns
$t_{SU:CE}$	nCE high setup time to SCL	1.7V-3.6V	200			ns
$t_{SU:SDI}$	SDI setup time	1.7V-3.6V	40			ns
$t_{HD:SDI}$	SDI hold time	1.7V-3.6V	50			ns
$t_{SU:SDO}$	SDO output delay from SCL	1.7V-3.6V			150	ns
$t_{HD:SDO}$	SDO output hold from SCL	1.7V-3.6V	0			ns
t_{HZ}	SDO output Hi-Z from nCE	1.7V-3.6V			250	ns
t_{BUF}	nCE high time before a new transmission	1.7V-3.6V	200			ns

3.9 Power On AC Electrical Characteristics

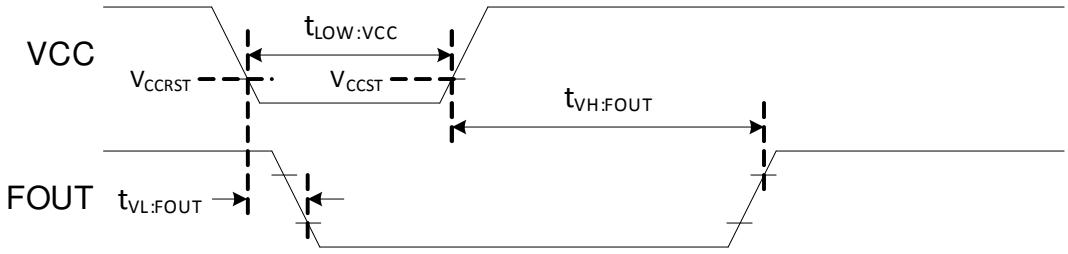


Figure 7 – Power On AC Parameter Definitions

Table 10 – Power On AC Electrical Parameters

T_A = -40 ℃ to 85 ℃, TYP values at 25 ℃, VBAT < 1.2 V

SYMBOL	PARAMETER	V_{CC}	MIN	TYP	MAX	UNIT
$t_{LOW:VCC}$	Low period of VCC to insure a valid POR	1.7V-3.6V		1		s
$t_{VL:FOUT}$	VCC low to FOUT low	1.7V-3.6V		1		ms
$t_{VH:FOUT}$	VCC high to FOUT high	1.7V-3.6V		300		ms
t_{BREF}	BREF/BPOL change to BBOD valid	1.7V-3.6V		1000		ms

3.10 nRST AC Electrical Characteristics

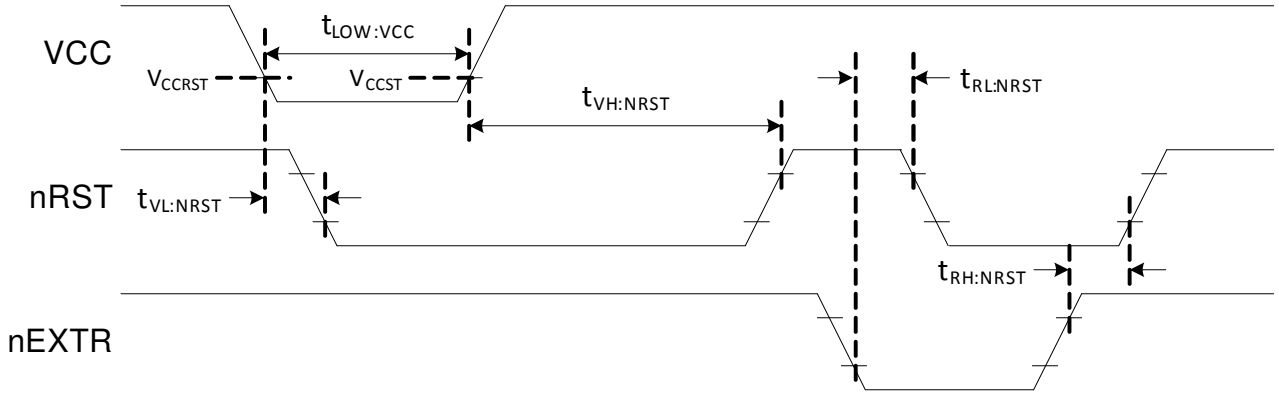


Figure 8 – nRST AC Parameter Definitions

Table 11 – nRST AC Electrical Parameters

T_A = -40 ℃ to 85 ℃, TYP values at 25 ℃, VBAT < 1.2 V

SYMBOL	PARAMETER	V_{CC}	MIN	TYP	MAX	UNIT
$t_{LOW:VCC}$	Low period of VCC to insure a valid POR	1.7V-3.6V		1		s
$t_{VL:NRST}$	VCC low to nRST low	1.7V-3.6V		1		ms
$t_{VH:NRST}$	VCC high to nRST high	1.7V-3.6V		700		ms
$T_{RL:NRST}$	nEXTR low to nRST low	1.7V-3.6V		50		ns
$T_{RH:NRST}$	nEXTR high to nRST high	1.7V-3.6V		50		ns

4. AB18XX Functional Description

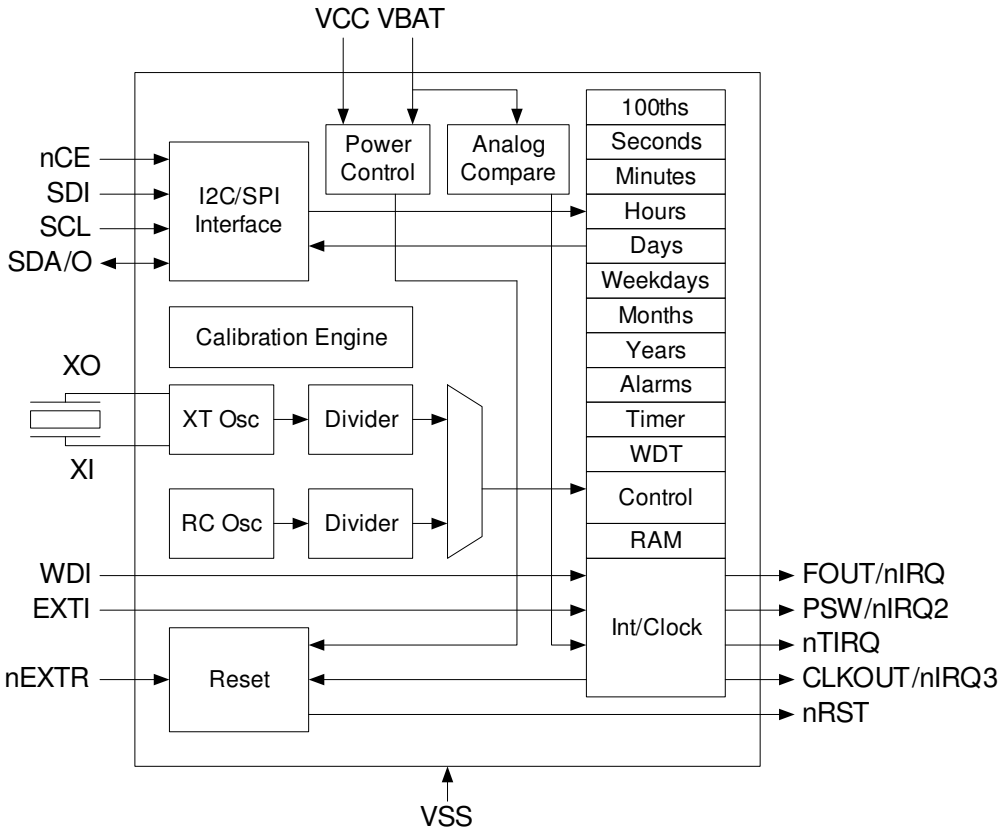


Figure 9 – AB18XX Detailed Block Diagram

The AB18XX serves as a companion part for host processors including microcontrollers, radios, and digital signal processors. It tracks time as in a typical RTC product and additionally provides unique power management functionality that makes it ideal for highly energy-constrained applications. To support such operation, the AB18XX includes 3 distinct feature groups: 1) baseline timekeeping features, 2) advanced timekeeping features, and 3) power management features. Functions from each feature group may be controlled via I/O offset mapped registers. These registers are accessed using either an I^2C serial interface (e.g., in the AB1805) or a SPI serial interface (e.g., in the AB1815). Each feature group is described briefly below and in greater detail in subsequent sections.

The baseline timekeeping feature group supports the standard 32 kHz crystal (XT) oscillation mode for maximum frequency accuracy with an ultra-low current draw of 50 nA. The baseline timekeeping feature group also includes a standard set of counters monitoring hundredths of a second up through centuries. A complement of countdown timers and alarms may additionally be set to initiate interrupts or resets on several of the outputs.

The advanced timekeeping feature group supports two additional oscillation modes: 1) RC oscillator mode, and 2) auto-calibration mode. At only 14 nA, the temperature-compensated ±10% RC oscillator mode provides an even lower current draw than the XT oscillator for applications with reduced frequency accuracy requirements. A proprietary calibration algorithm allows the AB18XX to digitally tune the RC oscillator frequency and the XT oscillator frequency with accuracy as low as 2 ppm at a given temperature. In auto-calibration mode, the RC oscillator is used as the primary oscillation source and is periodically calibrated against the XT oscillator. Calibration may be done automatically every 8.5 minutes or 17 minutes and may also be initiated via software. This mode enables average current draw of only 18 nA with frequency accuracy similar to the XT oscillator. The

advanced timekeeping feature group also includes a rich set of input and output configuration options that enables the monitoring of external interrupts (e.g., pushbutton signals), the generation of clock outputs, and watchdog timer functionality.

Power management features built into the AB18XX enable it to operate as a backup device in both line-powered and battery-powered systems. An integrated power control module automatically detects when main power (VCC) falls below a threshold and switches to backup power (VBAT). Up to 256B of ultra-low leakage RAM enable the storage of key parameters when operating on backup power.

The AB18XX is the first RTC to incorporate a number of more advanced power management features. In particular, the AB18XX includes a finite state machine (integrated with the Power Control block in Figure 9) that can control a host processor as it transitions between sleep/reset states and active states. Digital outputs can be configured to control the reset signal or interrupt input of the host controller. The AB18XX additionally integrates a power switch with <1 Ω impedance that can be used to cut off ground current on the host microcontroller and reduce sleep current to <1 nA. The AB18XX parts can wake up a sleeping system using internally generated timing interrupts or externally generated interrupts generated by digital inputs (e.g., using a pushbutton) or an analog comparator. The aforementioned functionality enables users to seamlessly power down host processors, leaving only the energy-efficient AB18XX chip awake. The AB18XX also includes voltage detection on the backup power supply.

Each functional block is explained in detail in the remainder of this section. Functional descriptions refer to the registers shown in Table 12 and Table 13. A detailed description of all registers can be found in Section 5.

Table 12 – Register Definitions (00 to 0F)

Offset	Register	7	6	5	4	3	2	1	0
00	Hundredths	Seconds - Tenths				Seconds - Hundredths			
01	Seconds	GP0	Seconds - Tens			Seconds - Ones			
02	Minutes	GP1	Minutes - Tens			Minutes - Ones			
03	Hours (24 hour)	GP3	GP2	Hours - Tens		Hours - Ones			
03	Hours (12 hour)	GP3	GP2	AM/ PM	Hours - Tens	Hours - Ones			
04	Date	GP5	GP4	Date - Tens		Date - Ones			
05	Months	GP8	GP7	GP6	Month - Tens	Month - Ones			
06	Years	Years - Tens				Years - Ones			
07	Weekdays	GP13	GP12	GP11	GP10	GP9	Weekdays		
08	Hundredths_Alarm	Hundredths_Alarm - Tenths				Hundredths_Alarm - Hundredths			
09	Second_Alarm	GP14	Second_Alarm - Tens			Second_Alarm - Ones			
0A	Minute_Alarm	GP15	Minute_Alarm - Tens			Minute_Alarm - Ones			
0B	Hour_Alarm (24 hour)	GP17	GP16	Hour_Alarm - Tens		Hour_Alarm - Ones			
0B	Hour Alarm (12 hour)	GP3	GP2	AM/ PM		Hours - Tens			
0C	Date_Alarm	GP19	GP18	Date_Alarm - Tens		Date_Alarm - Ones			
0D	Month_Alarm	GP22	GP21	GP20	Month_ Alarm - Tens	Month_Alarm - Ones			
0E	Weekday_Alarm	GP27	GP26	GP25	GP24	GP23	Weekday_Alarm		
0F	Status	CB	BAT	WDT	BL	TIM	ALM	EX2	EX1

Table 13 – Register Definitions (10 to FF)

Offset	Register	7	6	5	4	3	2	1	0
10	Control1	STOP	12/24	OUTB	OUT	RSP	ARST	PWR2	WRTC
11	Control2	OUTPP	-	RS1E	OUT2S			OUT1S	
12	IntMask	CEB	IM		BLIE	TIE	AIE	EX2E	EX1E
13	SQW	SQWE	-		SQFS				
14	Cal_XT	CMDX	OFFSETX						
15	Cal_RC_Hi	CMDR	OFFSETR[13:8]						
16	Cal_RC_Low	OFFSETR[7:0]							
17	Sleep_Control	SLP	SLRES	EX2P	EX1P	SLST	SLTO		
18	Timer Control	TE	TM	TRPT	RPT			TFS	
19	Timer	Countdown Timer							
1A	Timer_Initial	Timer Initial Value							
1B	WDT	WDS	BMB					WRB	
1C	Osc. Control	OSEL	ACAL		AOS	FOS	PWGT	OFIE	ACIE
1D	Osc. Status	XTCAL		LKO2	OMODE	XTF	-	OF	ACF
1E	RESERVED	RESERVED							
1F	Configuration Key	Configuration Key							
20	Trickle	TCS				DIODE	ROUT		
21	BREF Control	BREF				-			
22	RESERVED	RESERVED							
23	RESERVED	RESERVED							
24	RESERVED	RESERVED							
25	RESERVED	RESERVED							
26	RESERVED	RESERVED							
27	RESERVED	RESERVED							
28	ID0 (Read only)	Part Number – MS Byte = 00011000 (0x18)							
29	ID1 (Read only)	Part Number – LS Byte = 00000000 (0x00)							
2A	ID2 (Read only)	Revision – Major = 00010					Revision – Minor = 000		
2B	ID3 (Read only)	Mfg. Year				Mfg. Week[3:0]			
2C	ID4 (Read only)	Mfg. Wafer						Mfg. Week[5:4]	
2D	ID5 (Read only)	Mfg. Lot	Mfg. Quadrant						
2E	ID6 (Read only)	Mfg. Serialization						–	–
2F	ASTAT	BBOD	BMIN	-	-	-	-	VINIT	-
30	OCTRL	WDBM	EXBM	WDDS	EXDS	RSEN	O4EN	O3EN	O1EN
3F	Extension Address	O4BM	BPOL	WDIN	EXIN	XEN	XADA	XADS	
40–7F	RAM	Normal RAM Data							
80–FF	RAM	Alternate RAM Data (I^2C Mode Only)							

4.1 I²C Interface

The AB18XX includes a standard I²C interface. The device is accessed at addresses 0xD2/D3, and supports Fast Mode (up to 400 kHz). The I²C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor. By definition, a device that sends a message is called the "transmitter", and the device that accepts the message is called the "receiver". The device that controls the message transfer by driving SCL is called "master". The devices that are controlled by the master are called "slaves". The AB18XX is always a slave device.

I²C termination resistors should be above 2.2 kΩ, and for systems with short I²C busses and few connections these terminators can typically be as large as 22 kΩ (for 400 kHz operation) or 56 kΩ (for 100 kHz operation). Larger resistors will produce lower system current consumption.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

A number of bus conditions have been defined (see Figure 10) and are described in the following sections.

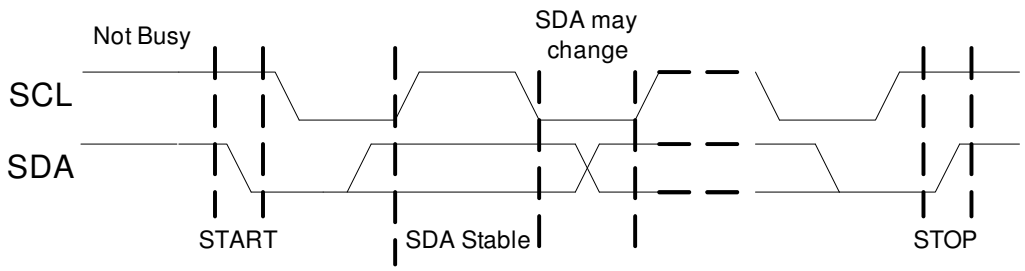


Figure 10 – Basic I²C Conditions

4.1.1 Bus Not Busy

Both SDA and SCL remain high.

4.1.2 Start Data Transfer

A change in the state of SDA from high to low, while SCL is high, defines the START condition. A START condition which occurs after a previous START but before a STOP is called a RESTART condition, and functions exactly like a normal STOP followed by a normal START.

4.1.3 Stop Data Transfer

A change in the state of SDA from low to high, while SCL is high, defines the STOP condition.

4.1.4 Data Valid

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

4.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge (ACK) bit as shown in Figure 11. This acknowledge bit is a low level driven onto SDA by the receiver, whereas the master generates an extra acknowledge related SCL pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, on a read transfer a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related SCL pulse. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge (a NAK) on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

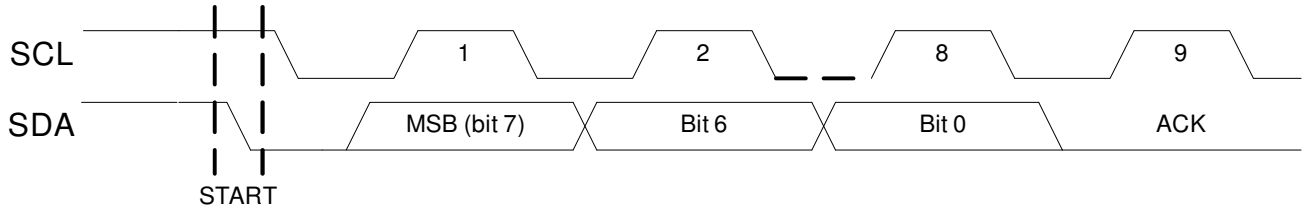


Figure 11 – I²C Acknowledge

4.1.6 Address Operation

Figure 12 shows the operation with which the master addresses the AB18XX. After the START condition, a 7-bit address is transmitted MSB first. If this address is 0b1101001x (0xD2/3), the AB18XX is selected, the eighth bit indicate a write (RW = 0) or a read (RW = 1) operation and the AB18XX supplies the ACK. The AB18XX ignores all other address values and does not respond with an ACK.

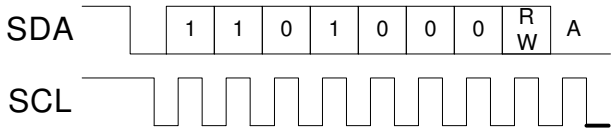


Figure 12 – I²C Address Operation

4.1.7 Offset Address Transmission

If the RW bit of the Address Operation indicates a write, the next byte transmitted from the master is the Offset Address as shown in Figure 13. This value is loaded into the Address Pointer of the AB18XX.

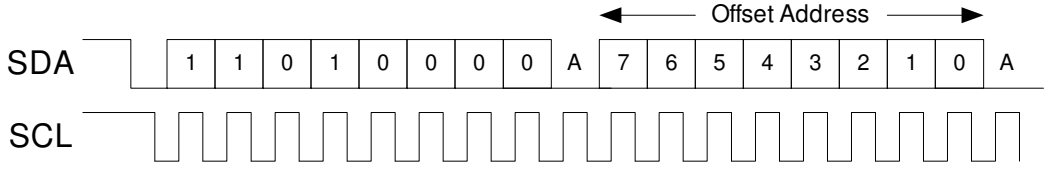


Figure 13 – I²C Offset Address Transmission

4.1.8 Write Operation

In a write operation the master transmitter transmits to the AB18XX slave receiver. The Address Operation has a RW value of 0, and the second byte contains the Offset Address as in Figure 13. The next byte is written to the register selected by the Address Pointer (which was loaded with the Offset Address) and the Address Pointer is incremented. Subsequent transfers write bytes into successive registers until a STOP condition is received, as shown in Figure 14.

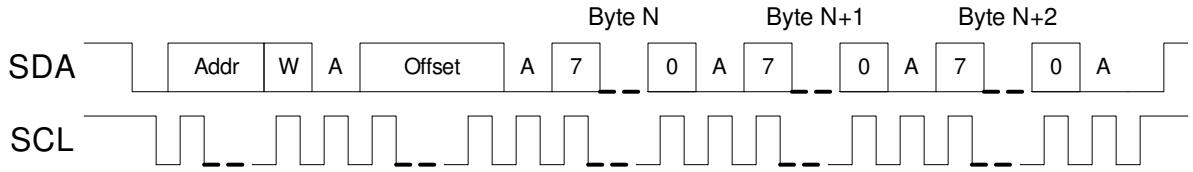


Figure 14 – I²C Write Operation

4.1.9 Read Operation

In a read operation, the master first executes an Offset Address Transmission to load the Address Pointer with the desired Offset Address. A subsequent operation will again issue the address of the AB18XX but with th RW bit as a 1 indicating a read operation. Figure 15 shows this transaction beginning with a RESTART condition, although a STOP followed by a START may also be used. After the address operation, the slave becomes the transmitter and sends the register value from the location pointed to by the Address Pointer, and the Address Pointer is incremented. Subsequent transactions produce successive register values, until the master receiver responds with a NAK and a STOP to complete the operation. Because the Address Pointer holds a valid register address, the master may initiate another read sequence at this point without performing another Offset Address operation.

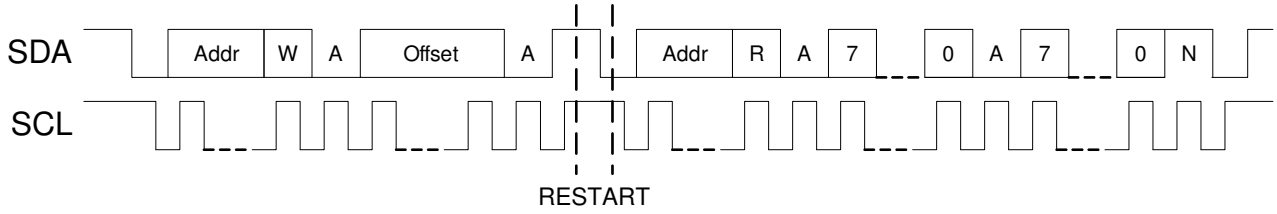


Figure 15 – I²C Read Operation

4.2 SPI Interface

The AB18XX includes a standard 4-wire SPI interface. The serial peripheral interface (SPI) bus is intended for synchronous communication between different ICs. It typically consists of four signal lines: serial data input (SDI), serial data output (SDO), serial clock (SCL) and an active low chip enable (nCE). The AB18XX may be connected to a master with a 3-wire SPI interface by tying SDI and SDO together. By definition, a device that sends a message is called the "transmitter", and the device that accepts the message is called the "receiver". The device that controls the message transfer by driving SCL is called "master". The devices that are controlled by the master are called "slaves". The AB18XX is always a slave device.

The nCE input is used to initiate and terminate a data transfer. The SCL input is used to synchronize data transfer between the master and the slave devices via the SDI (master to slave) and SDO (slave to master) lines. The SCL input, which is generated by the master, is active only during address and data transfer to any device on the SPI bus (see Figure 5 on page 9).

The AB18XX supports clock frequencies up to 2 MHz, and responds to either (CPOL = 0, CPAH = 0 or CPOL = 1, CPAH = 1). For these two modes, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL. There is one clock for each bit transferred. Address and data bits are transferred in groups of eight bits.

4.2.1 Write Operation

Figure 16 shows a SPI write operation. The operation is initiated when the nCE signal to the AB18XX goes low. At that point an 8-bit Address byte is transmitted from the master on the SDI line, with the upper RW bit indicating read (if 0) or write (if 1). In this example the RW bit is a one selecting a write operation, and the lower 7 bits of the Address byte contain the Offset Address, which is loaded into the Address Pointer of the AB18XX.

Each subsequent byte is loaded into the register selected by the Address Pointer, and the Address Pointer is incremented. Because the address is only 7 bits long, only the lower 128 registers of the AB18XX may be accessed via the SPI interface. The operation is terminated by the master by bringing the nCE signal high. Note that the SDO line is not used in a write operation and is held in the high impedance state by the AB18XX.

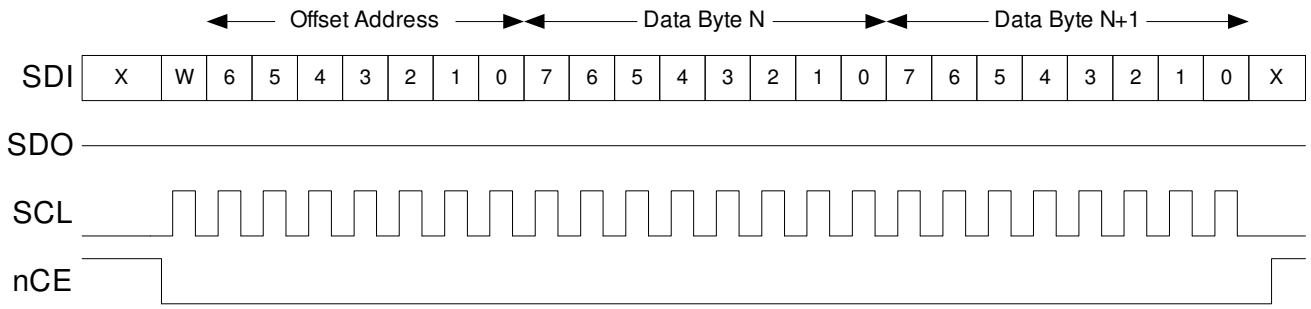


Figure 16 – SPI Write Operation

4.2.2 Read Operation

Figure 17 shows a read operation. The address is transferred from the master to the slave just as it is in a write operation, but in this case the RW bit is a 0 indicating a read. After the transfer of the last address bit (bit 0), the AB18XX begins driving data from the register selected by the Address Pointer onto the SDO line, bit 7 first, and the Address Pointer is incremented. The transfer continues until the master brings the nCE line high.

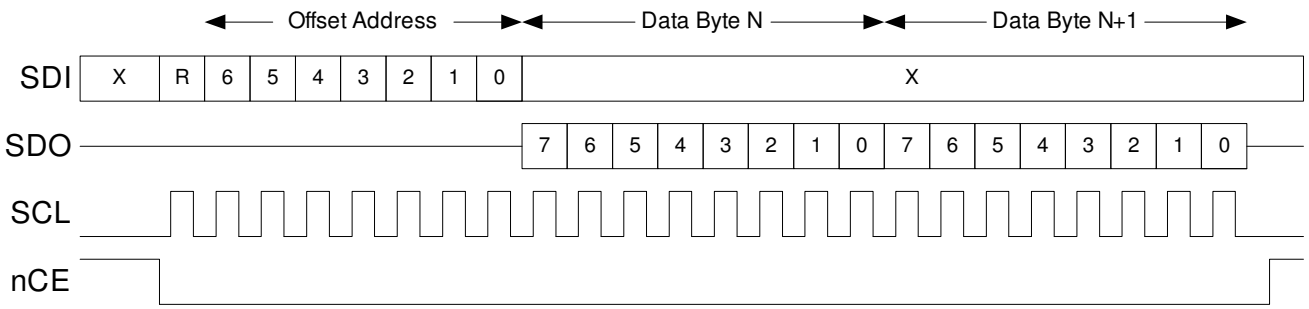


Figure 17 – SPI Read Operation

4.3 XT Oscillator

The AB18XX includes a very power efficient crystal (XT) oscillator which runs at 32 kHz. This oscillator is selected by setting the OSEL bit to 0 and includes a low jitter calibration function.

4.4 RC Oscillator

The AB18XX includes an extremely low power RC oscillator which runs at 128 Hz. This oscillator is selected by setting the OSEL bit to 1. Switching between the XT and RC Oscillators is guaranteed to produce less than one second of error in the Calendar Counters. The AB18XX may be configured to automatically switch to the RC Oscillator when VCC drops below its threshold by setting the AOS bit, and/or be configured to automatically switch if an XT Oscillator failure is detected by setting the FOS bit.

4.5 RTC Counter Access

When reading any of the counters in the RTC using a burst operation, the 1 Hz and 100 Hz clocks are held off during the access. This guarantees that a single burst will either read or write a consistent timer value (other than the Hundredths Counter – see Section 4.5.1). There is a watchdog function to insure that a very long pause on the interface does not cause the RTC to lose a clock.

On a write to any of the Calendar Counters, the entire timing chain up to 100 Hz (if the XT Oscillator is selected) or up to 1Hz (if the RC Oscillator is selected) is reset to 0. This guarantees that the Counters will begin counting immediately after the write is complete, and that in the XT oscillator case the next 100 Hz clock will occur exactly 10 ms later. In the RC Oscillator case, the next 1 Hz clock will occur exactly 1 second later. This allows a burst write to configure all of the Counters and initiate a precise time start. Note that a Counter write may cause one cycle of a Square Wave output to be of an incorrect period.

The WRTC bit must be set in order to write to any of the Counter registers. This bit can be cleared to prevent inadvertent software access to the Counters.

4.5.1 Hundredths Synchronization

If the Hundredths Counter is read as part of the counter burst, there is a small probability (approximately 1 in 10^9) that the Hundredths Counter rollover from 99 to 00 and the Seconds Counter increment will be separated by the read. In this case, correct read information can be guaranteed by the following algorithm.

1) Read the Counters, either in a burst. If the Hundredths Counter is neither 00 nor 99, the read is correct.
2) If the Hundredths Counter was 00, perform the read again. The resulting value from this second read is guaranteed to be correct.
3) If the Hundredths Counter was 99, perform the read again.
    a. If the Hundredths Counter is still 99, the results of the first read are guaranteed to be correct. Note that it is possible that the second read is not correct.
    b. If the Hundredths Counter has rolled over to 00, and the Seconds Counter value from the second read is equal to the Seconds Counter value from the first read plus 1, both reads produced correct values. Alternatively, perform the read again. The resulting value from this third read is guaranteed to be correct.
    c. If the Hundredths Counter has rolled over to 00, and the Seconds Counter value from the second read is equal to the Seconds Counter value from the first read, perform the read again. The resulting value from this third read is guaranteed to be correct.

4.6 Generating Hundredths of a Second

The generation of an exact 100 Hz signal for the Hundredths Counter requires a special logic circuit. The 2 kHz clock signal is divided by 21 for 12 iterations, and is alternately divided by 20 for 13 iterations. This produces an effective division of:

$$(21 * 12 + 20 * 13)/25 = 20.48$$

producing an exact long-term average 100 Hz output, with a maximum jitter of less than 1 ms. The Hundredths Counter is not available when the 128 Hz RC Oscillator is selected.

4.7 Watchdog Timer

The AB18XX includes a Watchdog Timer (WDT), which can be configured to generate an interrupt or a reset if it times out. The WDT is controlled by the Watchdog Timer Register (see Section 5.6.4). The RB field selects the frequency at which the timer is decremented, and the BMB field determines the value loaded into the timer when it is restarted. If the timer reaches a value of zero, the WDS bit determines whether an interrupt is generated in nIRQ (if WDS is 0) or the nRST output pin is asserted (if WDS is 1). The timer reaching zero sets the WDT flag in the Status Register, which may be cleared by setting the WDT flag to zero. If reset is selected, the nRST output pin is asserted within 1/16 second of the timer reaching zero and remains asserted for 1/16 second.

Two actions will restart the WDT timer:

1) Writing the Watchdog Timer Register with a new watchdog value.
2) A change in the level of the WDI pin.

If the Watchdog Timer generates an interrupt or reset, the Watchdog Timer Register must be written in order to restart the Watchdog Timer function. If the BMB field is 0, the Watchdog Timer function is disabled.

The BMB field describes the maximum timeout delay. For example, if RB = 01 so that the clock period is 250 ms, a BMB value of 9 implies that the timeout will occur between 2000 ms and 2250 ms after writing the Watchdog Timer Register.

4.8 Digital Calibration

4.8.1 XT Oscillator Digital Calibration

In order to improve the accuracy of the XT oscillator, a Distributed Digital Calibration function is included (see section 5.4.1). This function uses a calibration value, OFFSETX, to adjust the clock period over a 16 second or 32 second calibration period. When the 32 kHz XT oscillator is selected, the clock at the 16 kHz level of the divider chain is modified on a selectable interval. Clock pulses are either added or subtracted to ensure accuracy of the counters. If the CMDX bit is a 0 (normal calibration), OFFSETX cycles of the 16 kHz clock are gated (negative calibration) or replaced by 32 kHz pulses (positive calibration) within every 32 second calibration period. In this mode, each step in OFFSETX modifies the clock frequency by 1.907 ppm, with a maximum adjustment of ~+120/-122 ppm. If the CMDX bit is 1 (coarse calibration), OFFSETX cycles of the 16 kHz clock are gated or replaced by the 32 kHz clock within every 16 second calibration period. In this mode, each step in OFFSETX modifies the clock frequency by 3.814 ppm, with a maximum adjustment of ~+240/-244 ppm. OFFSETX contains a two's complement value, so the possible steps are from -64 to +63. Note that unlike other implementations, Distributed Digital Calibration guarantees that the clock is precisely calibrated every 32 seconds with normal calibration and every 16 seconds when coarse calibration is selected.

In addition to the normal calibration, the AB18XX also includes an Extended Calibration field to compensate for low capacitance environments. The frequency generated by the Crystal Oscillator may be slowed by 122 ppm times the value in the XTCAL (see Section 0) field (0, -122,-244 or -366 ppm). The clock is still precisely calibrated in 16 or 32 seconds.

The pulses which are added to or subtracted from the 16 kHz clock are spread evenly over each 16 or 32 second period using the ABRACON patented Distributed Calibration algorithm. This insures that in XT mode the maximum cycle-to-cycle jitter in any clock of a frequency 16 kHz or lower caused by calibration will be no more than one 16 kHz period. This maximum jitter applies to all clocks in the AB18XX, including the Calendar Counter, Countdown Timer and Watchdog Timer clocks and any clock driven onto the CLKFOUT/nIRQ pin.

4.8.1.1 XT Calibration Process

The XT oscillator calibration value is determined by the following process:

1) Set the OFFSETX, CMDX and XTCAL register fields to 0 to insure calibration is not occurring.
2) Select the XT oscillator by setting the OSEL bit to 0.
3) Configure a square wave output on one of the output pins of frequency Fnom (for example, 16 Hz).
4) Measure the frequency Fmeas at the output pin.
5) Compute the adjustment value required in ppm as ((Fnom – Fmeas)*1000000)/Fmeas = PAdj
6) Compute the adjustment value in steps as PAdj/(1000000/2^19) = PAdj/(1.90735) = Adj
7) If Adj < -320, the XT frequency is too high to be calibrated
8) Else if Adj < -256, set XTCAL = 3, CMDX = 1, OFFSETX = (Adj +192)/2
9) Else if Adj < -192, set XTCAL = 3, CMDX = 0, OFFSETX = Adj +192
10) Else if Adj < -128, set XTCAL = 2, CMDX = 0, OFFSETX = Adj +128
11) Else if Adj < -64, set XTCAL = 1, CMDX = 0, OFFSETX = Adj + 64
12) Else if Adj < 64, set XTCAL = 0, CMDX = 0, OFFSETX = Adj
13) Else if Adj < 128, set XTCAL = 0, CMDX = 1, OFFSETX = Adj/2
14) Else the XT frequency is too low to be calibrated

4.8.2 RC Oscillator Digital Calibration

The RC Oscillator has a patented Distributed Digital Calibration function similar to that of the XT Oscillator (see sections 5.4.2 and 5.4.3). However, because the RC Oscillator has a greater fundamental variability, the range of calibration is much larger, with four calibration ranges selected by the CMDR field. When the 128 Hz RC oscillator is selected, the clock at the 64 Hz level of the divider chain is modified on a selectable interval using the calibration value OFFSETR. Clock pulses are either added or subtracted to ensure accuracy of the counters. If the CMDR field is 00, OFFSETR cycles of the 64 Hz clock are gated (negative calibration) or replaced by 128 Hz pulses (positive calibration) within every 8,192 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 1.907 ppm, with a maximum adjustment of +15,623/-15,625 ppm (+/- 1.56%). If the CMDR field is 01, OFFSETR cycles of the 64 Hz clock are gated or replaced by the 128 Hz clock within every 4,096 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 3.82 ppm, with a maximum adjustment of +31,246/-31,250 ppm (+/-3.12%). If the CMDR field is 10, OFFSETR cycles of the 64 Hz clock are gated (negative calibration) or replaced by 128 Hz pulses (positive calibration) within every 2,048 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 7.64 ppm, with a maximum adjustment of +62,492/-62,500 ppm (+/- 6.25%). If the CMDR field is 01, OFFSETR cycles of the 64 Hz clock are gated or replaced by the 128 Hz clock within every 1,024 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 15.28 ppm, with a maximum adjustment of +124,984/-125,000 ppm (+/-12.5%). OFFSETR contains a two's complement value, so the possible steps are from -8,192 to +8,191.

The pulses which are added to or subtracted from the 64 Hz clock are spread evenly over each 8,192 second period using the ABRACON patented Distributed Calibration algorithm. This insures that in RC mode the maximum cycle-to-cycle jitter in any clock of a frequency 64 Hz or lower caused by calibration will be no more than one 64 Hz period. This maximum jitter applies to all clocks in the AB18XX, including the Calendar Counter, Countdown Timer and Watchdog Timer clocks and any clock driven onto the CLKFOUT/nIRQ pin.

Note that if the XT Oscillator is selected, the RC Calibration logic is disabled because the 128 Hz clock will have already been calibrated by the XT Calibration logic.

4.8.2.1 RC Calibration Process

The RC oscillator calibration value is determined by the following process:

1) Set the OFFSETR and CMDR register fields to 0 to insure calibration is not occurring.
2) Select the RC oscillator by setting the OSEL bit to 1.
3) Configure a square wave output on one of the output pins of frequency Fnom (for example, 16 Hz).
4) Measure the frequency Fmeas at the output pin.
5) Compute the adjustment value required in ppm as ((Fnom – Fmeas)*1000000)/Fmeas = PAdj
6) Compute the adjustment value in steps as PAdj/(1000000/2^19) = PAdj/(1.90735) = Adj
7) If Adj < -65,536, the RC frequency is too high to be calibrated
8) Else if Adj < -32,768, set CMDR = 3, OFFSETR = Adj/8
9) Else if Adj < -16,384, set CMDR = 2, OFFSETR = Adj/4
10) Else if Adj < -8,192, set CMDR = 1, OFFSETR = Adj/2
11) Else if Adj < 8192, set CMDR = 0, OFFSETR = Adj
12) Else if Adj < 16,384, set CMDR = 1, OFFSETR = Adj/2
13) Else if Adj < 32,768, set CMDR = 2, OFFSETR = Adj/4
14) Else if Adj < 65,536, set CMDR = 3, OFFSETR = Adj/8
15) Else the RC frequency is too low to be calibrated

4.9 Autocalibration

The AB18XX includes a very powerful, patented automatic calibration feature, referred to as Autocalibration, which allows the RC Oscillator to be automatically calibrated to the XT Oscillator. The XT Oscillator typically has

much better stability than the RC Oscillator but the RC Oscillator requires significantly less power. Autocalibration enables many system configurations to achieve accuracy and stability similar to that of the XT Oscillator while drawing current similar to that of the RC Oscillator. Autocalibration functions in two primary modes: XT Autocalibration Mode and RC Autocalibration Mode.

4.9.1 Autocalibration Operation

The Autocalibration operation counts the number of calibrated XT clock cycles within a specific period as defined by the RC Oscillator and then loads new values into the Calibration RC Upper and RC Lower registers which will then adjust the RC Oscillator output to match the XT frequency.

4.9.2 XT Autocalibration Mode

In XT Autocalibration Mode, the OSEL register bit is 0 and the AB18XX uses the XT Oscillator whenever the system power VCC is above the V_{CCSWF} voltage. The RC Oscillator is periodically automatically calibrated to the XT Oscillator. If the AOS bit is set, when VCC drops below the V_{CCSWF} threshold the system will switch to using VBAT, the clocks will begin using the RC Oscillator, autocalibration will be disabled and the XT Oscillator will be disabled to reduce power requirements. Because the RC Oscillator has been continuously calibrated to the XT Oscillator, it will be very accurate when the switch occurs. When VCC is again above the threshold, the system will switch back to use the XT Oscillator and restart autocalibration.

4.9.3 RC Autocalibration Mode

In RC Autocalibration Mode, the OSEL register bit is 1 and the AB18XX uses the RC Oscillator at all times. However, periodically the XT Oscillator is turned on and the RC Oscillator is calibrated to the XT Oscillator. This allows the system to operate most of the time with the XT Oscillator off but allow continuous calibration of the RC Oscillator.

4.9.4 Autocalibration Frequency and Control

The Autocalibration function is controlled by the ACAL field in the Oscillator Control register as shown in Table 14. If ACAL is 00, no Autocalibration occurs. If ACAL is 10 or 11, Autocalibration occurs every 1024 or 512 seconds. In RC Autocalibration Mode, an Autocalibration operation results in the XT Oscillator being enabled for roughly 50 seconds. The 512 second Autocalibration cycles have the XT Oscillator enabled approximately 10% of the time, while 1024 second Autocalibration cycles have the XT Oscillator enabled approximately 4% of the time.

Table 14 – Autocalibration Modes

ACAL Value	Calibration Mode
00	No Autocalibration
01	RESERVED
10	Autocalibrate every 1024 seconds (~17 minutes)
11	Autocalibrate every 512 seconds (~9 minutes)

If ACAL is 00 and is then written with a different value, an Autocalibration cycle is immediately executed. This allows Autocalibration to be completely controlled by software. As an example, software could choose to execute an Autocalibration cycle every 2 hours by keeping ACAL at 00, getting a two hour interrupt using the alarm function, generating an Autocalibration cycle by writing ACAL to 10 or 11, and then returning ACAL to 00.

4.9.5 Autocalibration Fail

If the temperature exceeds the specification of the AB18XX or internal adjustment parameters are altered incorrectly, it is possible that the basic frequency of the RC Oscillator is so far away from the nominal 128 Hz value (off by more than 12%) that the RC Calibration circuitry does not have enough range to correctly calibrate

the RC Oscillator. If this situation is detected during an Autocalibration operation, the ACF interrupt flag is set, an external interrupt is generated if the ACIE register bit is set and the Calibration RC registers are not updated.

4.10 Oscillator Failure Detection

If the 32 kHz XT Oscillator generates clocks at less than 8 kHz for a period of more than 32 ms, the AB18XX detects an Oscillator Failure. The Oscillator Failure function is controlled by several bits in the Oscillator Control Register (see section 5.7.1) and the Oscillator Status Register (see Section 0). The OF flag is set when an Oscillator Failure occurs, and is also set when the AB18XX initially powers up. If the OFIE bit is set, the OF flag will generate an interrupt on IRQ. The current status of the XT Oscillator can be read in the XTF bit, which will be a 1 if the XT Oscillator is not running at least 8 kHz. Note that XTF will always be set if the RC Oscillator is currently selected.

If the FOS bit is set and the AB18XX is currently using the XT Oscillator, it will automatically switch to the RC Oscillator on an Oscillator Failure. This guarantees that the system clock will not stop in any case. If the XT Oscillator experiences a temporary failure and subsequently restarts, the AB18XX will switch back to the XT Oscillator. The OMODE bit indicates the currently selected oscillator, which will not match the oscillator requested by the OSEL bit if the XT Oscillator is not running.

4.11 Interrupts

The AB18XX may generate a variety of interrupts which are ORed into the IRQ signal. This may be driven onto either the FOUT/nIRQ pin or the PSW/nIRQ2 pin depending on the configuration of the OUT1S and OUT2S fields (see Section 5.3.3).

4.11.1 Interrupt Summary

The possible interrupts are summarized in Table 15. All enabled interrupts are ORed into the IRQ signal when their respective flags are set. Note that most interrupt outputs use the inverse of the interrupt, denoted as e.g. nIRQ. The fields are:

Interrupt - the name of the specific interrupt.
Function - the functional area which generates the interrupt.
Enable - the register bit which enables the interrupt. Note that for the Watchdog interrupt, WDS is the steering bit, so that the flag generates an interrupt if WDS is 0 and a reset if WDS is 1. In either case, the BMB field must be non-zero to generate the interrupt or reset.
Pulse/Level - some interrupts may be configured to generate a pulse based on the register bits in this column. "Level Only" implies that only a level may be generated, and the interrupt will only go away when the flag is reset by software.
Flag - the register bit which indicates that the function has occurred. Note that the flag being set will only generate an interrupt signal on an external pin if the corresponding interrupt enable bit is also set.

Table 15 - Interrupt Summary

Interrupt	Function	Enable	Pulse/Level	Flag
AIRQ	Alarm Match	AIE	IM	ALM
TIRQ	Countdown Timer	TIM	TM	TIM
WIRQ	Watchdog	!WDS	Level Only	WDT
BLIRQ	Battery Low	BLIE	Level Only	BL
X1IRQ	External 1	EX1E	Level Only	EX1
X2IRQ	External 2	EX2E	Level Only	EX2
OFIRQ	Oscillator Fail	OFIE	Level Only	OF
ACIRQ	Autocal Fail	ACIE	Level Only	ACF

4.11.2 Alarm Interrupt AIRQ

The AB18XX may be configured to generate the AIRQ interrupt when the values in the Time and Date Registers match the values in the Alarm Registers. Which register comparisons are required to generate AIRQ is controlled by the RPT field as described in Table 22, allowing software to specify the interrupt interval. When an Alarm Interrupt is generated, the ALM flag is set and an external interrupt is generated based on the AIE bit and the pin configuration settings. The IM field controls the period of the external interrupt as described in Table 19, including both level and pulse configurations.

4.11.3 Countdown Timer Interrupt TIRQ

The AB18XX may be configured to generate the TIRQ interrupt when the Countdown Timer is enabled by the TE bit and reaches the value of zero, which will set the TIM flag. The TM, TRPT and TFS fields control the interrupt timing (see Section 5.6.1), and the TIE bit and the pin configuration settings control external interrupt generation. The Timer interrupt is always driven onto the nTIRQ pin if it is available, and may also be driven onto the CLKFOUT/nIRQ3 pin by a configuration of the SQFS field (see Section 5.3.5).

4.11.4 Watchdog Timer Interrupt WIRQ

The AB18XX may be configured to generate the WIRQ interrupt when the Watchdog Timer reaches its timeout value. This sets the WDT flag and is described in Section 4.7.

4.11.5 Battery Low Interrupt BLIRQ

The AB18XX may be configured to generate the BLIRQ when the voltage on the VBAT pin crosses one of the thresholds set by the BREF field. The polarity of the detected crossing is set by the BPOL bit.

4.11.6 External Interrupts X1IRQ and X2IRQ

The AB18XX may be configured to generate the X1IRQ and X2IRQ interrupts when the EXTI (X1IRQ) or WDI (X2IRQ) inputs toggle. The register bits EX1P and EX2P control whether the rising or falling transitions generate the respective interrupt. Changing EX1P or EX2P may cause an immediate interrupt, so the corresponding interrupt flag should be cleared after changing these bits.

The values of the EXTI and WDI pins may be directly read in the EXIN and WDIN register bits (see Section 5.11.1). By connecting an input such as a pushbutton to both EXTI and WDI, software can debounce the switch input using software configurable delays.

4.11.7 Oscillator Fail Interrupt OFIRQ

The AB18XX may be configured to generate the OFIRQ interrupt if the XT oscillator fails (see Section 4.10).

4.11.8 Autocalibration Fail Interrupt ACIRQ

The AB18XX may be configured to generate the ACIRQ interrupt if an autocalibration operation fails (see Section 4.9.5).

4.11.9 Servicing Interrupts

When an interrupt is detected, software must clear the interrupt flag in order to prepare for a subsequent interrupt. If only a single interrupt is enabled, software may simply write a zero to the corresponding interrupt flag to clear the interrupt. However, because all of the flags in the Status register are written at once, it is possible to clear an interrupt which has not been detected yet if multiple interrupts are enabled. The ARST register bit is provided to insure that interrupts are not lost in this case. If ARST is a 1, a read of the Status register will produce the current state of all the interrupt flags and then clear them. An interrupt occurring at any time relative to this read is guaranteed to either produce a 1 on the Status read, or to set the corresponding flag after the clear caused by the Status read. After servicing all interrupts which produced 1s in the read, software should read the Status register again until it returns all zeroes in the flags, and service any interrupts with flags of 1.

Note that the OF and ACF interrupts are not handled with this process because they are in the Oscillator Status register, but error interrupts are very rare and typically do not create any problems if the interrupts are cleared by writing the flag directly.

4.12 Power Control and Switching

The main power supply to the AB18XX is the VCC pin, which operates over the range of 1.7 V to 3.6 V if I/O interface operations are required, and the range of 1.5 V to 3.6 V if only timekeeping operations are required. Some versions also include a backup supply which is provided on the VBAT pin and must be in the range of 1.5 V to 3.6 V in order to supply battery power if VCC is below 1.5 V. There are several functions which are directly related to the VBAT input. If a single power supply is used it must be connected to the VCC pin.

Figure 18 shows the various power states and the transitions between them. There are three power states:

1) POR – the power on reset state. If the AB18XX is in this state, all registers including the Counter Registers are initialized to their reset values.
2) VCC Power – the AB18XX is powered from the VCC supply.
3) VBAT Power – the AB18XX is powered from the VBAT supply.

Initially, VCC is below the V_{CCST} voltage, VBAT is below the V_{BATSW} voltage and the AB18XX is in the POR state. VCC rising above the V_{CCST} voltage causes the AB18XX to enter the VCC Power state. If VBAT remains below V_{BATSW}, VCC falling below the V_{CCRST} voltage returns the AB18XX to the POR state.

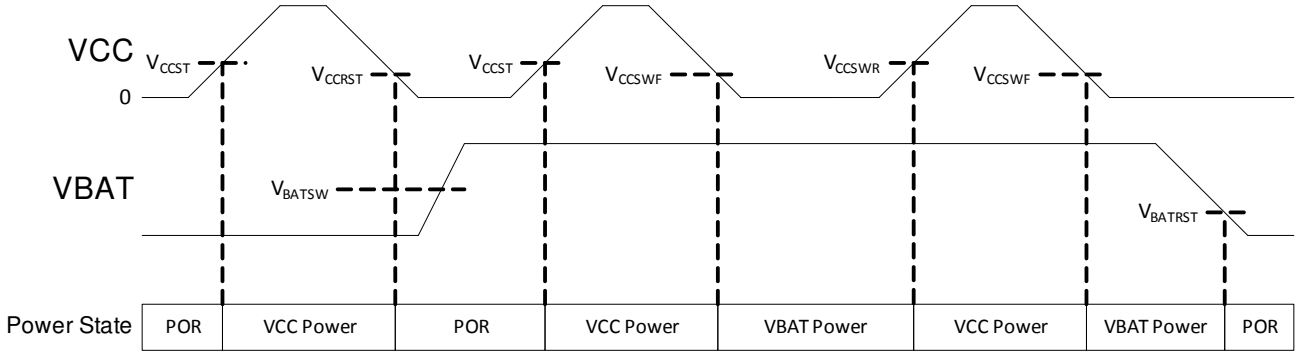


Figure 18 – Power States

If VBAT rises above V_{BATSW} in the POR state, the AB18XX remains in the POR state. This allows the AB18XX to be built into a module with a battery included, and minimal current will be drawn from the battery until VCC is applied to the module the first time.

If the AB18XX is in the VCC Power state and VBAT rises above V_{BATSW}, the AB18XX remains in the VCC Power state but automatic switchover becomes available. VBAT falling below V_{BATSW} has no effect on the power state as long as VCC remains above V_{CCSWF}. If VCC falls below the V_{CCSWF} voltage while VBAT is above V_{BATSW} the AB18XX switches to the VBAT Power state. VCC rising above V_{CCSWR} returns the AB18XX to the VCC Power state. There is hysteresis in the rising and falling VCC thresholds to insure that the AB18XX does not switch back and forth between the supplies if VCC is near the thresholds. V_{CCSWF} and V_{CCSWR} are independent of the VBAT voltage and allow the AB18XX to minimize the current drawn from the VBAT supply by switching to VBAT only at the point where VCC is no longer able to power the device.

If the AB18XX is in the VBAT Power state and VBAT falls below V_{BATRST}, the AB18XX will return to the POR state.

Whenever the AB18XX enters the VBAT Power state, the BAT flag in the Status Register (see Section 5.3.1) is set and may be polled by software. If the XT oscillator is selected and the AOS bit (see Section 5.7.1) is set, the AB18XX will automatically switch to the RC oscillator in the VBAT Power state in order to conserve battery power. If the IOBM bit (see Section 5.9.3) is clear, the I^2C or SPI interface is disabled in the VBAT Power state in order to prevent erroneous accesses to the AB18XX if the bus master loses power.

4.12.1 Battery Low Flag and Interrupt

If the VBAT voltage drops below the Falling Threshold selected by the BREF field (see Section 0), the BL flag in the Status Register (see Section 5.3.1) is set. If the BLIE interrupt enable bit (see Section 5.3.4) is set, the IRQ interrupt is generated. This allows software to determine if a backup battery has been drained. Note that the BPOL bit must be set to 0. The algorithm in the Analog Comparator section (4.12.2) should be used when configuring the BREF value.

4.12.2 Analog Comparator

If a backup battery is not required, the VBAT pin may be used as an analog comparator input. The voltage comparison level is set by the BREF field. If the BPOL bit is 0, the BL flag will be set when the VBAT voltage crosses from above the BREF Falling Threshold to below it. If the BPOL bit is 1, the BL flag will be set when the VBAT voltage crosses from below the BREF Rising Threshold to above it. The BBOD bit in the Analog Status Register (see Section 5.9.4) may be read to determine if the VBAT voltage is currently above the BREF threshold (BBOD = 1) or below the threshold (BBOD = 0).

There is a reasonably large delay t_{BREF} (on the order of seconds) between changing the BREF field and a valid value of the BBOD bit. Therefore, the algorithm for using the Analog Comparator should comprise the following steps:

1) Set the BREF and BPOL fields to the desired values.
2) Wait longer than the maximum t_{BREF} time.
3) Clear the BL flag, which may have been erroneously set as BBOD settles.
4) Check the BBOD bit to insure that the VBAT pin is at a level for which an interrupt can occur. If a falling interrupt is desired (BPOL = 0), BBOD should be 1. If a rising interrupt is desired (BPOL = 1), BBOD should be 0.

If the comparison voltage on the VBAT pin can remain when VCC goes to 0, it is recommended that a Software Reset (see Section 4.14) be generated to the AB18XX after power up.

4.12.3 Pin Control and Leakage Management

Like most ICs, the AB18XX may draw unnecessary leakage current if an input pin floats to a value near the threshold or an output pin is pulled to a power supply. Because external devices may be powered from VCC, extra care must be taken to insure that any input or output pins are handled correctly to avoid extraneous leakage when VCC goes away and the AB18XX is powered from VBAT. The Output Control register (see Section 5.9.5), the Batmode IO register (see Section 5.9.3) and the Extension RAM Address register (see Section 5.11.1) include bits to manage this leakage, which should be used as follows:

1) EXBM should be cleared if the EXTI pin is connected to a device which is powered down when the AB18XX is in the VBAT Power state.
2) WDBM should be cleared if the WDI pin is connected to a device which is powered down when the AB18XX is in the VBAT Power state.
3) O4BM should be cleared if the CLKOUT/nIRQ3 pin is connected to a device which is when the AB18XX is in the VBAT Power state.
4) IOBM should be cleared if the I^2C or SPI bus master is powered down when the AB18XX is in the VBAT Power state.

4.12.4 Power Up Timing

When the voltage levels on both the VCC and VBAT signals drop below V_{CCRST}, the AB18XX will enter the POR state. Once VCC rises above V_{CCST}, the AB18XX will enter the VCC Power state. I/O accesses via the I^2C or SPI interface will be disabled for a period of PUDEL (typically 300 ms). The FOUT/nIRQ pin will be low at power up, and will go high when PUDEL expires. Software should poll the FOUT/nIRQ value to determine when the AB18XX may be accessed. Figure 19 shows the timing of a power down/up operation.

Figure 19 – Power Up Timing

4.13 Reset Summary

The AB18XX controls the nRST output in a variety of ways, as shown in Table 16. The assertion of nRST is a low signal if the RSP bit is 0, and the assertion is high if RSP is 1.

Table 16 - Reset Summary

Function	Enable
Power Up	Always Enabled
nEXTR Pin	RS1E
Watchdog	WDS
Sleep	SLRES

4.13.1 Power Up Reset

When the AB18XX powers down (see Section 4.11.8) FOUT/nIRQ and nRST will be asserted low until I/O accesses are enabled. At that point FOUT/nIRQ will go high, and nRST will continue to be asserted for the delay RSTIM, and will then be deasserted. Figure 20 shows the reset timing on Power Up. Software should sample the FOUT/nIRQ signal prior to accessing the AB18XX.

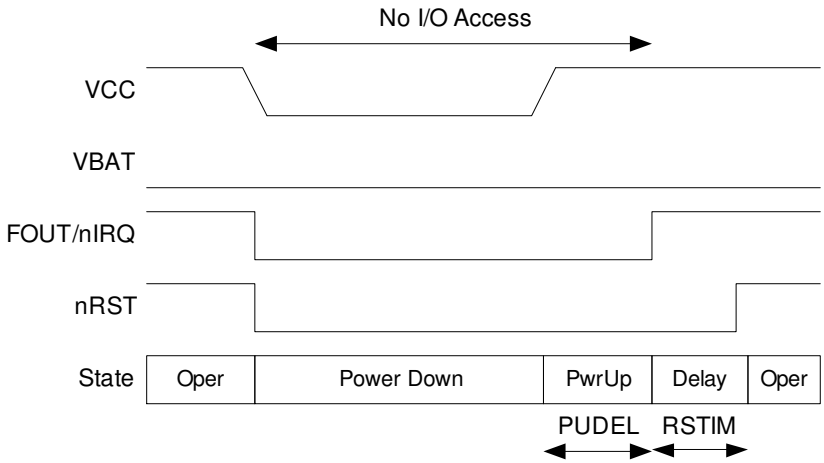


Figure 20 – Power Up Reset Timing

4.13.2 nEXTR

If the RS1E bit is set, nRST will be asserted whenever the nEXTR input pin is low. If no other sources are asserting nRST, the nRST pin will be deasserted immediately upon nEXTR going high with no delay.

4.13.3 Watchdog Timer

If the WDS bit is 1, expiration of the Watchdog Timer (see Section 4.7) will cause nRST to be asserted for approximately 60 ms.

4.13.4 Sleep

If the SLRES bit is set, nRST will be asserted whenever the AB18XX is in Sleep Mode (see Section 4.15). Once a trigger is received and the AB18XX exits Sleep Mode, nRST will continue to be asserted for the RSTIM delay. Figure 21 shows the timing of this operation.

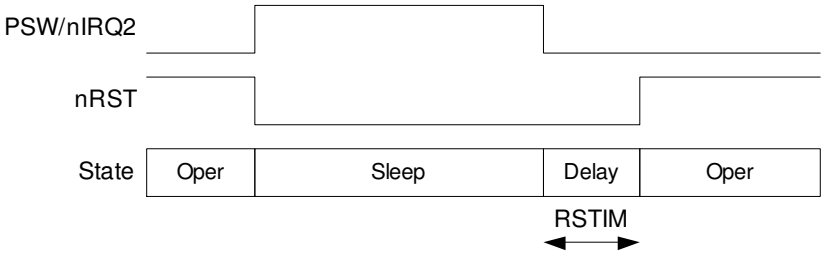


Figure 21 – Sleep Reset Timing

4.14 Software Reset

Software may reset the AB18XX by writing the special value of 0x3C to the Configuration Key register at offset 0x1F. This will provide the equivalent of a power on reset by initializing all of the AB18XX registers.

A software reset will not cause the nRST signal the be asserted.

4.15 Sleep Control

The AB18XX includes a sophisticated Sleep Control system that allows the AB18XX to manage power for other chips in a system. The Sleep Control system provides two outputs which may be used for system power control:

1) A reset (**nRST**) may be generated to put any host controller into a minimum power mode and to control sequencing during power up and power down operations.
2) A power switch signal may be generated (**PWR**), which allows the AB18XX to completely power down other chips in a system by allowing the PSW/nIRQ2 pin to float. The OUT2S field (see Section 5.3.3) must be set to a value of 6 to select the SLEEP output. When using the PWR output, PSW/nIRQ2 is configured as an open drain pin with approximately 1 Ω resistance. This allows the AB18XX to directly switch power with no external components for small systems, or to control a single external transistor for higher current switching. The low resistance power switch is enabled by setting the PWR2 bit (see Section 5.3.2). If the I^2C or SPI master (i.e., the host controller) is powered down by the power switch, the PWGT bit (see Section 5.7.1) should be set to insure that a floating bus does not corrupt the AB18XX.
3) If OUT2S is 6 but the PWR2 bit is not set, PSW/nIRQ2 will be configured as a high true Sleep output which may be used as an interrupt.

The Sleep state machine in Figure 22 receives several inputs which it uses to determine the current Sleep State:

1) **POR** – the indicator that power is valid, i.e. the AB18XX is in either the VCC Power state or the VBAT Power state.
2) **SLP** - the Sleep Request signal which is generated by a software access to the Sleep Register (see Section 5.5.1).
3) **TRIG** - the OR of the enabled interrupt request from the Alarm comparison in the RTC, the interrupt signal from the Countdown Timer in the RTC, the interrupt signal from the Watchdog Timer in the RTC, the External Interrupt 1 or 2 pins, the Battery Low detection interrupt, the Autocalibration Fail interrupt or the Oscillator Fail interrupt.
4) **TIM** - the timeout signal from the SL Timeout counter, indicating that it has decremented to 0.

4.15.1 RUN

RUN is the normal operating state of the AB18XX. PWR and nRST are not asserted, SLP is 0, and SLST holds the state of the previous Sleep. SLST should be cleared by software before entering the SWAIT state.

4.15.2 SWAIT

Software can put the chip to sleep by setting the SLP bit, as long as a valid interrupt is enabled (see Section 4.15.5) indicated by VAL being asserted. If SLTO is between 1 and 7, the SM moves to the SWAIT state and waits for between SLTO and (SLTO+1) ~8 ms periods. This allows software to perform additional cleanup after setting SLP before the MCU is shut down. Operation is the same in SWAIT as it is in RUN, and if an enabled operational interrupt occurs (TRIG) the SM returns to the RUN state and clears the SLP bit. PWR and nRST are not asserted, SLP is 1, and SLST is 0.

If SLTO is set to 0, the SM moves immediately to the SLEEP state. If the MCU is configured to be powered down in Sleep Mode, the I/O operation to write the Sleep Register must be the last instruction executed by the MCU.

4.15.3 SLEEP

Once the programmed number of periods has elapsed in the SWAIT state, the TIM signal is asserted and the machine moves to the SLEEP state, putting the AB18XX into Sleep Mode. In this case the PWR signal is removed, and nRST is asserted if SLRES is set. Once an enabled operational interrupt occurs (TRIG), the SM returns to the RUN state, reenables power and removes reset as appropriate. The SLST register bit is set when the SLEEP state is entered, allowing software to determine if a SLEEP has occurred.

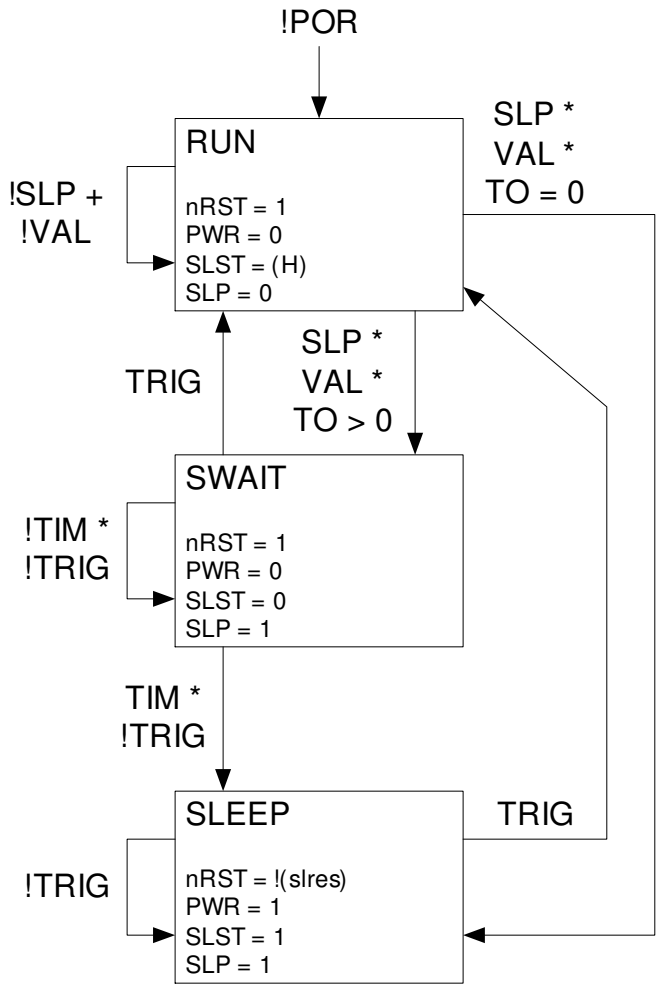


Figure 22 – Sleep State Machine

4.15.5 SLP Protection

Since going into Sleep Mode may prevent an MCU from accessing the AB18XX, it is critical to insure that the AB18XX can receive a TRIG signal. To guarantee this, the SLP signal cannot be set unless the STOP bit is 0 and at least one of the following conditions exists:

1) The AIE bit is 1, enabling an Alarm interrupt.
2) The TIE and the TE bits are 1, enabling a Countdown Timer interrupt.
3) The EX1E or EX2E bits are a 1, enabling an External interrupt.
4) The BMB field is not zero and the WDS bit is zero, enabling a Watchdog Interrupt

In addition, SLP cannot be set if there is an interrupt pending. Software should read the SLP bit after attempting to set it. If SLP is not asserted, the attempt to set SLP was unsuccessful either because a correct trigger was not enabled or because an interrupt was already pending. Once SLP is set, software should continue to poll it until the Sleep actually occurs, in order to handle the case where a trigger occurs before the AB18XX enters Sleep Mode.

4.15.6 OUT2S, OUTB and LKO2

If the OUT2S field is set to the initial value of 7, the PSW/nIRQ2 pin will be driven with the value of the OUTB bit which is initially zero. If this pin is used as the power switch, setting OUTB will remove power from the system and may prevent further access to the AB18XX. In order to insure that this does not happen inadvertently, the LKO2 bit must be cleared in order to change the OUTB bit to a 1. Note that in this power switch environment the OUT2S register field must not be written to any value other than 6 or 7, even if the PSW/nIRQ2 pin would remain at zero, because it is possible that a short high pulse could be generated on the PSW/nIRQ2 pin which could create a power down.

4.15.7 Pin Control and Leakage Management

Like most ICs, the AB18XX may draw unnecessary leakage current if an input pin floats to a value near the threshold or an output pin is pulled to a power supply. Because Sleep Mode can power down external devices connected to the AB18XX, extra care must be taken to insure that any input or output pins are handled correctly to avoid extraneous leakage. The Output Control register (see Section 5.9.5) includes bits to manage this leakage, which should be used as follows:

5) EXDS should be set if the EXTI pin is connected to a device which is powered down in Sleep Mode.
6) WDDS should be set if the WDI pin is connected to a device which is powered down in Sleep Mode.
7) O1EN should be cleared if the FOUT/nIRQ pin is connected to a device which is powered down in Sleep Mode.
8) O3EN should be cleared if the nTIRQ pin is connected to a device which is powered down in Sleep Mode (I^2C devices only).
9) O4EN should be cleared if the CLKOUT/nIRQ3 pin is connected to a device which is powered down in Sleep Mode.
10) RSEN should be cleared if the nRST pin is connected to a device which is powered down in Sleep Mode.

4.16 System Power Control Applications

The AB18XX enables a variety of system implementations in which the AB18XX can control power usage by other elements in the system. This is typically used when the entire system is powered from a battery and minimizing total power usage is critical.

4.16.1 VSS Power Switched

Figure 23 shows the recommended implementation, in which the internal power switch of the AB18XX is used to completely turn off the MCU and/or other system elements. In this case the PSW/nIRQ2 output is configured to generate the SLEEP function, and the SLRES bit is set to 0. Under normal circumstances, the PSW/nIRQ2pin is pulled to VSS with approximately 1 Ω of resistance, so that the MCU receives full power. The MCU initiates a SLP operation, and when the AB18XX enters the SLEEP state the PSW/nIRQ2 pin is opened and power is completely removed from the MCU. This results in significant additional power savings relative to the other alternatives.

The AB18XX normally powers up selecting the OUTB register bit to drive the PSW/nIRQ2 pin, and the OUTB bit is zero. This insures that the power switch is enabled at power up. If the power switch function is used, software should only change the PSW/nIRQ2 selection between OUTB (0b111) and SLEEP (0b110) to insure no glitches occur in the power switching function.

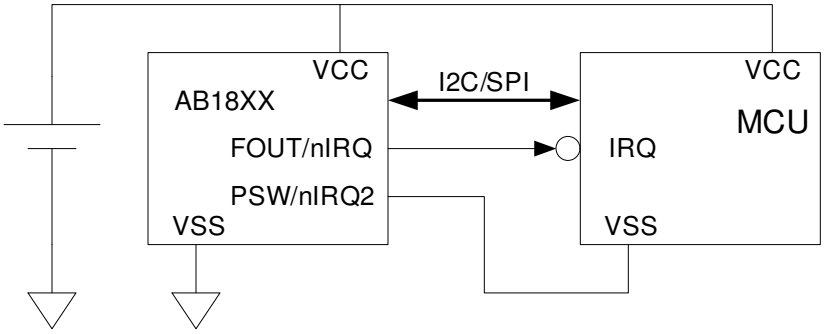


Figure 23 – Switched VSS Power Control

4.16.2 VCC Power Switched

Figure 24 shows the application in which an external transistor switch T is used to turn off power to the MCU. The SLP function operates identically to the VSS switched case above, but this implementation allows switching higher current and maintains a common ground. R can be on the order of megohms, so that negligible current is drawn when the circuit is active and PSW/nIRQ2 is low.

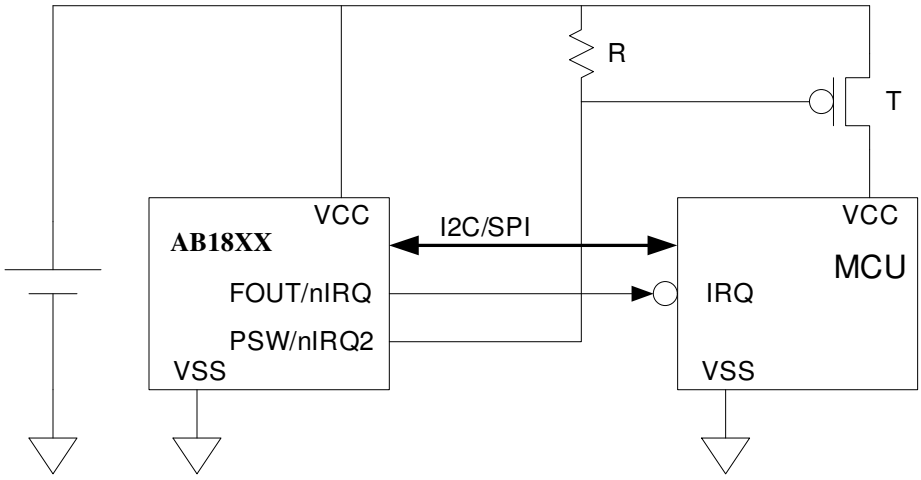


Figure 24 – Switched VCC Power Control

4.16.3 Reset Driven

Figure 25 shows the application in which the AB18XX communicates with the system MCU using the reset function. In this case the MCU sets the SLRES bit so that when the AB18XX enters the SLEEP state, it brings nRST low to reset the MCU, and initiates a SLP operation. When the trigger occurs, the AB18XX releases the MCU from reset, and may also generate an interrupt which the MCU can query to determine how reset was exited. Since some MCUs use much less power when reset, this implementation can save system power.

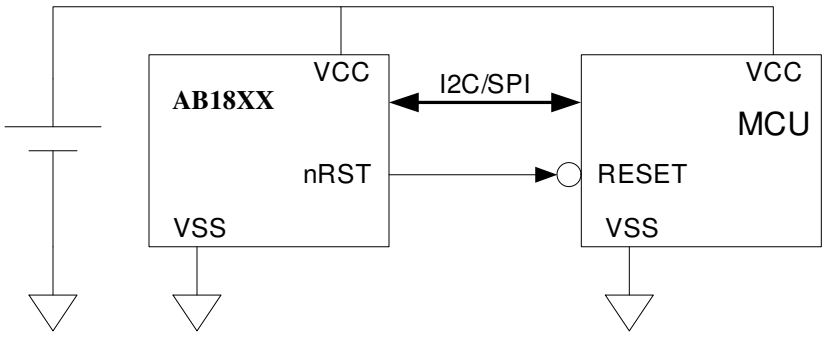


Figure 25 – Reset Driven Power Control

One potential issue with this approach is that many MCUs include internal pullup resistors on their reset inputs, and the current drawn through that resistor when the reset input is held low is generally much higher than the MCU would draw in its inactive state. Any pullup resistor should be disabled and the nRST output of the AB18XX should be configured as a push-pull output.

4.16.4 Interrupt Driven

Figure 26 shows the simplest application, in which the AB18XX communicates with the system MCU using an interrupt. The MCU can go into standby mode, reducing power somewhat, until the AB18XX generates an interrupt based on an alarm or a timer function.

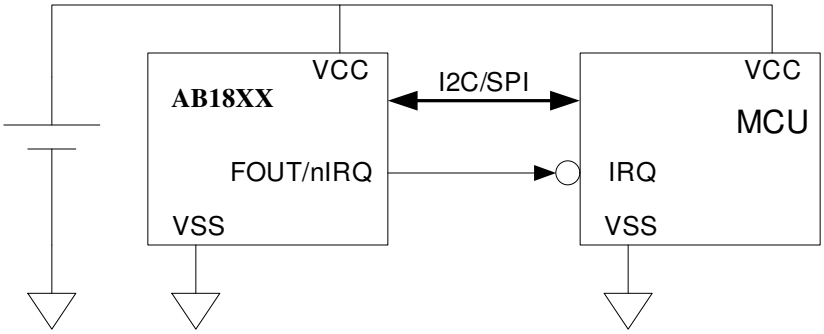


Figure 26 – Interrupt Driven Power Control

4.17 Trickle Charger

The AB18XX includes a trickle charging circuit which allows a battery or supercapacitor connected to the VBAT pin to be charged from the power supply connected to the VCC pin. The circuit of the Trickle Charger is shown in Figure 27. The Trickle Charger configuration is controlled by the Trickle register (see Section 5.9.1). The Trickle Charger is enabled if a) the TCS field is 1010, b) the DIODE field is 01 or 10 and c) the ROUT field is not 00. A diode, with a typical voltage drop of 0.7V, is inserted in the charging path if DIODE is 10. The series current limiting resistor is selected by the ROUT field as shown in the figure.

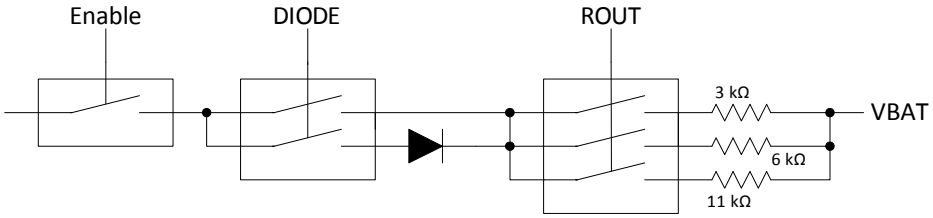


Figure 27 – Trickle Charger

5. Register Descriptions

Registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte. Table 12 and Table 13 summarize the function of each register. In Table 12, the GPx bits (where x is between 0 and 27) are 28 register bits which may be used as general purpose storage. These bits are not described in the Sections below. All of the GPx bits are cleared when the AB18XX powers up, and they can therefore be used to allow software to determine if a true Power On Reset has occurred or hold other initialization data.

5.1 Time and Date Registers

5.1.1 00 - Hundredths (Reset Value = 0x99)

This register holds the count of hundredths of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 99. Note that in order to divide from 32 kHz, the hundredths register will not be fully accurate at all times but will be correct every 500 ms. Maximum jitter of this register will be less than 1 ms. The Hundredths Counter is not valid if the 128 Hz RC Oscillator is selected.

5.1.2 01 - Seconds (Reset Value = 0x00)

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

5.1.3 02 - Minutes (Reset Value = 0x00)

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

5.1.4 03 - Hours (Reset Value = 0x00)

This register holds the count of hours, in two binary coded decimal (BCD) digits. Values will be from 00 to 23 if the 12/24 bit is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours, and hour values will range from 1 to 12.

5.1.5 04 - Date (Reset Value = 0x01)

This register holds the current day of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

5.1.6 05 - Months (Reset Value = 0x01)

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

5.1.7 06 - Years (Reset Value = 0x00)

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

5.1.8 07 - Weekday (Reset Value = 0x00)

This register holds the current day of the week. Values will range from 0 to 6.

5.2 Alarm Registers

5.2.1 08 - Hundredths Alarm (Reset Value = 0x00)

This register holds the alarm value for hundredths of seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

5.2.2 09 - Seconds Alarm (Reset Value = 0x00)

This register holds the alarm value for seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

5.2.3 0A - Minutes Alarm (Reset Value = 0x00)

This register holds the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

5.2.4 0B - Hours Alarm (Reset Value = 0x00)

This register holds the alarm value for hours, in two binary coded decimal (BCD) digits. Values will range from 00 to 23 if the 12/24 bit is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours, and hour values will be from 1 to 12.

5.2.5 0C - Date Alarm (Reset Value = 0x00)

This register holds alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

5.2.6 0D - Months Alarm (Reset Value = 0x00)

This register holds alarm value for months, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

5.2.7 0E - Weekday Alarm (Reset Value = 0x00)

This register holds the alarm value for the day of the week. Values will range from 0 to 6.

5.3 Configuration Registers

5.3.1 0F - Status

This register holds a variety of status bits. The register may be written at any time to clear or set any status flag. If the ARST bit is set, any read of the Status Register will clear all of the bits except CB.

CB [7] - century. This bit will be toggled when the Years register rolls over from 99 to 00 if the CEB bit is a 1. A 0 assumes the century is 19xx or 21xx, and a 1 assumes it is 20xx for leap year calculations.
BAT [6] - set when the system switches to the VBAT Power state.
WDT [5] - set when the Watchdog Timer is enabled and is triggered, and the WDS bit is 0.
BL [4] - set if the battery voltage VBAT crosses the reference voltage selected by BREF in the direction selected by BPOL.
TIM [3] - set when the Countdown Timer is enabled and reaches zero.
ALM [2] - set when the Alarm function is enabled and all selected Alarm registers match their respective counters.
EX2 [1] - set when an external trigger is detected on the WDI pin. The EX2E bit must be set in order for this interrupt to occur, but subsequently clearing EX2E will not automatically clear this flag.
EX1 [0] - set when an external trigger is detected on the EXTI pin. The EX1E bit must be set in order for this interrupt to occur, but subsequently clearing EX1E will not automatically clear this flag.

5.3.2 10 - Control1 (Reset Value = 0x13)

This register holds some major control signals.

STOP [7] - when 1, stops the oscillator. This bit allows the oscillator to be precisely started, by setting it to 1 and back to 0. The clock is guaranteed to start within one second.
12/24 [6] - when 0, the Hours register operates in 24 hour mode. When 1, the Hours register operates in 12 hour mode.
OUTB [5] - a static value which may be driven on the PSW/nIRQ2 pin. The OUTB bit cannot be set to 1 if the LKO2 bit is 1.
OUT [4] - a static value which may be driven on the FOUT/nIRQ pin. This bit also defines the default value for the Square Wave output when SQWE is not asserted.
RSP [3] – Reset Polarity. When 1, the nRST pin is asserted high. When 0, the nRST pin is asserted low.
ARST [2] - auto reset enable. When 1, a read of the Status register will cause any interrupt bits (TIM, BL, ALM, WDT, XT1, XT2) to be cleared. When 0, the bits must be explicitly cleared by writing the Status register.
PWR2 [1] - when 1, the PSW/nIRQ2 pin is driven by an approximately 1 Ω pulldown which allows the AB18XX to switch power to other system devices through this pin. When 0, the PSW/nIRQ2pin is a normal open drain output.
WRTC [0] - write RTC. This bit must be set in order to write any of the Counter registers (Hundredths, Seconds, Minutes, Hours, Date, Months, Years or Weekdays).

5.3.3 11 - Control2 (Reset Value = 0x3C)

This register holds additional control and configuration signals for the flexible output pins FOUT/nIRQ and PSW/nIRQ2. Note that PSW/nIRQ2 is an open drain output, and FOUT/nIRQ is open drain if OUTPP is 0 and push-pull if OUTPP is 1.

OUTPP [7] – if 1, the FOUT/nIRQ and nTIRQ (in I^2C mode only) are push-pull. If 0, these outputs are open drain.
RS1E [5] - when 1, enable the nEXTR pin to generate nRST.
OUT2S [4:2] - controls the function of the PSW/nIRQ2 pin, as shown in Table 17.
OUT1S [1:0] - controls the function of the FOUT/NIRQ pin, as shown in Table 18.

Table 17 – PSW/nIRQ2 Pin Control

OUT2S Value	PSW/nIRQ2 Pin Function
000	nIRQ if at least one interrupt is enabled, else OUTB
001	SQW if SQWE = 1, else OUTB
010	RESERVED
011	nAIRQ if AIE is set, else OUTB
100	TIRQ if TIE is set, else OUTB
101	nTIRQ if TIE is set, else OUTB
110	SLEEP
111	OUTB

Table 18 - FOUT/nIRQ Pin Control

OUT1S Value	FOUT/nIRQ Pin Function
00	nIRQ if at least one interrupt is enabled, else OUT
01	SQW if SQWE = 1, else OUT
10	SQW if SQWE = 1, else nIRQ if at least one interrupt is enabled, else OUT
11	nAIRQ if AIE is set, else OUT

5.3.4 12 - Interrupt Mask (Reset Value = 0xE0)

This register holds the interrupt enable bits and other configuration information.

CEB [7] - century enable. When 1, the CB bit will toggle when the Years register rolls over from 99 to 00. When 0, the CB bit will never be automatically updated.
IM [6:5] - interrupt mode. This controls the length of nAIRQ as shown in Table 19. The interrupt output always goes high when the corresponding flag in the Status Register is cleared. In order to minimize current drawn by the AB18XX this field should be kept at 0x3.
BLIE [4] - Battery Low interrupt enable. When 1, the Battery Low detection will generate an interrupt.
TIE [3] - Timer interrupt enable. When 1, the Countdown Timer will generate an IRQ signal and set the TIM flag when the timer reaches 0.
AIE [2] - Alarm interrupt enable. When 1, a match of all the enabled alarm registers will generate an IRQ signal.
EX2E [1] - when 1, the WDI input pin will generate the XT2 interrupt when the edge specified by EX2P occurs.
EX1E [0] - when 1, the EXTI input pin will generate the XT1 interrupt when the edge specified by EX1P occurs.

Table 19 - Interrupt Pulse Control

IM Value	Interrupt Pulse Width	
	32 kHz Oscillator	128 Hz Oscillator
00	Level	Level
01	1/8192 s	1/64 s
10	1/64 s	1/64 s
11	1/4 s	1/4 s

5.3.5 13 - SQW (Reset Value = 0x06)

This register holds the control signals for the square wave output. Note that some frequency selections are not valid if the 128 Hz RC Oscillator is selected.

SQWE [7] - When 1, the square wave output is enabled. When 0, the square wave output is held at the value of OUT.
SQFS [4:0] - selects the frequency of the square wave output, as shown in Table 20. Note that some selections are not valid if the 128 Hz oscillator is selected. Some selections also produce short pulses rather than square waves, and are intended primarily for test usage.

Table 20 – Square Wave Function Select

SQFS Value	SquareWave Output
00000	1 century (**)
00001	32 kHz (*)
00010	8 kHz (*)
00011	4 kHz (*)
00100	2 kHz (*)
00101	1 kHz (*)
00110	512 Hz (*) – Default value
00111	256 Hz (*)
01000	128 Hz
01001	64 Hz
01010	32 Hz
01011	16 Hz
01100	8 Hz
01101	4 Hz
01110	2 Hz
01111	1 Hz
10000	½ Hz
10001	¼ Hz
10010	1/8 Hz
10011	1/16 Hz
10100	1/32 Hz
10101	1/60 Hz (1 minute)
10110	16 kHz (*)
10111	100 Hz (*) (**)
11000	1 hour (**)
11001	1 day (**)
11010	TIRQ
11011	NOT TIRQ
11100	1 year (**)
11101	1 Hz to Counters (**)
11110	1/32 Hz from Acal (**)
11111	1/8K Hz from Acal (**)

(*) - NA if 128 Hz Oscillator selected
(**) - Pulses for Test Usage

5.4 Calibration Registers

5.4.1 14 - Calibration XT (Reset Value = Preconfigured)

This register holds the control signals for a digital calibration function of the XT Oscillator.

CMDX [7] - the calibration adjust mode. When 0 (Normal Mode), each adjustment step is +/- 2 ppm. When 1 (Coarse Mode), each adjustment step is +/- 4 ppm.
OFFSETX [6:0] - the amount to adjust the effective time. This is a two's complement number with a range of -64 to +63 adjustment steps.

5.4.2 15 - Calibration RC Upper (Reset Value = Preconfigured)

This register holds the control signals for the fine digital calibration function of the low power RC Oscillator.

CMDR [7:6] - the calibration adjust mode for the RC calibration adjustment. CMDR selects the highest frequency used in the RC Calibration process, as shown in Table 21.
OFFSETRU [5:0] - the upper 6 bits of the OFFSETR field, which is used to set the amount to adjust the effective time. OFFSETR is a two's complement number with a range of -2^13 to +2^13-1 adjustment steps.

Table 21 - CMDR Function

CMDR	Calibration Period	Minimum Adjustment	Maximum Adjustment
00	8,192 seconds	+/-1.91 ppm	+/-1.56%
01	4,096 seconds	+/-3.82 ppm	+/-3.13%
10	2,048 seconds	+/-7.64 ppm	+/-6.25%
11	1,024 seconds	+/-15.28 ppm	+/-12.5%

5.4.3 16 - Calibration RC Lower (Reset Value = Preconfigured)

This register holds the lower 8 bits of the OFFSETR field for the digital calibration function of the low power RC Oscillator.

OFFSETRL [7:0] - the lower 8 bits of OFFSETR.

5.5 Sleep Control Register

5.5.1 17 - Sleep Control (Reset Value = 0x00)

This register controls the Sleep function of the Power Control system.

SLP [7] - when 1, the Power Control SM will transition to the SWAIT state. This bit will be cleared when the SM returns to the RUN state. If either STOP is 1 or no interrupt is enabled, SLP will remain at 0 even after an attempt to set it to 1.
SLRES [6] - when 1, assert nRST low when the Power Control SM is in the SLEEP state.
EX2P [5] - when 1, the external interrupt XT2 will trigger on a rising edge of the WDI pin. When 0, the external interrupt XT2 will trigger on a falling edge of the WDI pin.
EX1P [4] - when 1, the external interrupt XT1 will trigger on a rising edge of the EXTI pin. When 0, the external interrupt XT1 will trigger on a falling edge of the EXTI pin.
SLST [3] - set when the AB18XX enters Sleep Mode. This allows software to determine if a SLEEP has occurred since the last time this bit was read.
SLTO [2:0] - the number of 7.8 ms periods after SLP is set until the Power Control SM goes into the SLEEP state. If SLTO is not 0, the actual delay is guaranteed to be between SLTO and (SLTO + 1) periods. If SLTO is 0, the transition will occur with no delay.

5.6 Timer Registers

5.6.1 18 - Countdown Timer Control (Reset Value = 0x23)

This register controls the Countdown Timer function. Note that the 00 frequency selection is slightly different depending on whether the 32 kHz XT Oscillator or the 128 Hz RC Oscillator is selected.

TE [7] - Timer Enable. When 1, the Countdown Timer will count down. When 0, the Countdown Timer retains the current value. If TE is 0, the clock to the Timer is disabled for power minimization.
TM [6] - Timer Interrupt Mode. Along with TRPT, this controls the Timer Interrupt function as shown in Table 23. A Level Interrupt will cause the nIRQ signal to be driven low by a Countdown Timer interrupt until the associated flag is cleared. A Pulse interrupt will cause the nIRQ signal to be driven low for the time shown in Table 23 or until the flag is cleared.
TRPT [5] – Along with TM, this controls the repeat function of the Countdown Timer. If Repeat is selected, the Countdown Timer reloads the value from the Timer_Initial register upon reaching 0, and continues counting. If Single is selected, the Countdown Timer will halt when it reaches zero. This allows the generation of periodic interrupts of virtually any frequency.
RPT [4:2] - these bits enable the Alarm Interrupt repeat function, as shown in Table 22. HA is the Hundredths_Alarm register value.
TFS [1:0] - select the clock frequency and interrupt pulse width of the Countdown Timer, as defined in Table 23. RCPLS is a 80-120 us pulse.

Table 22 - Repeat Function

RPT	HA	Repeat When
7	FF	Once per hundredth (*)
7	F[9-0]	Once per tenth (*)
7	[9-0][9-0]	Hundredths match (once per second)
6		Hundredths and seconds match (once per minute)
5		Hundredths, seconds and minutes match (once per hour)
4		Hundredths, seconds, minutes and hours match (once per day)
3		Hundredths, seconds, minutes, hours and weekday match (once per week)
2		Hundredths, seconds, minutes, hours and date match (once per month)
1		Hundredths, seconds, minutes, hours, date and month match (once per year)
0		Alarm Disabled

(*) – Once per second if 128 Hz Oscillator selected

Table 23 - Countdown Timer Function Select

TM	TRPT	TFS	Int	Repeat	Countdown Timer Frequency		Interrupt Pulse Width	
					32 kHz Oscillator	128 Hz Oscillator	32 kHz Oscillator	128 Hz Oscillator
0	0	00	Pulse	Single	4 kHz	128 Hz	1/4096 s	1/128 s
0	0	01	Pulse	Single	64 Hz	64 Hz	1/128 s	1/128 s
0	0	10	Pulse	Single	1 Hz	1 Hz	1/64 s	1/64 s
0	0	11	Pulse	Single	1/60 Hz	1/60 Hz	1/64 s	1/64 s
0	1	00	Pulse	Repeat	4 kHz	128 Hz	1/4096 s	1/128 s
0	1	01	Pulse	Repeat	64 Hz	64 Hz	1/128 s	1/128 s
0	1	10	Pulse	Repeat	1 Hz	1 Hz	1/64 s	1/64 s
0	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/64 s	1/64 s
1	0	00	Level	Single	4 kHz	128 Hz	N/A	N/A
1	0	01	Level	Single	64 Hz	64 Hz	N/A	N/A
1	0	10	Level	Single	1 Hz	1 Hz	N/A	N/A
1	0	11	Level	Single	1/60 Hz	1/60 Hz	N/A	N/A
1	1	00	Pulse	Repeat	4 kHz	128 Hz	1/4096 s	RCPLS
1	1	01	Pulse	Repeat	64 Hz	64 Hz	1/4096 s	RCPLS
1	1	10	Pulse	Repeat	1 Hz	1 Hz	1/4096 s	RCPLS
1	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/4096 s	RCPLS

5.6.2 19 - Countdown Timer (Reset Value = 0x00)

This register holds the current value of the Countdown Timer. It may be loaded with the desired starting value when the Countdown Timer is stopped.

5.6.3 1A - Timer Initial Value (Reset Value = 0x00)

This register holds the value which will be reloaded into the Countdown Timer when it reaches zero if the TRPT bit is a 1. This allows for periodic timer interrupts, and a period of (Timer_initial + 1) * (1/Countdown_frequency).

5.6.4 1B - Watchdog Timer (Reset Value = 0x00)

This register controls the Watchdog Timer function.

WDS [7] - Watchdog Steering. When 0, the Watchdog Timer will generate WIRQ when it times out. When 1, the Watchdog Timer will generate a reset when it times out.
BMB [6:2] - the number of clock cycles which must occur before the Watchdog Timer times out. A value of 00000 disables the Watchdog Timer function.
WRB [1:0] - the clock frequency of the Watchdog Timer, as shown in Table 24.

Table 24 - Watchdog Timer Frequency Select

WRB Value	Watchdog Timer Frequency
00	16 Hz
01	4 Hz
10	1 Hz
11	1/4 Hz

5.7 Oscillator Registers

5.7.1 1C - Oscillator Control (Reset Value = 0x00)

This register controls the overall Oscillator function. It may only be written if the Configuration Key register contains the value 0xA1. An Autocalibration cycle is initiated immediately whenever this register is written with a value in the ACAL field which is not zero.

OSEL [7] - When 1, request the RC Oscillator to generate a 128 Hz clock for the timer circuits. When 0, request the XT Oscillator to generate a 32 kHz clock to the timer circuit. Note that if the XT Oscillator is not operating, the oscillator switch will not occur. The OMODE field in the Oscillator Status register indicates the actual oscillator which is selected.
ACAL [6:5] – controls the automatic calibration function, as described in Table 14 (see Section 4.9).
AOS [4] - When 1, the oscillator will automatically switch to RC oscillator mode when the system is powered from the battery. When 0, no automatic switching occurs.
FOS [3] - When 1, the oscillator will automatically switch to RC oscillator mode when an oscillator failure is detected. When 0, no automatic switching occurs.
PWGT [2] - When 1, the I/O interface will be disabled when the power switch is active and disabled (PWR2 is a 1 and the OUT2 output is a 1).
OFIE [1] - Oscillator Fail interrupt enable. When 1, an Oscillator Failure will generate an IRQ signal.
ACIE [0] - When 1, an Autocalibration Failure will generate an interrupt.

5.7.2 1D – Oscillator Status Register (Reset Value = 0x00)

This register holds several miscellaneous bits used to control and observe the Oscillators.

XTCAL [7:6] – Extended Crystal Calibration. This field defines a value by which the Crystal Oscillator is adjusted to compensate for low capacitance crystals, independent of the normal Crystal Calibration function controlled by the Calibration XT Register. The frequency generated by the Crystal Oscillator is slowed by 122 ppm times the value in the XTCAL field (0, -122,-244 or -366 ppm).
LKO2 [5] – Lock OUT2. If this bit is a 1, the OUTB register bit (see Section 5.3.2) cannot be set to 1. This is typically used when OUT2 is configured as a power switch, and setting OUTB to a 1 would turn off the switch.
OMODE [4] (read only) – Oscillator Mode. This bit is a 1 if the RC Oscillator is selected to drive the internal clocks, and a 0 if the Crystal Oscillator is selected.
XTF [3] (read only) – Crystal Oscillator Not Operable. This bit is a 1 if the crystal oscillator is not switching, either because a failure has occurred to stop the oscillator or because it is disabled, for example if the AB08xx is currently operating from the RC oscillator.
OF [1] - Oscillator Failure. This bit is set on a power on reset, when both the system and battery voltages have dropped below acceptable levels. It is also set if an Oscillator Failure occurs, indicating that the crystal oscillator is running at less than 8 kHz.
ACF [0] - Set when an Autocalibration Failure occurs, indicating that either the RC Oscillator frequency is too different from 128 Hz to be correctly calibrated or the XT Oscillator did not start.

5.8 Miscellaneous Registers

5.8.1 1F - Configuration Key (Reset Value = 0x00)

This register contains the Configuration Key, which must be written with specific values in order to access some registers and functions. The Configuration Key is reset to 0x00 on any register write.

1) Writing a value of 0xA1 enables write access to the Oscillator Control register
2) Writing a value of 0x3C does not update the Configuration Key register, but generates a Software Reset (see Section 4.14).
3) Writing a value of 0x9D enables write access to the Trickle Register (0x20), the VREF Register (0x21) and the Output Control Register (0x30).

5.9 Analog Control Registers

5.9.1 20 -Trickle (Reset Value = 0x00)

This register controls the Trickle Charger. The Key Register must be written with the value 0x9D in order to enable access to this register.

TCS [7:4] - a value of 1010 enables the trickle charge function. All other values disable the Trickle Charger.
DIODE [3:2] - Diode Select. A value of 10 inserts a diode into the trickle charge circuit. A value of 01 does not insert a diode. Other values disable the Trickle Charger.
ROUT [1:0] - Output Resistor. This selects the output resistor of the trickle charge circuit, as shown in Table 25.

Table 25 - Trickle Charge Output Resistor

ROUT Value	Series Resistor
00	Disable
01	3 KΩ
10	6 KΩ
11	11 KΩ

5.9.2 21 - BREF Control (Reset Value = 0x00)

This register controls the reference voltages used in the Wakeup Control system. The Key Register must be written with the value 0x9D in order to enable access to this register.

BREF [7:4] - this selects the voltage reference which is compared to the battery voltage VBAT to produce the BBOD signal, as shown in Table 26. The voltage sensing circuitry includes hysteresis to insure that the system does not toggle between VBAT and VCC, and both rising and falling voltages are specified in the table. If the VBAT voltage is above the rising voltage which corresponds to the current BREF setting, BBOD will be set. At that point the VBAT voltage must fall below the falling voltage in order to clear the BBOD bit, set the BAT flag and generate a falling edge BL interrupt. If BBOD is clear, the VBAT voltage must rise above the rising voltage in order to clear the BBOD bit and generate a rising edge BL interrupt.

Table 26 - VBAT Reference Voltage

BREF Value	VBAT Falling Voltage (Nom)	VBAT Rising Voltage (Nom)
0000	1.2V	1.35V
0001	1.35V	1.5V
0010	1.5V	1.65V
0011	1.65V	1.8V
0100	1.8V	1.95V
0101	1.95V	2.1V
0110	2.1V	2.25V
0111	2.25V	2.4V
1000	2.4V	2.55V
1001	2.55V	2.7V
1010	2.7V	2.85V
1011	2.85V	3.0V
1100	3.0V	3.15V
1101	3.15V	3.3V
1110	3.3V	3.45V
1111	3.45V	3.7V

This register controls the Crystal Oscillator function. It may only be written if the Configuration Key register contains the value 0x9D. Note that bits 4:0 are initialized with the inverse of the NVMB value.

VREFVL [7:6] - the lower 2 bits of the 4 bit VREFV field which holds the voltage calibration value for the Voltage Reference Generator.
VREFT [5:0] – the temperature calibration value for the Voltage Reference Generator.

5.9.3 27 – Batmode IO Register (Reset Value = 0x80)

This register holds the IOBM bit which controls the enabling and disabling of the I/O interface when a Brownout Detection occurs. It may only be written if the Configuration Key register contains the value 0x9D. All undefined bits must be written with 0.

IOBM [7] – if 1, the AB18XX will not disable the I/O interface even if VCC goes away and VBAT is still present. This allows external access while the AB18XX is powered by VBAT.

5.9.4 2F – Analog Status Register (Read Only)

This register holds eight status bits which indicate the voltage levels of the VCC and VBAT power inputs.

BBOD [7] – if 1, the VBAT input voltage is above the BREF threshold.
BMIN [6] – if 1, the VBAT input voltage is above the minimum operating voltage (1.2 V).
VINIT [1] – if 1, the VCC input voltage is above the minimum power up voltage (1.6 V).

5.9.5 30 – Output Control Register

This register holds bits which control the behavior of the I/O pins under various power down conditions. The Key Register must be written with the value 0x9D in order to enable access to this register.

WDBM [7] – if 1, the WDI input is enabled when the AB18XX is powered from VBAT. If 0, the WDI input is disabled when the AB18XX is powered from VBAT.
EXBM [6] – if 1, the EXTI input is enabled when the AB18XX is powered from VBAT. If 0, the EXTI input is disabled when the AB18XX is powered from VBAT.
WDDS [5] – if 1, the WDI input is disabled when the AB18XX is in Sleep Mode. If 0, the WDI input is enabled when the AB18XX is in Sleep Mode If WDI is disabled, it will appear as a 1 to the internal logic.
EXDS [4] – if 1, the EXTI input is disabled when the AB18XX is in Sleep Mode. If 0, the EXTI input is enabled when the AB18XX is in Sleep Mode. If EXTI is disabled, it will appear as a 1 to the internal logic.
RSEN [3] – if 1, the nRST output is enabled when the AB18XX is in Sleep Mode. If 0, the nRST output is completely disconnected when the AB18XX is in Sleep Mode.
O4EN [2] – if 1, the CLKOUT/nIRQ3 output is enabled when the AB18XX is in Sleep Mode. If 0, the CLKOUT/nIRQ3 output is completely disconnected when the AB18XX is in Sleep Mode.
O3EN [1] – if 1, the nTIRQ output is enabled when the AB18XX is in Sleep Mode. If 0, the nTIRQ output is completely disconnected when the AB18XX is in Sleep Mode.
O1EN [0] – if 1, the FOUT/nIRQ output is enabled when the AB18XX is in Sleep Mode. If 0, the FOUT/nIRQ output is completely disconnected when the AB18XX is in Sleep Mode.

5.10 ID Registers

5.10.1 28 – ID0 - Part Number Upper Register (Read Only, Reset Value = 0x18)

This register holds the upper eight bits of the part number, which is always 0x18 for the AB18XX family.

5.10.2 29 – ID1 - Part Number Lower Register (Read Only, Reset Value = TBD)

This register holds the lower eight bits of the part number.

5.10.3 2A – ID2 - Part Revision (Read Only, Reset Value = 0x13)

This register holds the Revision number of the part.

MAJOR [7:3] – this field holds the major revision of the AB18XX.
MINOR [2:0] – this field holds the minor revision of the AB18XX.

5.10.4 2B – ID3 – Year/Week (Read Only, Reset Value = TBD)

This register holds part of the manufacturing information of the part.

YEAR [7:4] – this field holds the year the part was fabricated (0 = 2026, 1 = 2011, etc.).
WEEKL [3:0] – this field holds the lower 4 bits of the week the part was fabricated.

5.10.5 2C – ID4 – Wafer/Week (Read Only, Reset Value = TBD)

This register holds part of the manufacturing information of the part.

WAFER [7:2] – this field holds the wafer number.
WEEKU [1:0] – this field holds the upper 2 bits of the week the part was fabricated.

5.10.6 2D – ID5– Lot/Quadrant (Read Only, Reset Value = TBD)

This register holds part of the manufacturing information of the part.

LOT [7:6] – this field holds the lot number within a manufacturing week.
QUADRANT [5:0] – this field holds the quadrant of the wafer where this part was located.

5.10.7 2E – ID6– Serialization (Read Only, Reset Value = TBD)

SERIALIZATION [7:0] – this field holds a serialization value which may be combined with other fields to produce a unique value for each part.

5.11 RAM Registers

5.11.1 3F - Extension RAM Address (Reset Value = 0x00)

This register controls access to the Extension RAM, and includes some miscellaneous control bits.

O4BM [7] – if 1, the CLKOUT/nIRQ3 output is enabled when the AB18XX is powered from VBAT. If 0, the CLKOUT/nIRQ3 output is completely disconnected when the AB18XX is powered from VBAT.
BPOL [6] – BL Polarity. When 0, the Battery Low flag BL is set when the VBAT voltage goes below the BREF threshold. When 1, the Battery Low flag BL is set when the VBAT voltage goes above the BREF threshold.
WDIN [5] (read only) – this bit supplies the current level of the WDI pin.
EXIN [4] (read only) – this bit supplies the current level of the EXTI pin.
XEN [3] – Extended address enable. When 1, the XADA and XADS fields are used to generate the upper RAM address. When 0, the upper RAM address is forced to zero.
XADA [2] - this field supplies the upper bit for addresses to the Alternate RAM address space.
XADS [1:0] - this field supplies the upper two address bits for the Standard RAM address space.

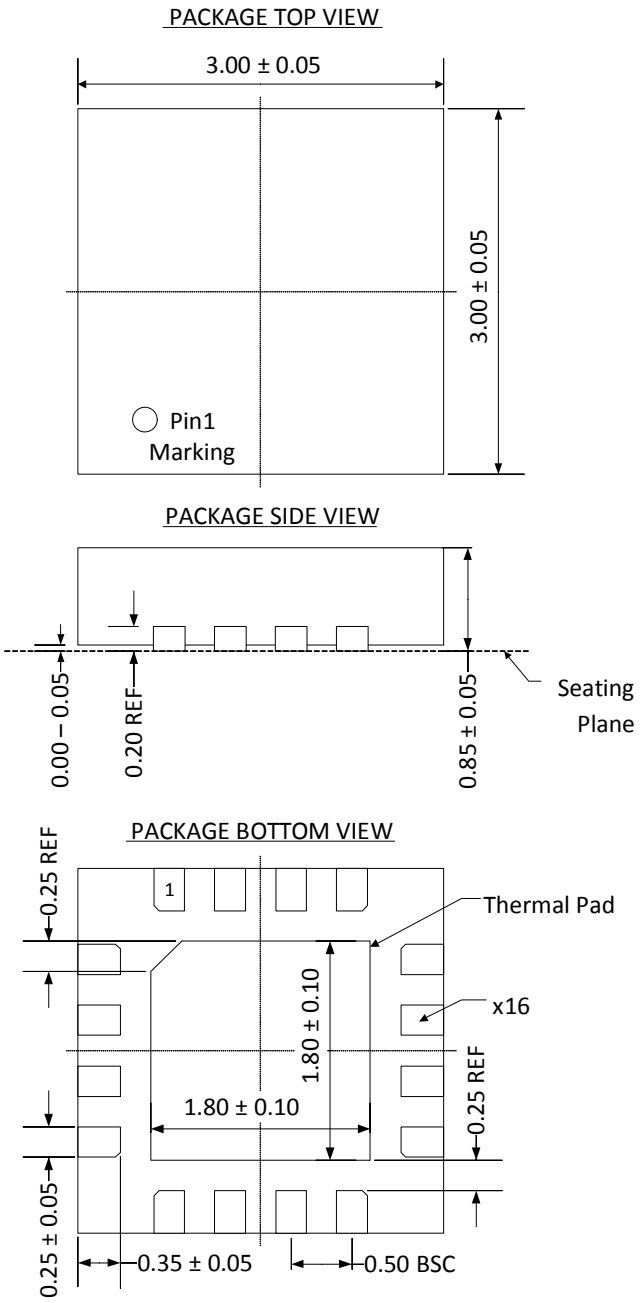
5.11.2 40 - 7F – Standard RAM (Reset Value = 0xXX)

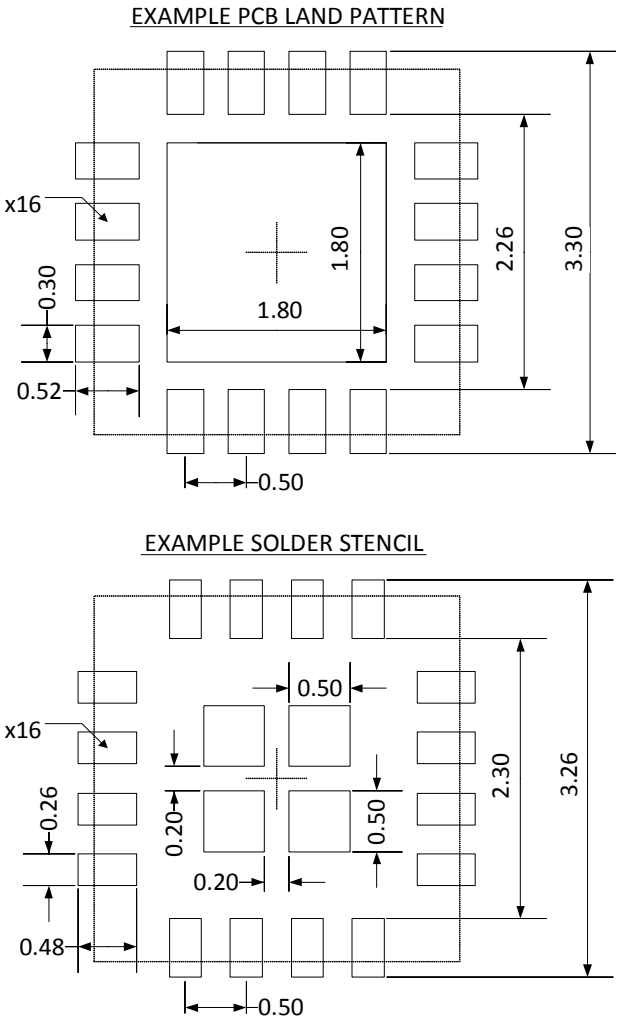
64 bytes of RAM space which may be accessed in either I^2C or SPI interface mode. The data in the RAM is held when using battery power. The upper 2 bits of the RAM address are taken from the XADS field, and the lower 6 bits are taken from the address offset, supporting a total RAM of 256 bytes.

5.11.3 80 - FF – Alternate RAM (Reset Value = 0xXX)

128 bytes of RAM which may be accessed only in I^2C interface mode. The data in the RAM is held when using battery power. The upper bit of the RAM address is taken from the XADA field, and the lower 7 bits are taken from the address offset, supporting a total RAM of 256 bytes.

6. Package Mechanical Information



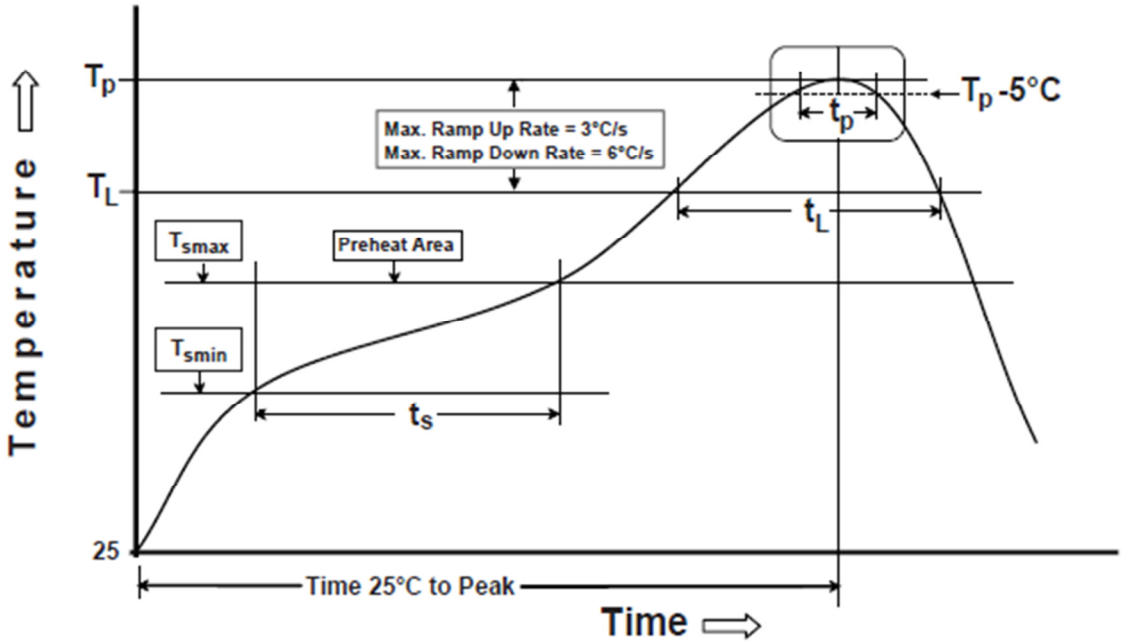


Drawing Notes:

1. All dimensions are in millimeters.
2. These drawings are subject to change without notice.
3. Quad Flat-pack, No-leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for connectivity and mechanical performance.
5. Customers should contact their board fabricator for minimum solder mask tolerances between signal pads.

7. Reflow Profile

The AB18XX reflow soldering requirements are described below.



Profile Feature	Requirement
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (ts) from (T_{smin} to T_{smax})	 150 ℃ 200 ℃ 60-120 seconds
Ramp-up rate (T_L to T_p)	3 ℃/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217 ℃ 60-150 seconds
Peak package body temperature (T_p)	260 ℃ max.
Time (t_p) within 5 ℃ of T_p	30 seconds max.
Ramp-down rate (T_p to T_L)	6 ℃/second max.
Time 25 ℃ to peak temperature	8 minutes max.

8. Ordering Information

AB18XX Orderable Part Numbers	Package	Operating Temperature Range	MSL Level[2]
AB1801-T3	Pb-Free[1] 16-Pin QFN 3 x 3 mm {3k units per reel}	-40°C to +85°C	1
AB1803-T3			
AB1804-T3			
AB1805-T3			
AB1811-T3			
AB1813-T3			
AB1814-T3			
AB1815-T3			

Notes:

[1] Compliant and certified with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in raw homogeneous materials. The package was designed to be soldered at high temperatures (per reflow profile) and can be used in specified lead-free processes.
[2] Moisture Sensitivity Level rating according to the JEDEC J-STD-020D industry standard classifications.

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