Micropower, RRIO, CMOS, 18 V Operational Amplifier

AD8546

FEATURES

Micropower at high voltage (18 V): 22 µA max
Low input bias current: 20 pA max
Gain bandwidth product: 200 kHz
Slew rate: 70 V/ms
Single-supply operation: 2.7 V to 18 V
Dual-supply operation: ±1.35 V to ±9 V
Unity-gain stable

APPLICATIONS

Portable medical equipment
Remote sensors
Transimpedance amplifiers
Current monitors
4 mA to 20 mA loop drivers
Buffer/level shifting

PIN CONFIGURATION

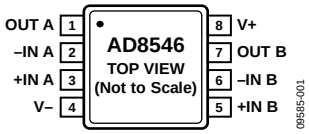

Figure 1. 8-Lead MSOP

GENERAL DESCRIPTION

The AD8546 is a dual, micropower, high input impedance amplifier optimized for low power and wide operating supply voltage range applications.

The AD8546 RRIO provides increased dynamic range to drive low frequency data converters, which is ideal for dc gain and buffering of sensor front ends or high impedance input sources in wireless or remote sensors or transmitters.

The AD8546 specification of low supply current (22 µA) over the wide range of operating voltage 2.7 V to 18 V or dual supplies (±1.35 V to ±9 V) makes it useful for a variety of battery-powered, portable applications such as ECGs, pulse monitors, glucose meters, smoke and fire detectors, vibration monitors, and backup battery sensors.

The AD8546 is specified over the extended industrial temperature range of −40°C to +125°C and is available in an 8-lead MSOP.

Table 1. Micropower Op Amps[1]

	Supply Voltage		
Amplifier	**5 V**	**12 V to 16 V**	**36 V**
Single	AD8500 ADA4505-1 AD8505 AD8541 AD8603	AD8663	
Dual	AD8502 ADA4505-2 AD8506 AD8542 AD8607	AD8667 AD8657 OP281	OP295 ADA4062-2
Quad	AD8504 ADA4505-4 AD8508 AD8544 AD8609	AD8669 OP481	OP495 ADA4062-4

[1] See www.analog.com for the latest selection of micropower op amps.

Rev. A

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REVISION HISTORY

4/11—Rev. 0 to Rev. A

Changes to Product Title, Features Section, Applications Section, General Description Section and Table 1 1

1/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

V_{SY} = 2.7 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 2.7 V			3	mV
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +85°C			4	mV
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +85°C			5	mV
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +125°C			4	mV
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +125°C			12.5	mV
Input Bias Current	I_B			1	10	pA
		−40°C ≤ T_A ≤ +125°C			2.6	nA
Input Offset Current	I_{OS}				20	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	60	75		dB
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +85°C	59			dB
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +85°C	57			dB
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +125°C	58			dB
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +125°C	49			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ; V_O = 0.5 V to 2.2 V	92	105		dB
		−40°C ≤ T_A ≤ +85°C	75			dB
		−40°C ≤ T_A ≤ +125°C	65			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			3.5		pF
Common Mode	C_{INCM}			3.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	2.69			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			10	mV
Short-Circuit Current	I_{SC}			±4		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz; A_V = +1		20		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	90	120		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	µA
		−40°C ≤ T_A ≤ +125°C			33	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		38		V/ms
Settling Time to 0.1%	t_S	V_{IN} = 1 V step; R_L = 100 kΩ; C_L = 10 pF		14		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		170		kHz
Phase Margin	Φ_M	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		69		Degrees
Channel Separation	CS	f = 10 kHz; R_L = 1 MΩ		105		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		56		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—10 V OPERATION

V_{SY} = 10 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 10 V			3	mV
		V_{CM} = 0.3 V to 9.7 V; −40°C ≤ T_A ≤ +85°C			4.2	mV
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +85°C			5	mV
		V_{CM} = 0.3 V to 9.7 V; −40°C ≤ T_A ≤ +125°C			8.5	mV
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C			12.5	mV
Input Bias Current	I_B			2	15	pA
		−40°C ≤ T_A ≤ +125°C			2.6	nA
Input Offset Current	I_{OS}				30	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 10 V	70	88		dB
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +85°C	70			dB
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ; V_O = 0.5 V to 9.5 V	95	115		dB
		−40°C ≤ T_A ≤ +85°C	90			dB
		−40°C ≤ T_A ≤ +125°C	67			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		μV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			3.5		pF
Common Mode	C_{INCM}			3.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	9.98			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			20	mV
Short-Circuit Current	I_{SC}			±11		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz; A_V = +1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	90	120		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	μA
		−40°C ≤ T_A ≤ +125°C			33	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		60		V/ms
Settling Time to 0.1%	t_S	V_{IN} = 1 V step; R_L = 100 kΩ; C_L = 10 pF		13		μs
Gain Bandwidth Product	GBP	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		200		kHz
Phase Margin	Φ_M	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		60		Degrees
Channel Separation	CS	f = 10 kHz; R_L = 1 MΩ		105		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		5		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—18 V OPERATION

V_{SY} = 18 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 18 V			3	mV
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +85°C			4.5	mV
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +85°C			5	mV
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +125°C			11	mV
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C			14	mV
Input Bias Current	I_B			5	20	pA
		−40°C ≤ T_A ≤ +125°C			2.9	nA
Input Offset Current	I_{OS}				40	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 18 V	80	95		dB
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +85°C	77			dB
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +85°C	72			dB
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +125°C	65			dB
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C	63			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ; V_O = 0.5 V to 17.5 V	88	100		dB
		−40°C ≤ T_A ≤ +85°C	82			dB
		−40°C ≤ T_A ≤ +125°C	73			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			3.5		pF
Common Mode	C_{INCM}			10.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	17.97			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			30	mV
Short-Circuit Current	I_{SC}			±12		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz; A_V = +1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	90	120		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	µA
		−40°C ≤ T_A ≤ +125°C			33	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		70		V/ms
Settling Time to 0.1%	t_S	V_{IN} = 1 V step; R_L = 100 kΩ; C_L = 10 pF		12		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		200		kHz
Phase Margin	Φ_M	R_L = 1 MΩ; C_L = 10 pF; A_V = +1		60		Degrees
Channel Separation	CS	f = 10 kHz; R_L = 1 MΩ		105		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage	(V–) − 300 mV to (V+) + 300 mV
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

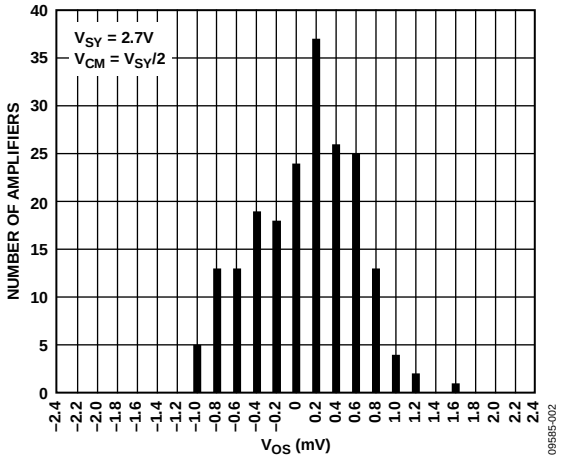


Figure 2. Input Offset Voltage Distribution

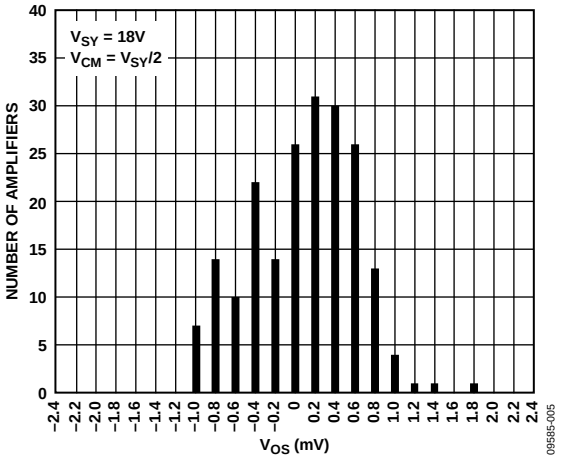


Figure 5. Input Offset Voltage Distribution

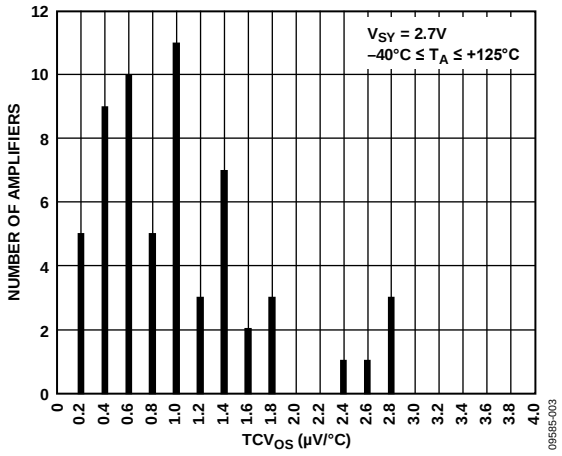


Figure 3. Input Offset Voltage Drift Distribution

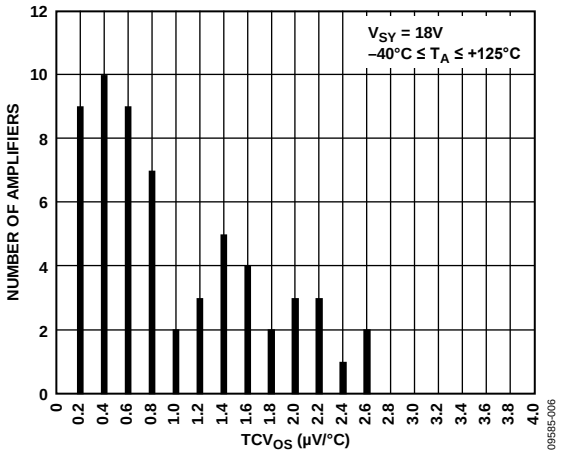


Figure 6. Input Offset Voltage Drift Distribution

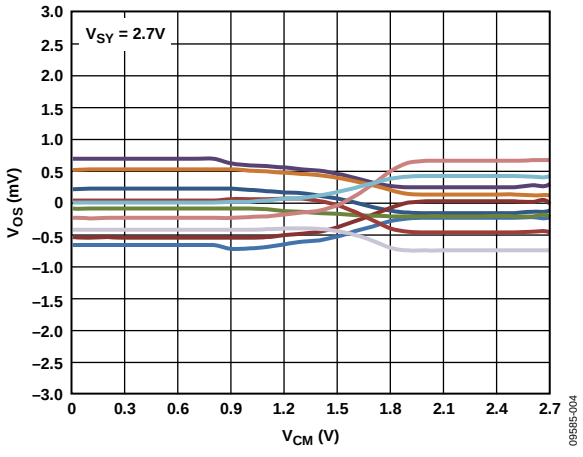


Figure 4. Input Offset Voltage vs. Common-Mode Voltage

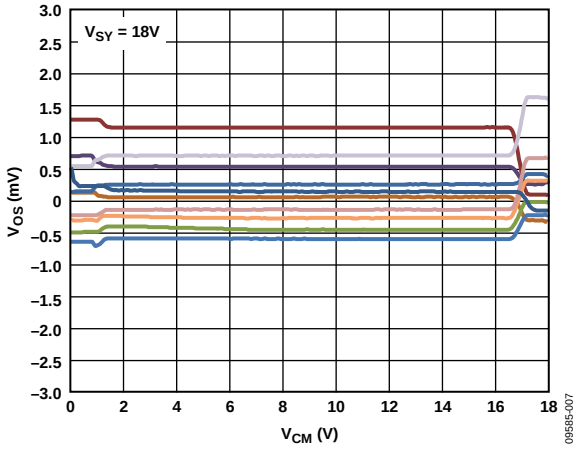


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

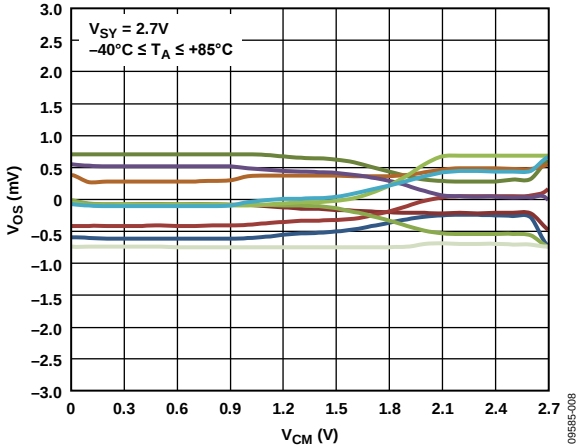


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

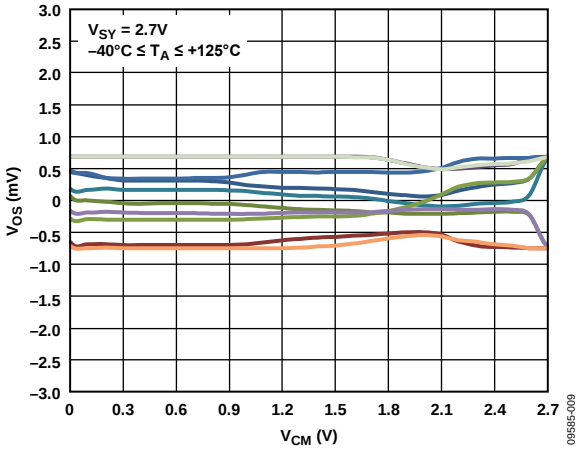


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

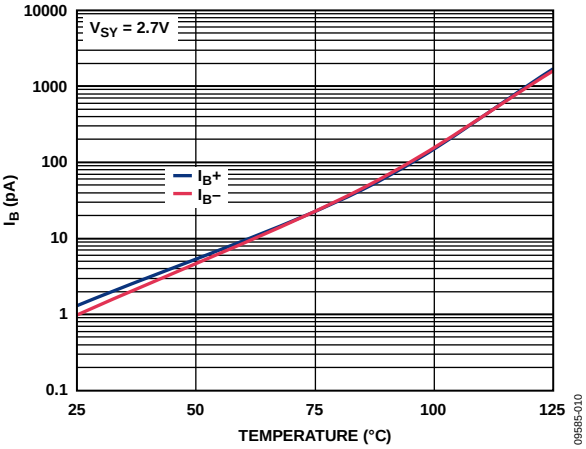


Figure 10. Input Bias Current vs. Temperature

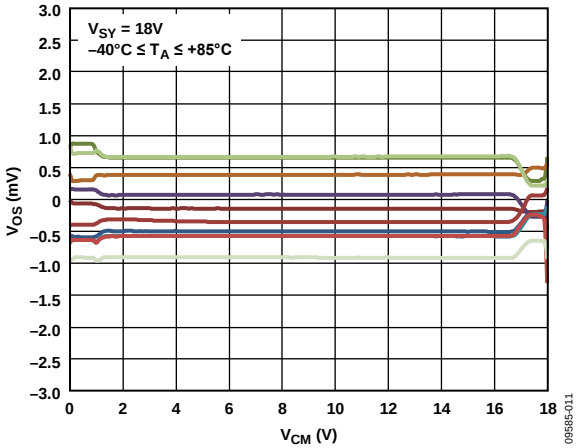


Figure 11. Input Offset Voltage vs. Common-Mode Voltage

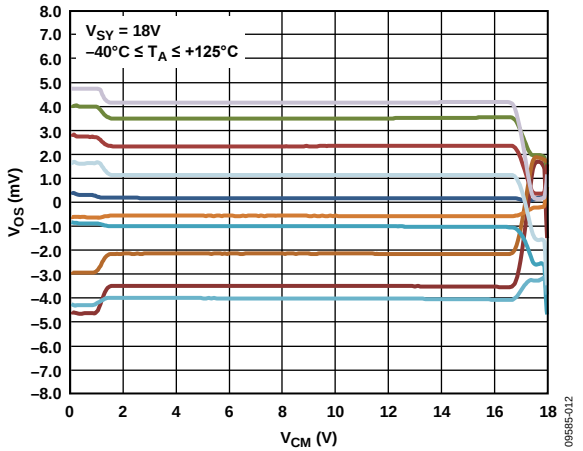


Figure 12. Input Offset Voltage vs. Common-Mode Voltage

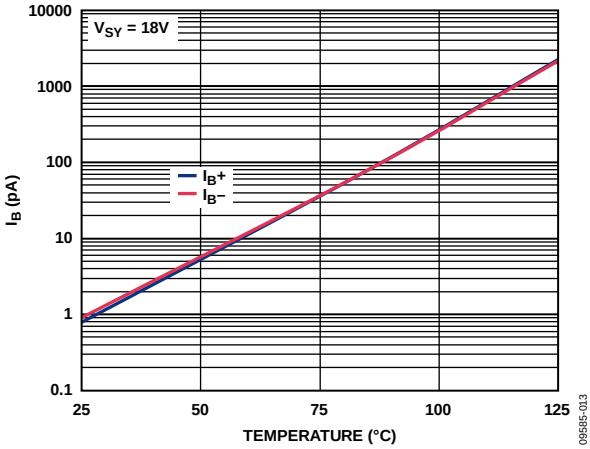


Figure 13. Input Bias Current vs. Temperature

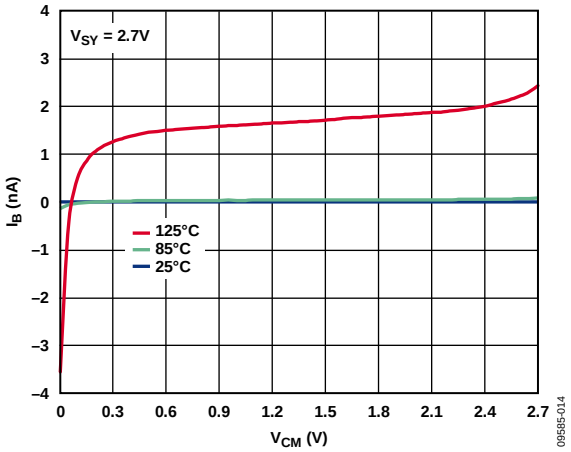


Figure 14. Input Bias Current vs. Common-Mode Voltage

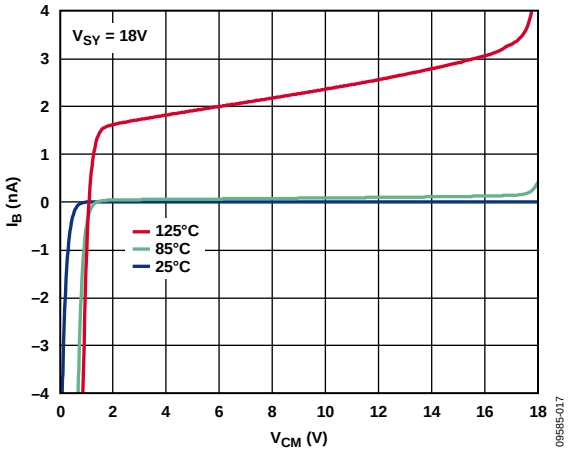


Figure 17. Input Bias Current vs. Common-Mode Voltage

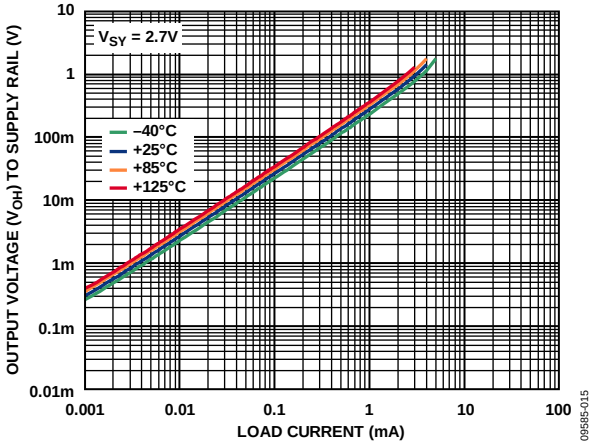


Figure 15. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

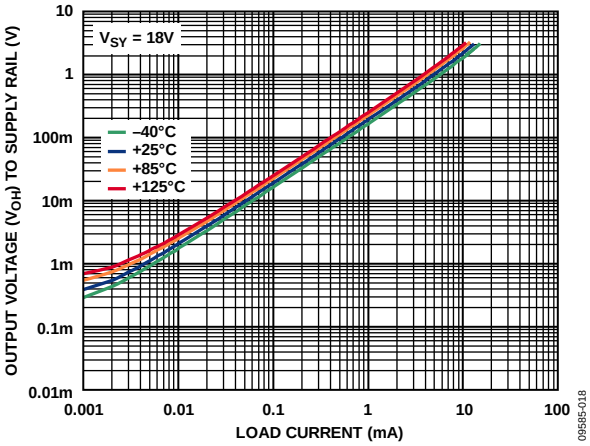


Figure 18. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

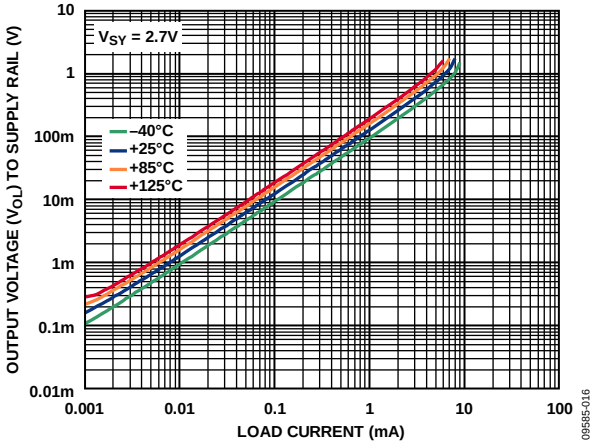


Figure 16. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

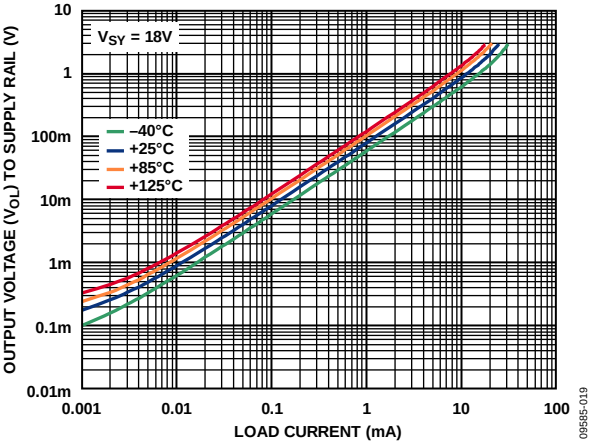


Figure 19. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

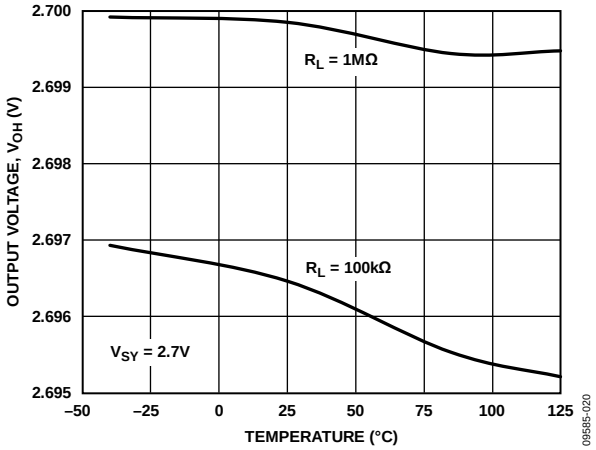


Figure 20. Output Voltage (V_{OH}) vs. Temperature

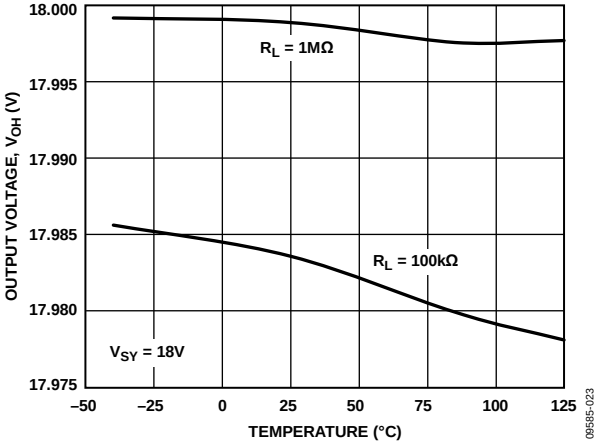


Figure 23. Output Voltage (V_{OH}) vs. Temperature

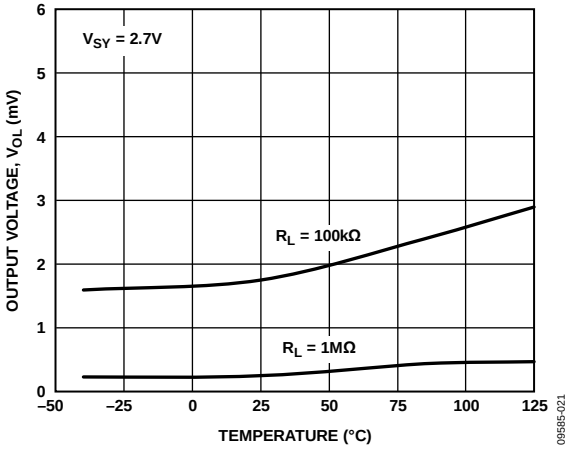


Figure 21. Output Voltage (V_{OL}) vs. Temperature

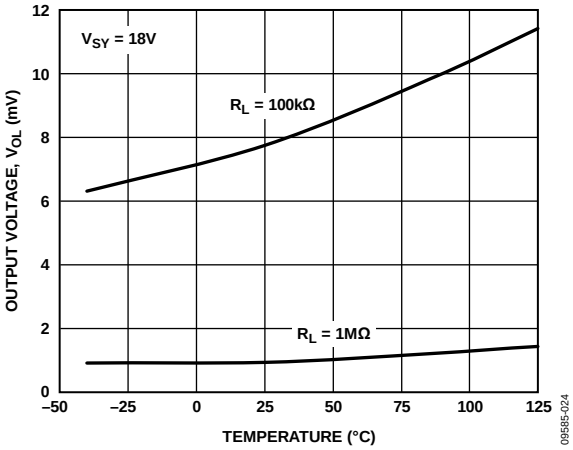


Figure 24. Output Voltage (V_{OL}) vs. Temperature

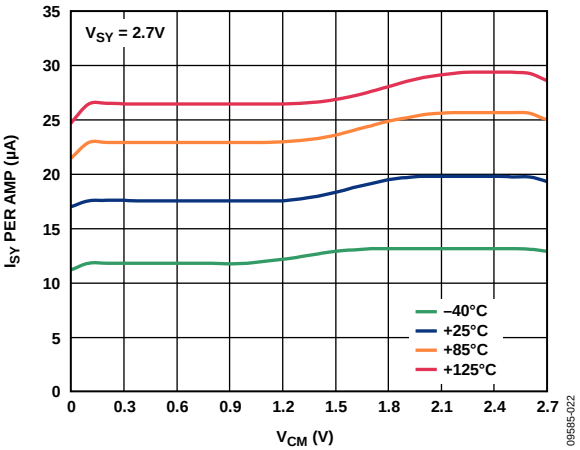


Figure 22. Supply Current per Amplifier vs. Common-Mode Voltage

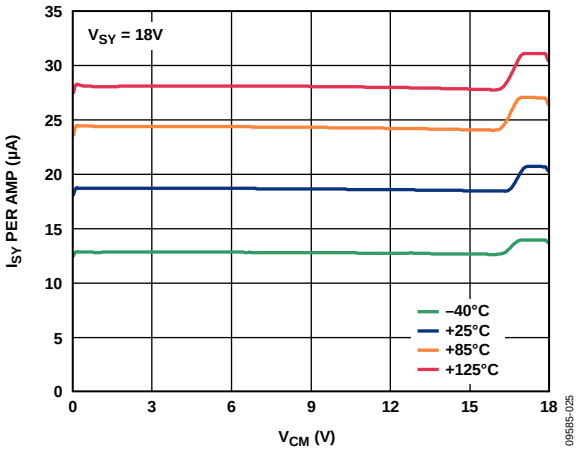


Figure 25. Supply Current per Amplifier vs. Common-Mode Voltage

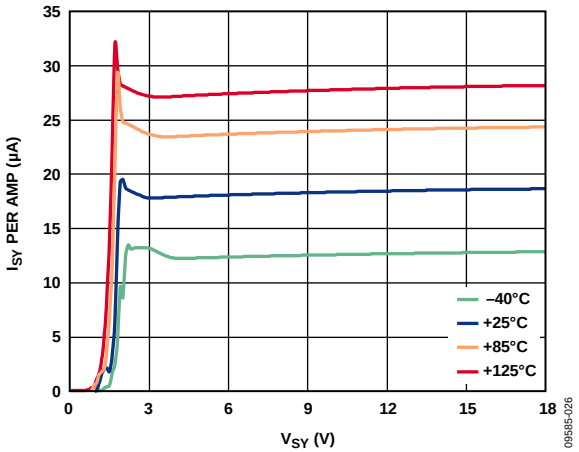


Figure 26. Supply Current per Amplifier vs. Supply Voltage

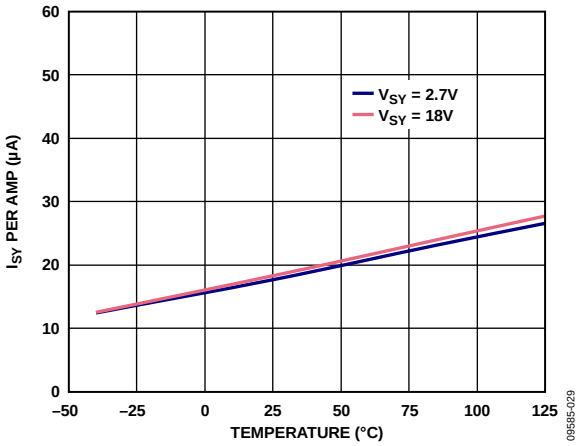


Figure 29. Supply Current per Amplifier vs. Temperature

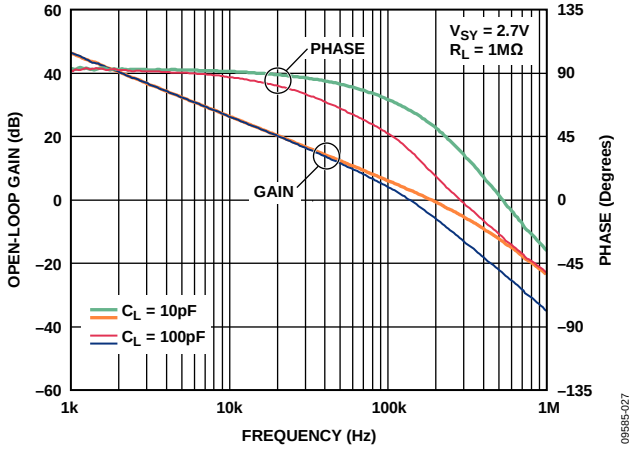


Figure 27. Open-Loop Gain and Phase vs. Frequency

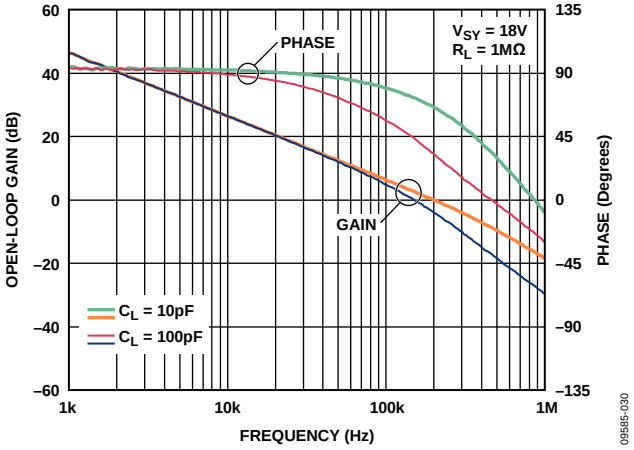


Figure 30. Open-Loop Gain and Phase vs. Frequency

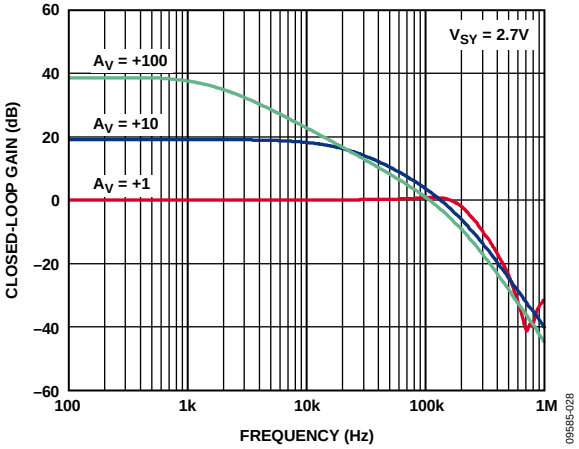


Figure 28. Closed-Loop Gain vs. Frequency

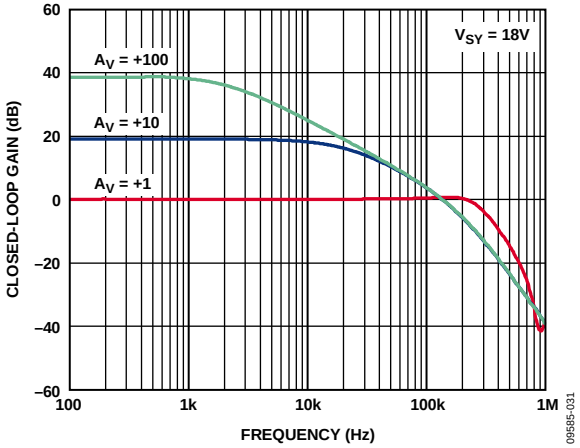


Figure 31. Closed-Loop Gain vs. Frequency

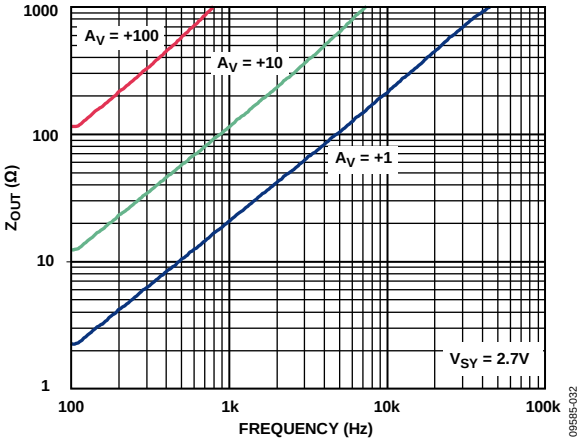


Figure 32. Output Impedance vs. Frequency

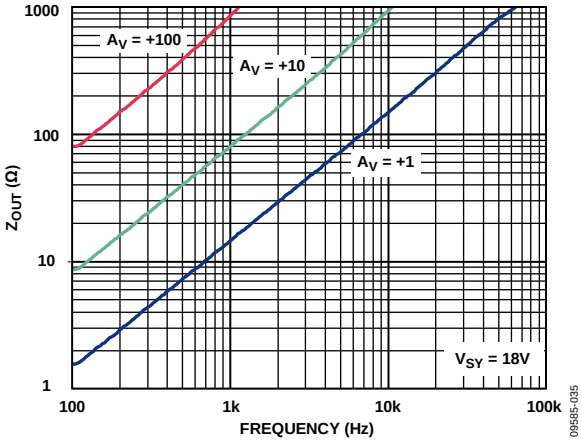


Figure 35. Output Impedance vs. Frequency

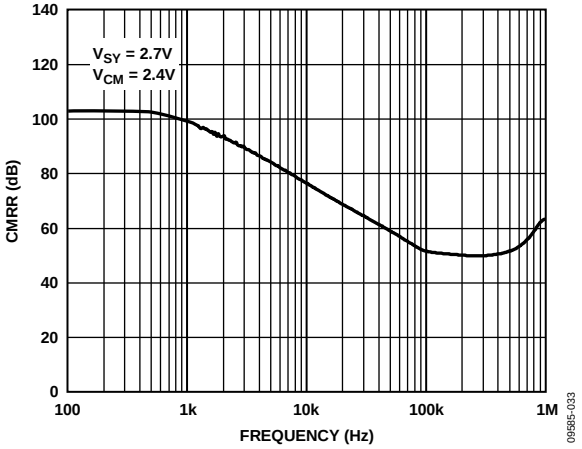


Figure 33. CMRR vs. Frequency

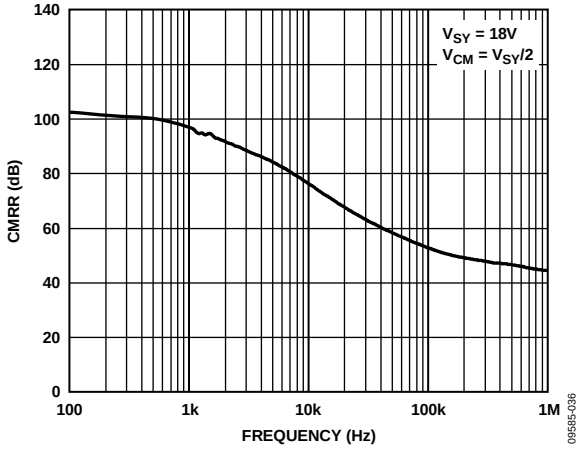


Figure 36. CMRR vs. Frequency

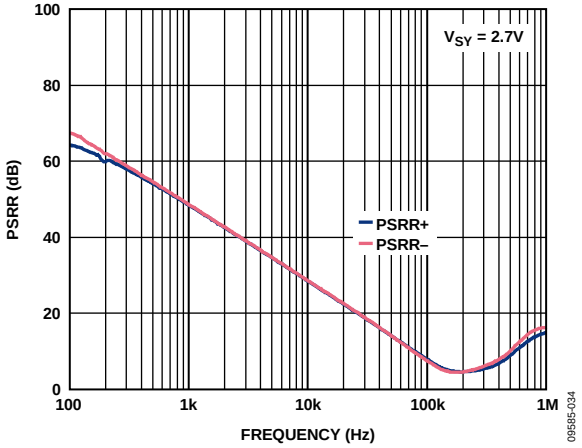


Figure 34. PSRR vs. Frequency

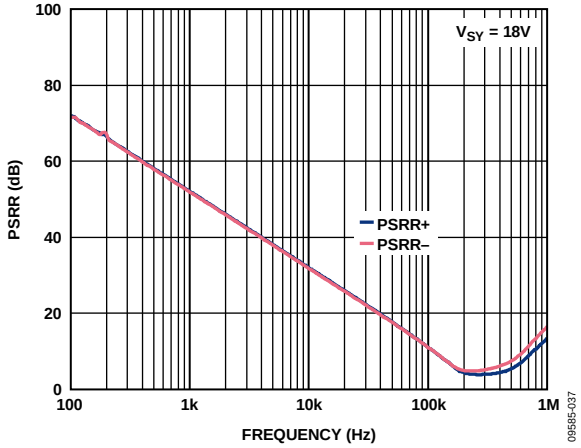


Figure 37. PSRR vs. Frequency

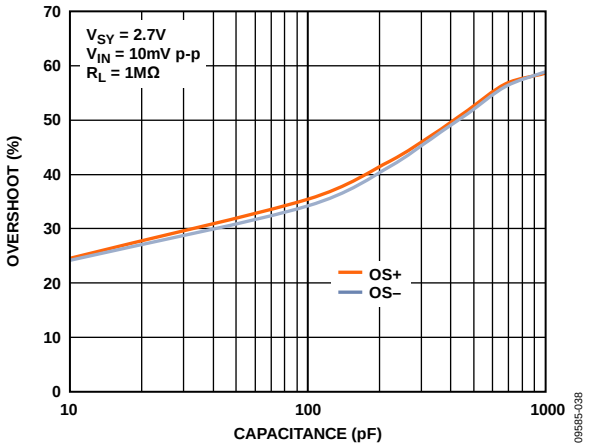


Figure 38. Small Signal Overshoot vs. Load Capacitance

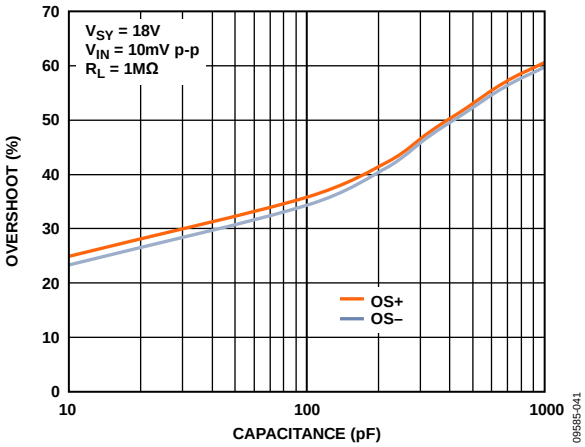


Figure 41. Small Signal Overshoot vs. Load Capacitance

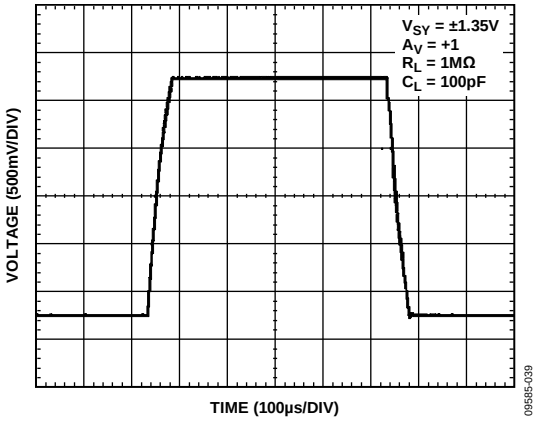


Figure 39. Large Signal Transient Response

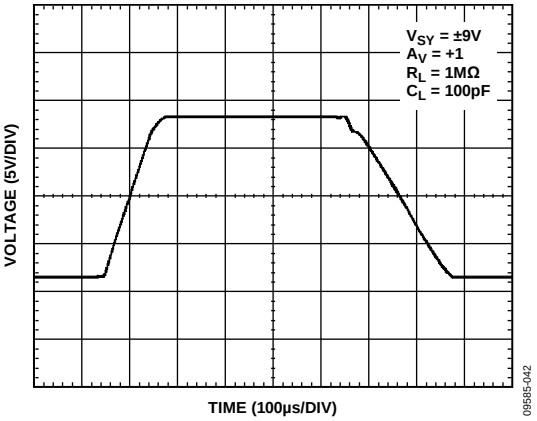


Figure 42. Large Signal Transient Response

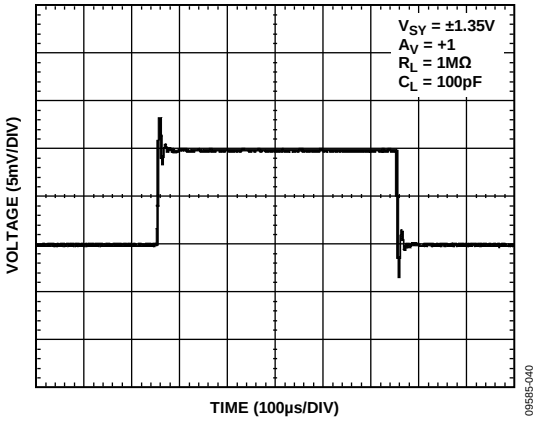


Figure 40. Small Signal Transient Response

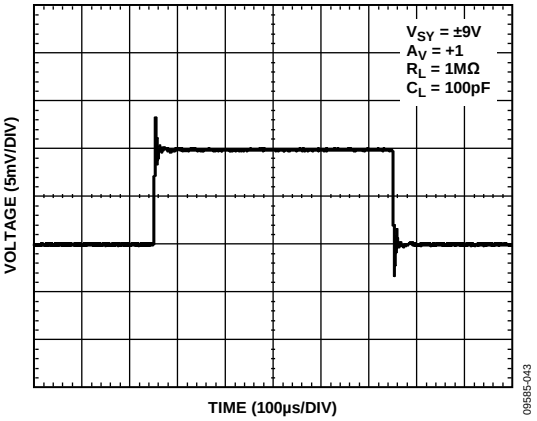


Figure 43. Small Signal Transient Response

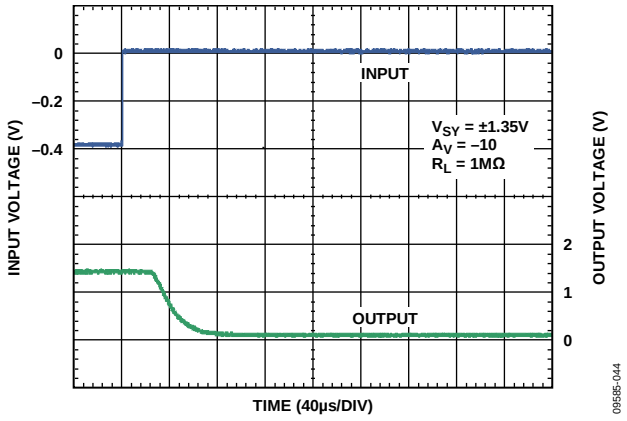


Figure 44. Positive Overload Recovery

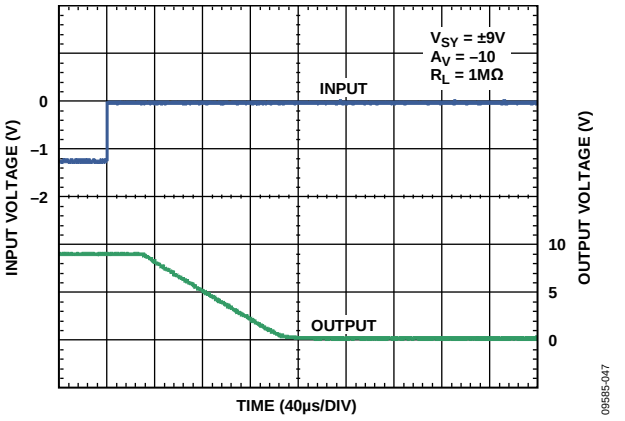


Figure 47. Positive Overload Recovery

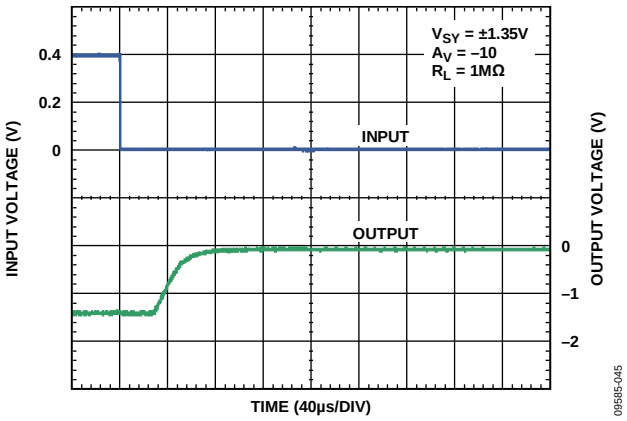


Figure 45. Negative Overload Recovery

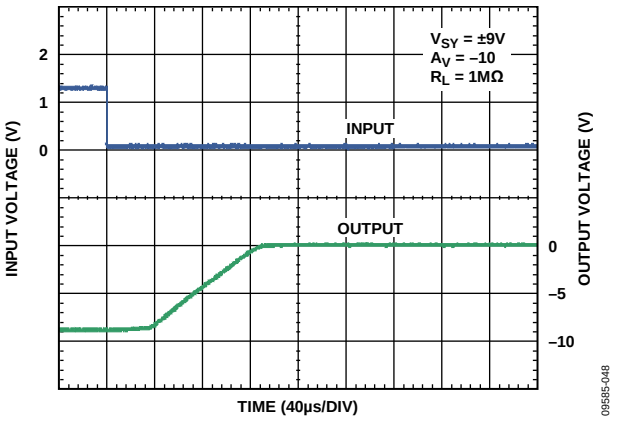


Figure 48. Negative Overload Recovery

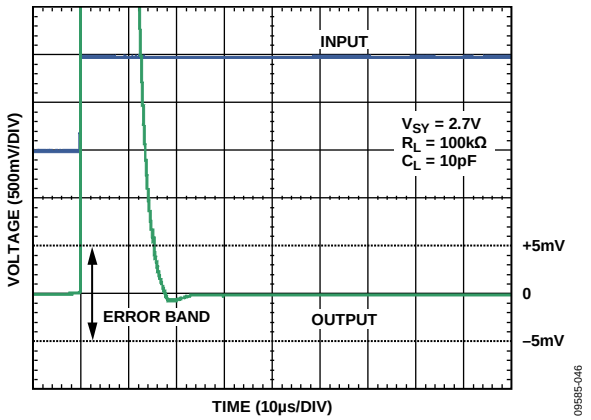


Figure 46. Positive Settling Time to 0.1%

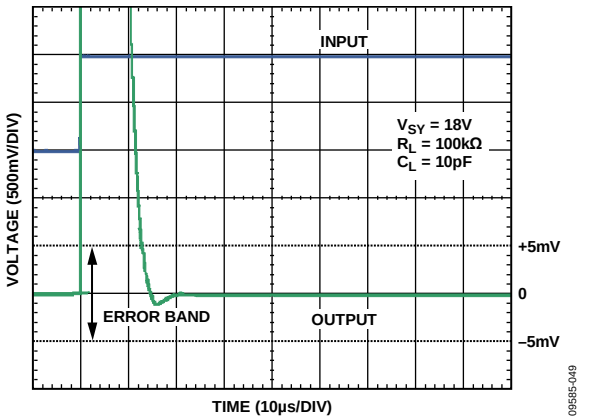


Figure 49. Positive Settling Time to 0.1%

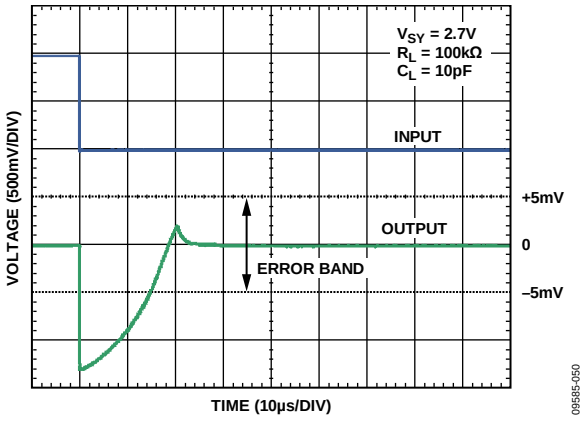


Figure 50. Negative Settling Time to 0.1%

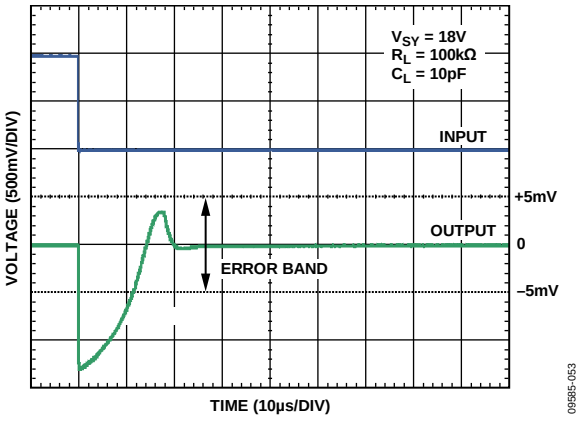


Figure 53. Negative Settling Time to 0.1%

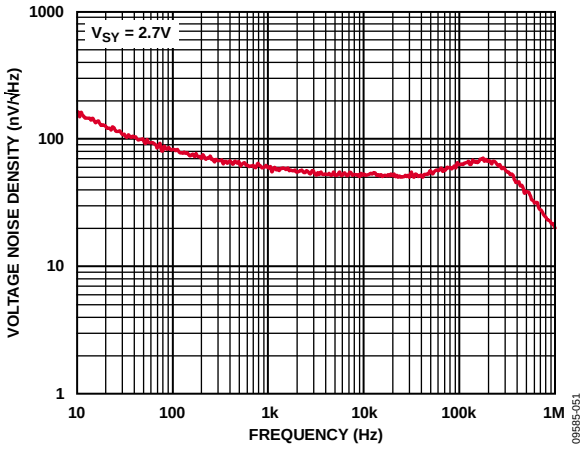


Figure 51. Voltage Noise Density vs. Frequency

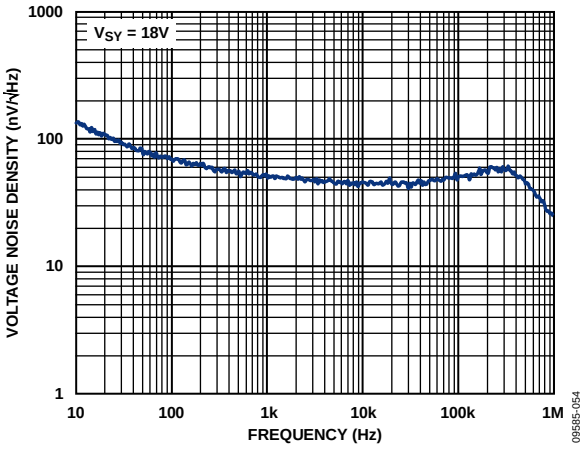


Figure 54. Voltage Noise Density vs. Frequency

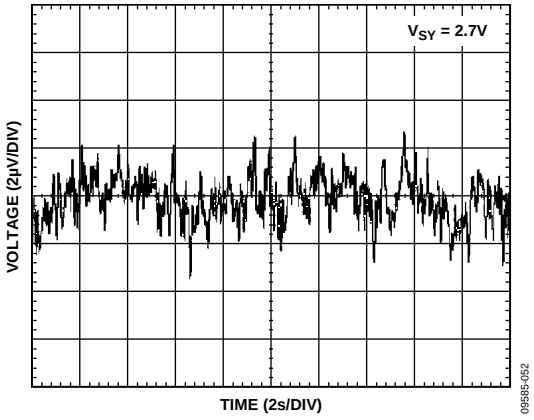


Figure 52. 0.1 Hz to 10 Hz Noise

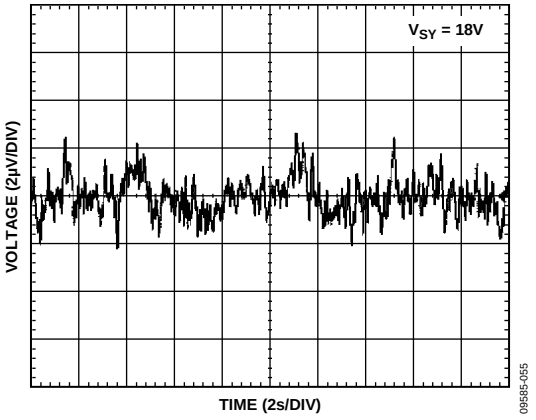


Figure 55. 0.1 Hz to 10 Hz Noise

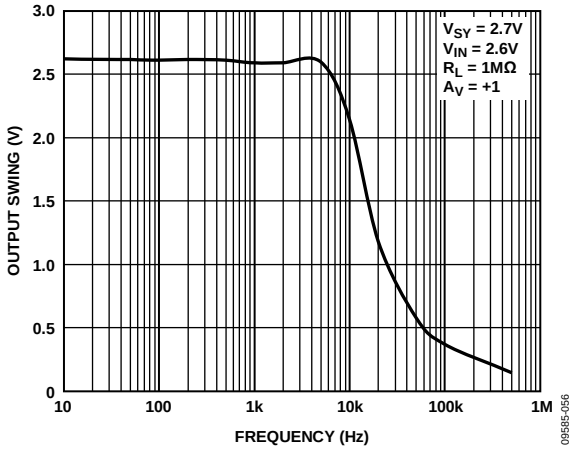


Figure 56. Output Swing vs. Frequency

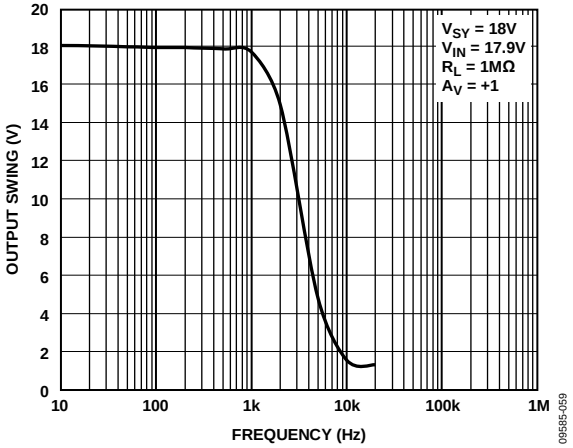


Figure 59. Output Swing vs. Frequency

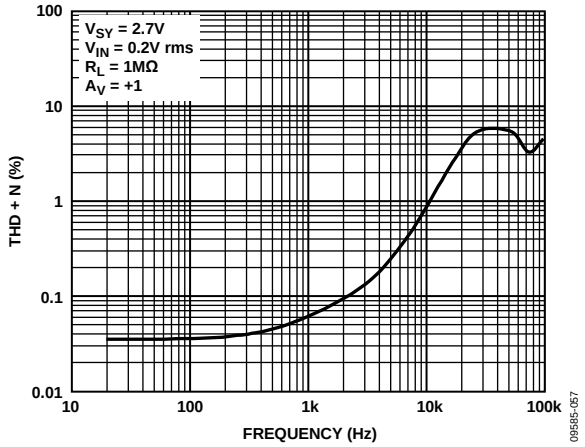


Figure 57. THD + N vs. Frequency

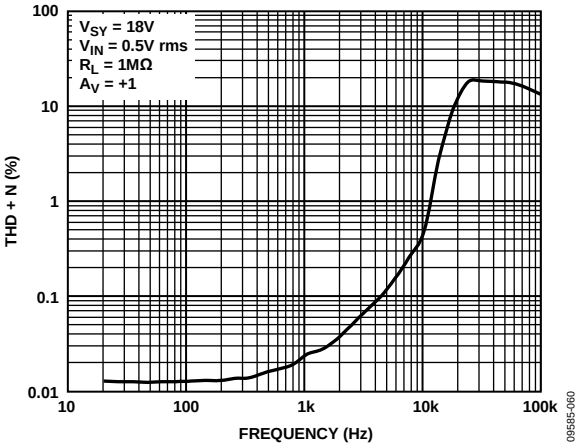


Figure 60. THD + N vs. Frequency

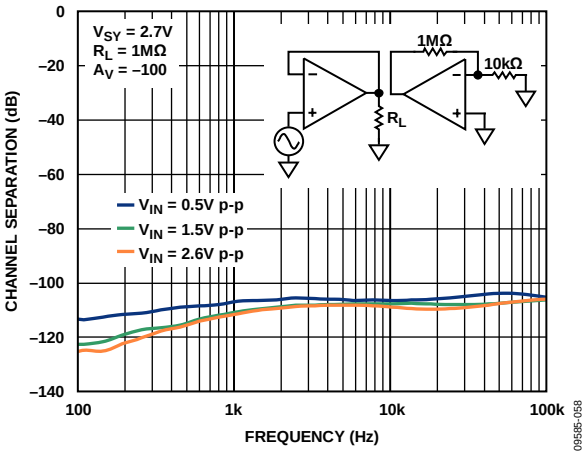


Figure 58. Channel Separation vs. Frequency

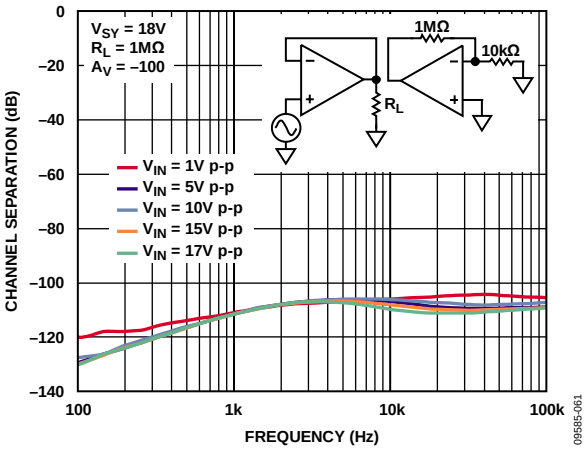


Figure 61. Channel Separation vs. Frequency

APPLICATIONS INFORMATION

The AD8546 is a low input bias current, micropower CMOS amplifier that operates over a wide supply voltage range of 2.7 V to 18 V. The AD8546 also employs unique input and output stages to achieve a rail-to-rail input and output range with a very low supply current.

INPUT STAGE

Figure 62 shows the simplified schematic of the AD8546. The input stage comprises two differential transistor pairs, an NMOS pair (M1, M2) and a PMOS pair (M3, M4). The input common-mode voltage determines which differential pair turns on and is more active than the other.

The PMOS differential pair is active when the input voltage approaches and reaches the lower supply rail. The NMOS pair is needed for input voltages up to and including the upper supply rail. This topology allows the amplifier to maintain a wide dynamic input voltage range and maximize signal swing to both supply rails.

For the majority of the input common-mode voltage range, the PMOS differential pair is active. Differential pairs commonly exhibit different offset voltages. The handoff from one pair to the other creates a step-like characteristic that is visible in the V_{OS} vs. V_{CM} graphs (see Figure 4 and Figure 7). This characteristic is inherent in all rail-to-rail amplifiers that use the dual differential pair topology. Therefore, always choose a common-mode voltage that does not include the region of handoff from one input differential pair to the other.

Additional steps in the V_{OS} vs. V_{CM} curves are also visible as the input common-mode voltage approaches the power supply rails. These changes are a result of the load transistors (M8, M9, M14, and M15) running out of headroom. As the load transistors are forced into the triode region of operation, the mismatch of their drain impedances contributes to the offset voltage of the amplifier. This problem is exacerbated at high temperatures due to the decrease in the threshold voltage of the input transistors. Refer to Figure 8, Figure 9, Figure 11, and Figure 12 for typical performance data.

Current Source I1 drives the PMOS transistor pair. As the input common-mode voltage approaches the upper rail, I1 is steered away from the PMOS differential pair through the M5 transistor. The bias voltage, VB1, controls the point where this transfer occurs.

M5 diverts the tail current into a current mirror consisting of the M6 and M7 transistors. The output of the current mirror then drives the NMOS transistor pair. Note that the activation of this current mirror causes a slight increase in supply current at high common-mode voltages (see Figure 22 and Figure 25).

The AD8546 achieves its high performance by using low voltage MOS devices for its differential inputs. These low voltage MOS devices offer excellent noise and bandwidth per unit of current. Each differential input pair is protected by proprietary regulation circuitry (not shown in the simplified schematic). The regulation circuitry consists of a combination of active devices that maintain the proper voltages across the input pairs during normal operation and passive clamping devices that protect the amplifier during fast transients. However, these passive clamping devices begin to forward-bias as the common-mode voltage approaches either power supply rail. This causes an increase in the input bias current (see Figure 14 and Figure 17).

The input devices are also protected from large differential input voltages by clamp diodes (D1 and D2). These diodes are buffered from the inputs with two 10 k Ω resistors (R1 and R2). The differential diodes turn on whenever the differential voltage exceeds approximately 600 mV; in this condition, the differential input resistance drops to 20 kΩ.

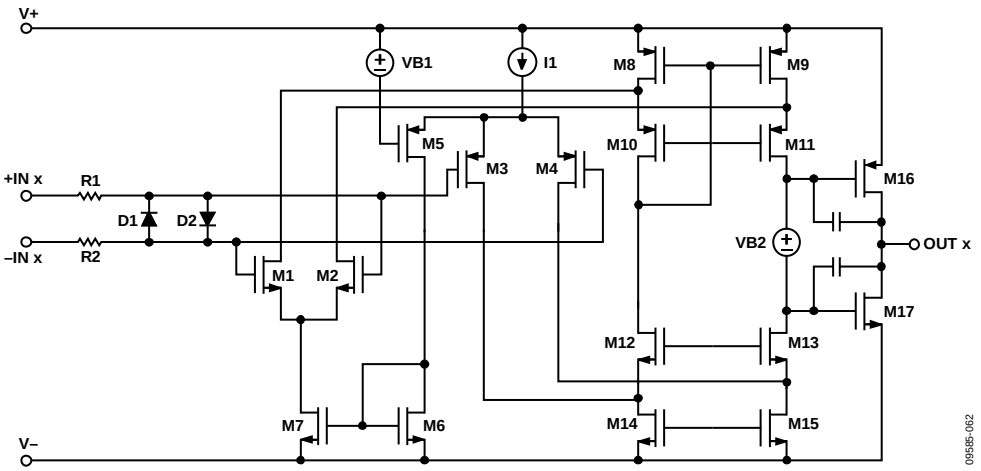


Figure 62. Simplified Schematic

OUTPUT STAGE

The AD8546 features a complementary output stage consisting of the M16 and M17 transistors (see Figure 62). These transistors are configured in Class AB topology and are biased by the voltage source, VB2. This topology allows the output voltage to go within millivolts of the supply rails, achieving a rail-to-rail output swing. The output voltage is limited by the output impedance of the transistors, which are low R_{ON} MOS devices. The output voltage swing is a function of the load current and can be estimated using the output voltage to supply rail vs. load current diagrams (see Figure 15, Figure 16, Figure 18, and Figure 19).

RAIL-TO-RAIL INPUT AND OUTPUT

The AD8546 features rail-to-rail input and output with a supply voltage from 2.7 V to 18 V. Figure 63 shows the input and output waveforms of the AD8546 configured as a unity-gain buffer with a supply voltage of ±9 V and a resistive load of 1 MΩ. With an input voltage of ±9 V, the AD8546 allows the output to swing very close to both rails. Additionally, it does not exhibit phase reversal.

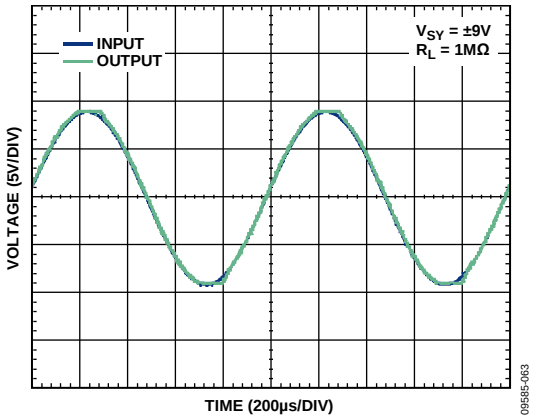


Figure 63. Rail-to-Rail Input and Output

RESISTIVE LOAD

The feedback resistor alters the load resistance that an amplifier sees. It is, therefore, important to be aware of the value of the feedback resistors selected for use with the AD8546. The AD8546 is capable of driving resistive loads down to 100 k Ω. The following two examples, inverting and noninverting configurations, show how the feedback resistor changes the actual load resistance seen at the output of the amplifier.

Inverting Configuration

Figure 64 shows the AD8546 in an inverting configuration with a resistive load, R_L, at the output. The actual load seen by the amplifier is the parallel combination of the feedback resistor, R2, and the load, R_L. The combination of a feedback resistor of 1 kΩ and a load of 1 MΩ results in an equivalent load resistance of 999 Ω at the output. In this condition, the AD8546 is incapable of driving such a heavy load; therefore, its performance degrades greatly.

To avoid loading the output, use a larger feedback resistor, but consider the effect of resistor thermal noise on the overall circuit.

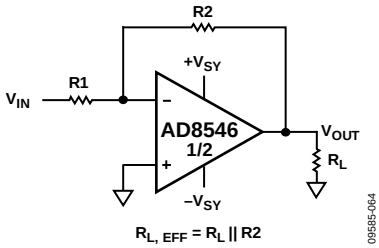


Figure 64. Inverting Op Amp Configuration

Noninverting Configuration

Figure 65 shows the AD8546 in a noninverting configuration with a resistive load, R_L, at the output. The actual load seen by the amplifier is the parallel combination of R1 + R2 and R_L.

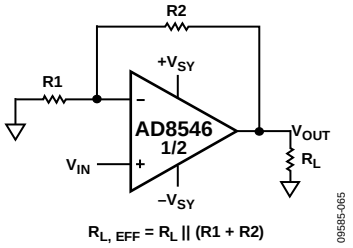


Figure 65. Noninverting Op Amp Configuration

COMPARATOR OPERATION

An op amp is designed to operate in a closed-loop configuration with feedback from its output to its inverting input. Figure 66 shows the AD8546 configured as a voltage follower with an input voltage that is always kept at midpoint of the power supplies. The same configuration is applied to the unused channel. A1 and A2 indicate the placement of ammeters to measure supply current. I_{SY}+ refers to the current flowing from the upper supply rail to the op amp, and I_{SY}– refers to the current flowing from the op amp to the lower supply rail. As expected, Figure 67 shows that in normal operating condition, the total current flowing into the op amp is equivalent to the total current flowing out of the op amp, where I_{SY}+ = I_{SY}– = 36 µA for the dual AD8546 at V_{SY} = 18 V.

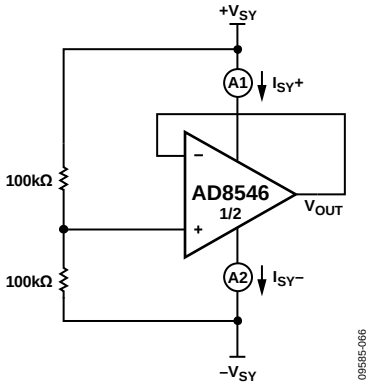


Figure 66. Voltage Follower Configuration

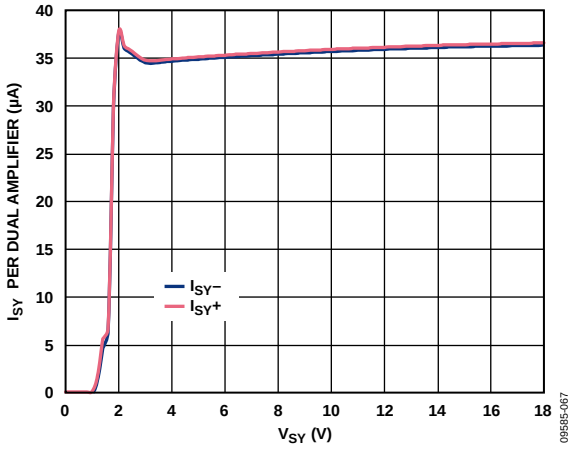


Figure 67. Supply Current vs. Supply Voltage (Voltage Follower)

In contrast to op amps, comparators are designed to work in an open-loop configuration and to drive logic circuits. Although op amps are different from comparators, occasionally an unused section of a dual op amp is used as a comparator to save board space and cost; however, this is not recommended.

Figure 68 and Figure 69 show the AD8546 configured as a comparator, with 100 kΩ resistors in series with the input pins. Any unused channels are configured as buffers with the input voltage kept at the midpoint of the power supplies.

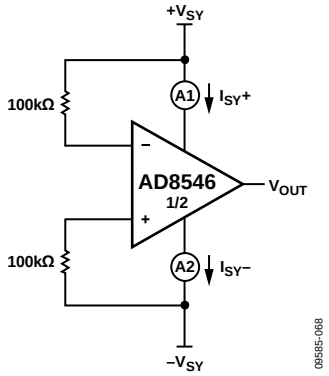


Figure 68. Comparator A

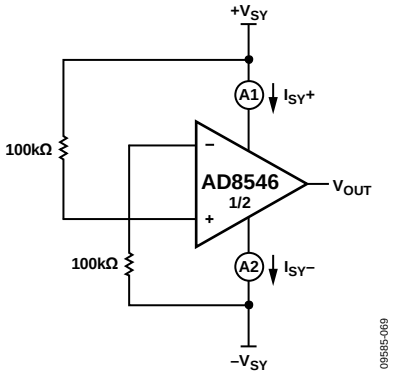


Figure 69. Comparator B

The AD8546 has input devices that are protected from large differential input voltages by Diode D1 and Diode D2 (see Figure 62). These diodes consist of substrate PNP bipolar transistors and conduct whenever the differential input voltage exceeds approximately 600 mV; however, these diodes also allow a current path from the input to the lower supply rail, thus resulting in an increase in the total supply current of the system. As shown in Figure 70, both configurations yield the same result. At 18 V of power supply, I_{SY}+ remains at 36 µA per dual amplifier, but I_{SY}– increases to 140 µA in magnitude per dual amplifier.

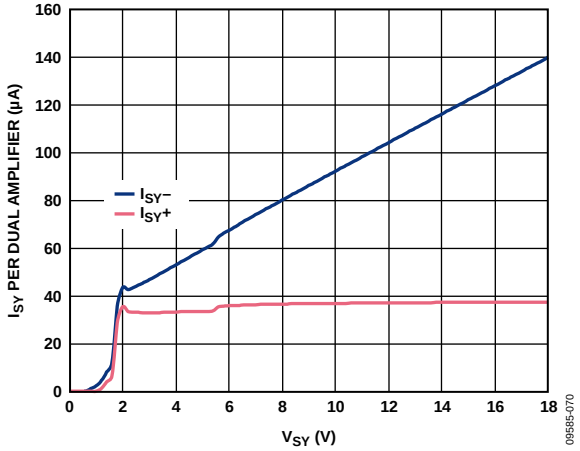


Figure 70. Supply Current vs. Supply Voltage (AD8546 as a Comparator)

Note that 100 kΩ resistors are used in series with the input of the op amp. If smaller resistor values are used, the supply current of the system increases much more. For more information about using op amps as comparators, see the AN-849 Application Note, *Using Op Amps as Comparators*.

4 mA TO 20 mA PROCESS CONTROL CURRENT LOOP TRANSMITTER

A 2-wire current transmitter is often used in distributed control systems and process control applications to transmit analog signals between sensors and process controllers. Figure 71 shows a 4 mA to 20 mA current loop transmitter.

The transmitter is powered directly from the control loop power supply, and the current in the loop carries signal from 4 mA to 20 mA. Thus, 4 mA establishes the baseline current budget within which the circuit must operate.

The AD8546 is an excellent choice due to its low supply current of 33 µA per amplifier over temperature and supply voltage. The current transmitter controls the current flowing in the loop, where a zero-scale input signal is represented by 4 mA of current and a full-scale input signal is represented by 20 mA. The transmitter also floats from the control loop power supply, V_{DD}, whereas signal ground is in the receiver. The loop current is measured at the load resistor, R_L, at the receiver side.

With a zero-scale input, a current of V_{REF}/R_{NULL} flows through R´. This creates a current flowing through the sense resistor, I_{SENSE}, determined by the following equation:

$$I_{SENSE, MIN} = (V_{REF} \times R´)/(R_{NULL} \times R_{SENSE})$$

With a full-scale input voltage, current flowing through R´ is increased by the full-scale change in V_{IN}/R_{SPAN}. This creates an increase in the current flowing through the sense resistor.

$$I_{SENSE, DELTA} = (\textit{Full-Scale Change in } V_{IN} \times R´)/(R_{SPAN} \times R_{SENSE})$$

Therefore

$$I_{SENSE, MAX} = I_{SENSE, MIN} + I_{SENSE, DELTA}$$

When R´ >> R_{SENSE}, the current through the load resistor at the receiver side is almost equivalent to I_{SENSE}.

Figure 71 shows a design for a full-scale input voltage of 5 V. At 0 V of input, loop current is 3.5 mA, and at a full-scale input of 5 V, the loop current is 21 mA. This allows software calibration to fine-tune the current loop to the 4 mA to 20 mA range.

The AD8546 and ADR125 together consume only 160 µA quiescent current, making 3.34 mA current available to power additional signal conditioning circuitry or to power a bridge circuit.

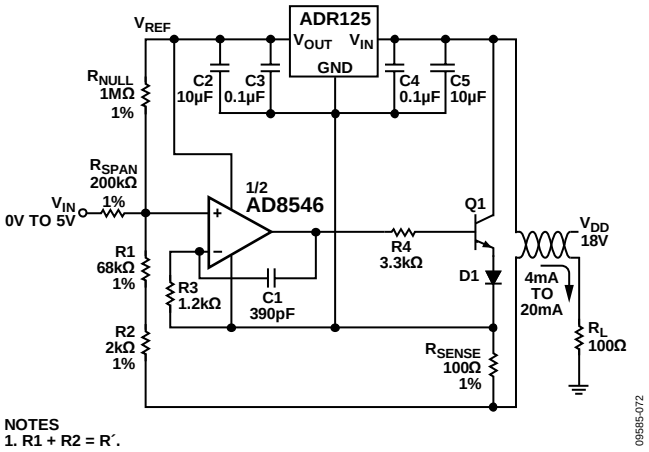
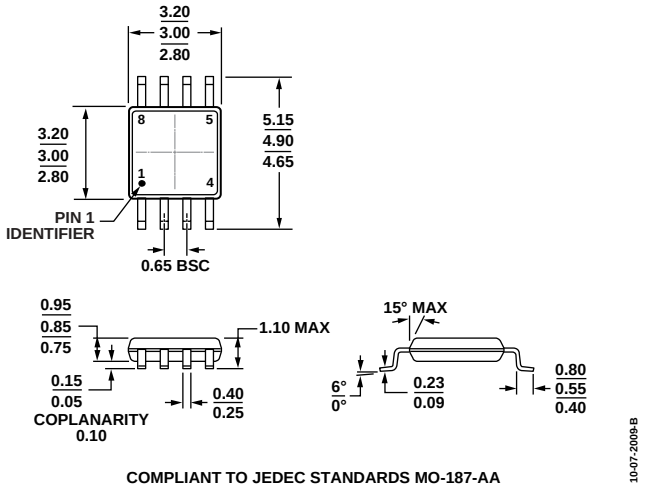


Figure 71. 4 mA to 20 mA Current Loop Transmitter

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 72. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8546ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2V
AD8546ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2V
AD8546ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2V

[1] Z = RoHS Compliant Part.

NOTES

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D09585-0-4/11(A)