AD9125-EBZ
Quick Start Guide

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Getting Started with the AD9125-EBZ Evaluation Board

WHAT'S IN THE BOX

AD9125-EBZ Evaluation Board
Evaluation Board CD
Mini-USB Cable

RECOMMENDED EQUIPMENT

Sinusoidal Clock Source (at least 1.0GHz)
Sinusoidal Clock Source (for modulator LO)
Spectrum Analyzer
DC Power Supply
Data Pattern Generator Series 2 (DPG2)

INTRODUCTION

The AD9125 Evaluation Board connects to a DPG2 to allow for quick evaluation of the AD9125. Control of the SPI port in the AD9125 is available through USB with accompanying PC software.

To ease the subsystem evaluation, a clock distribution chip (AD9516) and a quadrature modulator are also designed into this evaluation board.

SOFTWARE

The AD9125 Evaluation board is designed to receive data from a Data Patten Generator 2 (DPG2). The DAC Software Suite, plus the AD9125 Update, is required for evaluation. The DAC Software Suite is included on the Evaluation Board CD, or can be downloaded from the DPG web site at http://www.analog.com/dpg. This will install DPGDownloader (for loading vectors into the DPG2) and the AD9125 SPI Controller application.

HARDWARE SETUP

Connect a +5V DC power supply to the banana jacks (P5 and P6). A clock source should be connected to the SMA jack labeled J1 (CLKIN). The AD9516 buffers this clock and distributes clock signals with proper frequencies to the AD9125 and the DPG2. In order to monitor the AD9125 outputs, a spectrum analyzer should be connected to the SMA jack labeled J3 (DAC1_P) for I channel DAC or J8 (DAC2_P) for Q channel DAC. The DPG2 connects through connector P1 and P2 on the left edge of the evaluation board, and the USB cable should be connected to the mini USB connector labeled XP2 USB on the lower left side of the board. Note that the PC software needs to be installed before connecting the USB cable to your computer.

JUMPER CONFIGURATIONS

There are 7 pin jumpers and 13 solder jumpers on the evaluation board. The pin jumpers are corresponding to the 6 supplies, i.e., AVDD3.3, DVDD1.8, CVDD1.8 and etc, on the board. They serve as 'switches' that determine if the LDOs on board or external supplies are used for each individual supply. Most of the pin jumpers, except JP1, are 2 pin jumpers. They are shunted by default, which means on board LDOs are used. When an external supply is necessary, pull off the shunt from the corresponding supply and connect the external supply to the SMA jack close to the jumper. JP1 should be left in the default configuration.

Solder jumpers JP4, 5, 6, and 17 determine whether the DAC outputs go to the SMA connectors or to the modulator inputs. When direct DAC outputs are to be monitored, JP4, 5, 6, and 17 should be configured as what Figure 1 shows. When the modulator output is to be measured, they should be configured as what Figure 2 shows.

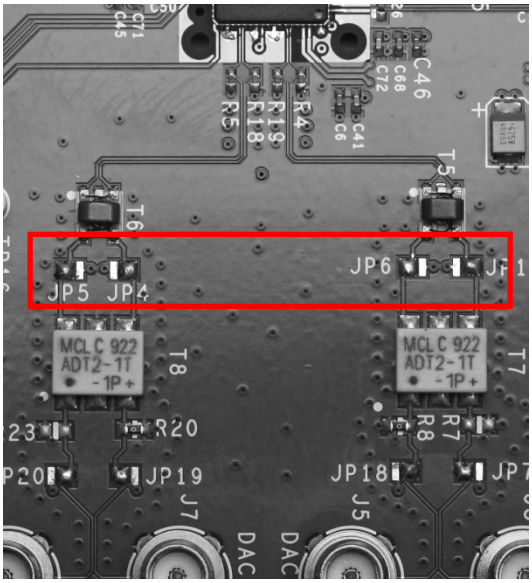

Figure 1 - DAC Output Configuration

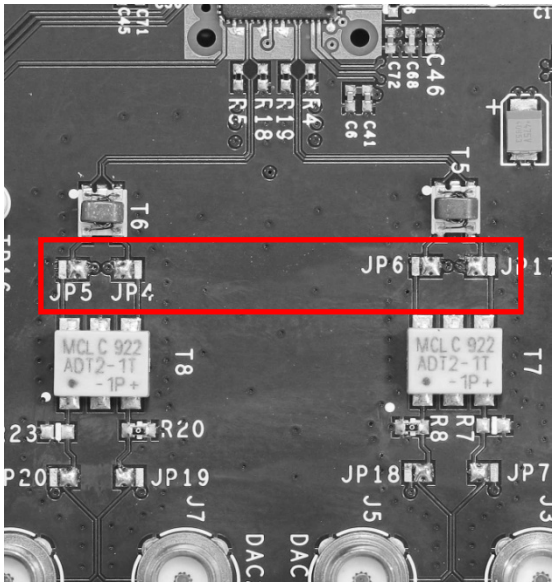

Figure 2 - Modulator Output Configuration

The solder jumper on the left side of C139 determines whether the ref/sync clock of the AD9125 is from the AD9516 or an external source through the SMA jack J14 (AD9125_REF_CLKIN). When the AD9516 is used for the clock source, the jumper should be configured so that the center pad is connected to the top pad. When an external source is used, the center pad should be connected to the bottom pad.

Other solder jumpers should be left in the default configuration.

GETTING STARTED

Single Tone Test

This setup configures the AD9125 to generate a sine wave by using the DPG2 as a data source. This allows the user to measure the single-tone AC performance at the DAC output. Install the software as described in the *Software* section, and connect all the required cables as described in the *Hardware Setup* section. Turn on the power supply.

For this setup, the clock source is set to generate a 500MHz tone at 3dBm. Using 2x interpolation and word mode, the data clock should be 250MHz. Jumpers JP4, 5, 6, and 17 should be set to their DAC output position. Open the AD9125 customer SPI software and go to the 2nd tab (data clock). Set the interpolation rate to 2X. Hit 'run' button. This will set the part to 2x interpolation mode and configure the clock going into the DPG2 to half of the DAC rate.

In DPG2 Downloader software, the 'DCO frequency' shown should be 250MHz. (Due to the resolution of the DPG frequency counter, the measured frequency could be a little off). In the 'evaluation board' drop down menu, the selection should be shown as 'AD9125'. This selection is automatically done when you plug the USB cable into the evaluation board.

Select 'Single Tone' in the 'Add Generated Waveform' drop down menu in the DPG2 Downloader. Set the sample rate to 250MHz and the desired frequency to 31MHz. Check the box of 'Generate Complex Data (I&Q)'. Pick the generated waveforms in the 'I Data Vector' and 'Q Data Vector'. Click Download ( ) and Play ( ). This results in a single-tone at the DAC output centered at 31MHz. The current on the 5V supply should be approximately 700mA with JP11 open (modulator supply off).

SPI CONTROLLER

The SPI Controller application is split into several tabs. These tabs group related functions. Several of the functions provided by the SPI Controller are described here, as they relate to the evaluation board. For complete descriptions of each register, refer to the AD9125 datasheet. In the interest of continuous quality improvements, the images below may not exactly match your version of the software.

Running the SPI Controller

Figure 3

When the *Run* button is clicked, the SPI controller will run once. It will both write and read from the AD9122/AD9125 and setup the clock chip (AD9516) on the evaluation board. The *Run Forever* control will setup both the AD9122/AD9125 and AD9516. This mode of operation will continue to read from the chip and will update the SPI when any of the controls change. The *Force Write* and *Read Only* controls force the controller to write all the controls to the evaluation board or only read from the SPI port.

Data Clock Control

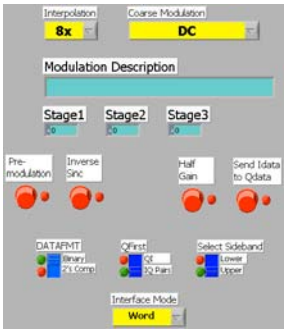

Figure 4

This section, shown in Figure 2, provides control over the Interpolation Rate and Course Modulation. Once the controller is executed, the *Modulation Description* field will return a summary of control. If an improper selection is made, the field will return 'Invalid.' The *DATAFMT* field selects the number format of the incoming data, between unsigned (Binary) and signed (2's compliment). The *QFirst* control selects which DAC receives data first from the interleaved bus. For use with the DPG2, this should always be set to *IQ Pairs*. The *Interface Mode* selects how wide the data bus will be. This setting will need to match the setting in the DPG AD9125 panel for proper operation with the DPG2.

NCO Control

This tab controls the Fine Modulation within the AD9122/AD9125. The top portion of this tab helps the user easily control the frequency shift. It will calculate the NCO Frequency using Data Frequency entered by the user. The NCO can shift the signal by at most +/- $f_{nco}/2$. An indicator also displays the frequency shift from the course modulation on the previous tab. The total shift will be the sum of the course and fine modulations. To manually enter the Frequency Tuning Word (FTW), the Enable Advanced Control will bypass the calculations on the top of the page.

PLL Control

The AD9122/AD9125 has an on-chip PLL. When *PLL_ENABLE* is turned on, the chip will automatically select the appropriate band using the Divder1 and Divider0 values. This tab provides the calculation for the DAC Freq and VCO Freq based on the Reference Clock and the value of the dividers. The VCO Frequency must be between 1 and 2 GHz for proper operation. The auto-band select can be bypassed by enabling *PLL MANUAL* and entering a band in PLL Band Select. Divider1 and Divider0 must still be chosen appropriately in this mode of operation.

Interrupts

This tab provides a visual indication of the state of each interrupt. Enabling the button to the left of each interrupt with enable the interrupt. A green indicator to the right of the button will light when the interrupt is asserted. Once asserted, the interrupt can be acknowledged by pressing the *Clear* button.

Main DAC Control

This tab controls the two main DACs in the AD9122/AD9125. The Full-Scale Current of each DAC can be set with the *I DAC Gain* and *Q DAC Gain* controls. The *I Sleep* and *Q Sleep* controls put their respective DAC into a low-power sleep state. When the AD9122/AD9125 is used with a modulator, the *Phase Compensation/DC Offset* controls can be used to correct any mismatches between the two DACs.

AUX DAC Control

As with the main DACs, the full-scale current of the auxiliary DACs can be set over the SPI port. Each DAC can also be powered down.

Sampling Error Detection

The Sampling Error Detection (SED) checks the data inputs. An 8-byte signature is handed to the AD9122/AD9125. The controller can automatically generate and load the vectors using the DPG2 device. Indicators display the result of the comparison between the input data and the expected signature.

SPI Map

The SPI Map tab provides an overview of all the settings currently written to the part. The individual register values are indicated graphically (with red and green boxes) and numerically. The numeric results can be used in whatever system the AD9122/AD9125 connects to, to duplicate the current settings in the end system.

AD9516 Control

The evaluation board contains its own clock chip. The AD9516 has an optional on-chip PLL. The top half of the control tab helps the user select the appropriate control values for the PLL controller. If the PLL is bypassed, the DAC Clock has the same frequency as the input to the AD9516. Two additional clocks, Ref Clk and DCO Clk, are generated based off of the DAC Clock. The DCO Clock controlling the data frequency can be synced with the interpolation rate on the Data Clock Control tab. If this is enabled, changing the interpolation rate will automatically update the AD9516 to have the appropriate DCO Clock Divider Ratio.

Save and Load

The SPI controller has options to save and load all the control registers. The save takes place after the controller is run once and the load happens before any of the read or writes to the evaluation board.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ANALOG DEVICES

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