AD9789-EBZ
Quick Start Guide

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Getting Started with the AD9789-EBZ Evaluation Board

WHAT'S IN THE BOX

AD9789-EBZ Evaluation Board
Evaluation Board CD
Mini-USB Cable

RECOMMENDED EQUIPMENT

Sinusoidal Clock Source (>2GHz, <0.5ps RMS jitter) OR
Low-Frequency Clock Source (using on-board multiplier)
Spectrum Analyzer
+5Vdc Regulated Power Supply (>1.5Amp)
Data Pattern Generator Series 2 (DPG2)

INTRODUCTION

The AD9789-EBZ Evaluation Board connects to a DPG2 to allow for quick evaluation of the AD9789. Control of the SPI port in the AD9789 is available through USB with accompanying PC software. The AD9789-EBZ allows evaluation of both CMOS and LVDS modes, as well as numerous interface modes of the AD9789. The DPGDownloader software automatically formats the data sent to the DPG2 to account for the interface mode.

SOFTWARE

The AD9789-EBZ is designed to receive data from a DPG2. The DAC Software Suite, plus the AD9789 Update, is required for evaluation. The DAC Software Suite is included on the Evaluation Board CD, or can be downloaded from the DPG web site at http://www.analog.com/dpg. This will install DPGDownloader (for loading vectors into the DPG2) and the AD9789 SPI Controller application.

HARDWARE SETUP

Connect a +5Vdc power supply to the banana jacks (P5 and P6). The clock source (AC or DC coupled) should be connected to the SMA jack labeled S1 (HF_DACCLK), and the spectrum analyzer should be connected to the SMA jack labeled S5 (AOUT_DAC-). The DPG2 connects through connector J3 and J4, and the USB cable should be connected to XP2. Note that the PC software needs to be installed before connecting the USB cable to your computer.

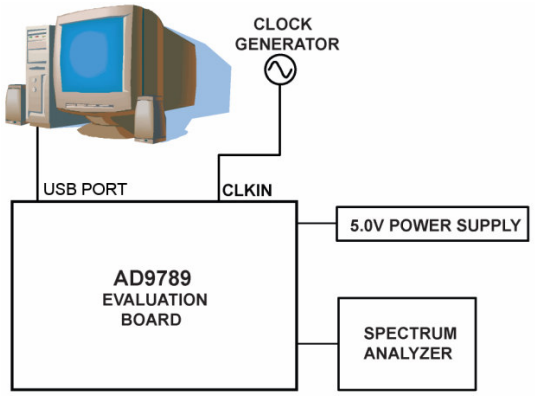

Figure 1

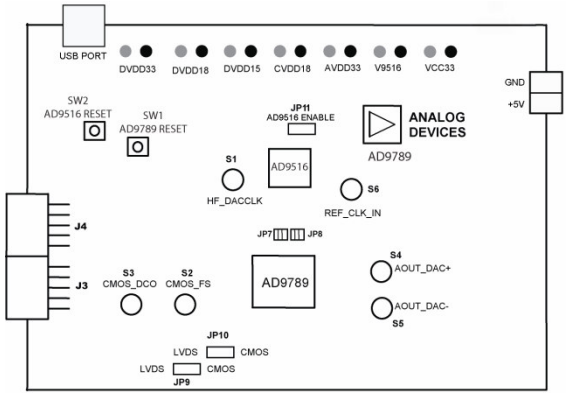

Figure 2

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GETTING STARTED

Three different setups are explained here, each utilizing different sections of the AD9789 and the AD9789-EBZ Evaluation Board. All three assume a high frequency, low-jitter input clock. To use a low frequency clock, see the section entitled *Using the AD9516 as the Clock* Source.

Internal Single-Tone Test

This setup configures the AD9789 to generate a sine wave internally by using the on-chip NCO. This allows the user to measure the single-tone AC performance at the DAC output without needing an external data source. In this example, the data inputs are held constant, only channel 0 is enabled and its NCO center frequency is set to 120MHz (Fdac=2GHz). This will modulate the DC static value on the port up to the NCO frequency resulting in a single-tone at the DAC output centered at 120MHz.

Install the software as described in the *Software* section, and connect all the required cables as described in the *Hardware Setup* section. Turn on the power supply. The current should be approximately 200mA. For this setup, the clock source should be set to generate a 2.0GHz tone at 2dBm. Jumpers JP9 and JP10 should be set to their CMOS position (away from the DPG2 connector).

Open the AD9789 SPI application from your Start Menu (Start > Programs > Analog Devices > AD9789-EBZ > AD9789 SPI). In the lower left, click the Load button (it will stay depressed). Press the Run ( ) button in the upper left. A dialog will appear asking for the file to load. Open *AD9789_SPIsettings_Int_Sine_Wave.txt*, located in the same directory as the SPI controller. After the run has completed, click the Load button again to disable it. Click the PARMNEW control in the Reference/Sample/Sync Clock Control block and click the run button to enable the digital clocks. After the run completes, disable the PARMNEW button and run the SPI controller again.

Also, ensure that the FREQNEW control bit is set. This bit needs to be set for any changes made to the center frequency of the BPF and the rate converter (P/Q) to take effect. If the FREQNEW is set properly, the read back indicators for the rate converter and BPF will be updated to the correct values upon the second run of the SPI program. Note that FREQNEW is a self-clearing bit and can therefore always be set high.

Expected DAC Performance

For the setup described in the previous sections, the expected DAC output spectral performance is illustrated in Figure 3.

DAC Settings: f_{DAC}=2GHz, static CMOS data, f_{C0}=120MHz, f_{BPF} =120MHz, Ch. 1, 2 and 3 are disabled.

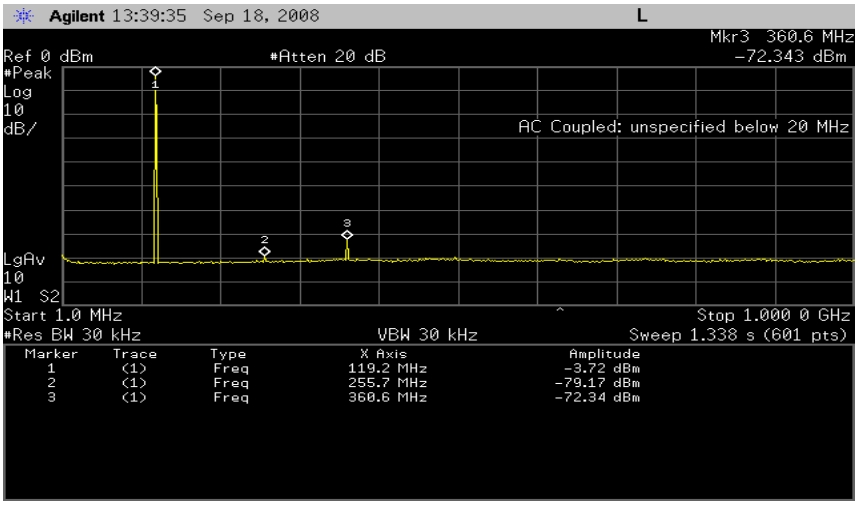

Figure 3 - AD9789 Output Spectrum, Fout = 120MHz, Fdac = 2000MHz

Internal QAM Test

In this example, the AD9789 is configured to generate a QAM vector internally by using the internal pseudo-random number (PRN) generator in conjunction with the on-chip QAM encoder. This allows the user to measure the AC performance of a QAM signal at the DAC output without needing an external data source. The steps that follow show the user how to enable the internal PRN generator and setup each channel of the data path to map the PRN to 256QAM, shape and interpolate the QAM carrier such that it is DOCSIS compliant and modulate each channel to 834MHz, 840MHz, 846MHz, and 852MHz respectively (Fdac=2.29376GHz).

Install the software as described in the *Software* section, and connect all the required cables as described in the *Hardware Setup* section. Turn on the power supply. The current should be approximately 200mA. For this setup, the clock source should be set to generate a 2.29376GHz tone at 2dBm. Jumpers JP9 and JP10 should be set to their LVDS position (towards the DPG2 connector).

Open the AD9789 PRN software (Start > Programs > Analog Devices > AD9789-EBZ > AD9789 PRN). Click Run, and wait for the status indicator to become bright green. Next, open the AD9789 SPI application (Start > Programs > Analog Devices > AD9789-EBZ > AD9789 SPI). Click the Load button, and then click the Run button (). When prompted for a file to load, select *AD9789_SPISettings_Int_QAM.txt*. Once that run has completed, click the Load button again to de-select it. Enable the PARMNEW button, and click Run again. De-select PARMNEW after the run has completed.

Also, ensure that the FREQNEW control bit is set. This bit needs to be set for any changes made to the center frequency of the BPF and the rate converter (P/Q) to take effect. If the FREQNEW is set properly, the read back indicators for the rate converter and BPF will be updated to the correct values upon the second run of the SPI program. Note that FREQNEW is a self-clearing bit and can therefore always be set high.

Expected DAC Performance

For the setup described in above the expected DAC output spectral performance is illustrated in Figure 4.

DAC Settings: f_{DAC} = 2.29376GHz, f_{C0} = 834MHz, f_{C1} = 840MHz, f_{C2} = 846MHz, f_{C3} = 852MHz, f_{BPF} = 843MHz, QAM Mapper, SRRC, Filters1-4 enabled

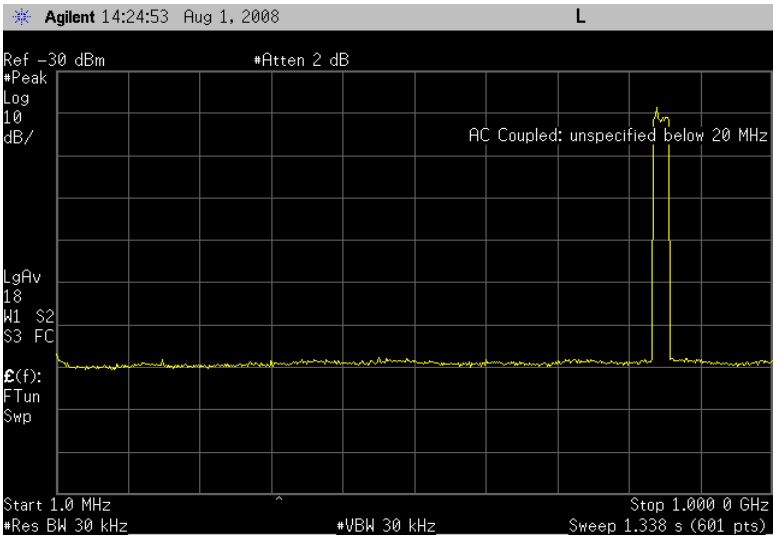

Figure 4

The center frequencies, QAM Mapper modes, # of carriers, etc. can be varied for an assortment of AC performance testing.

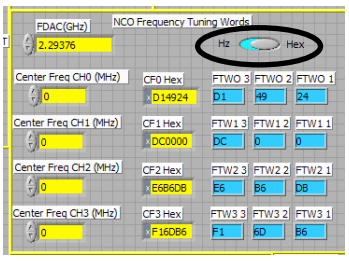

Figure 5

Take note of the Hz or Hex slide control in Figure 5. Once a SPI configuration file is loaded this slide control will be set to Hex, meaning that center frequencies of the channels are controlled by entering the Frequency Tuning Word (FTW) for each NCO. The user can opt to change this control to Hz and control the center frequencies of the channels by inputting the desired frequency in MHz and the software will calculate the FTW. Note that for this calculation to be accurate, the user must also enter the DAC rate in GHz.

Below are the recommended Sum Scale values for all QAM Mapper modes and channel counts.

QAM Mode	Sum Scale Value			
	1 Channel	2 Channel	3 Channel	4 Channel
DVB 16-QAM	48	28	22	16
DVB 32-QAM	54	34	26	20
DVB 64-QAM	54	34	26	20
DVB 128-QAM	80	50	38	30
DVB 256-QAM	54	34	26	20
DOCSIS 64-QAM	54	34	26	20
DOCSIS 256-QAM	54	34	26	20

Table 1

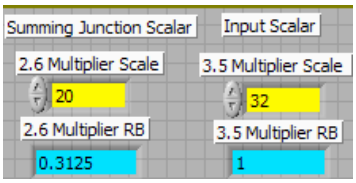

Figure 6

QAM Vector Playback with the DPG2

Install the software as described in the *Software* section, and connect all the required cables as described in the *Hardware Setup* section. Turn on the power supply. The current should be approximately 200mA. Turn on the clock source, with a 2.4GHz tone at 2dBm. This setup will use the LVDS mode, so ensure that jumpers JP9 and JP10 are in their LVDS positions (towards the DPG2 connector).

Open the AD9789 SPI application from your Start Menu (Start > Programs > Analog Devices > AD9789-EBZ > AD9789 SPI). If you have the SPI controller open from a previous setup, close and re-open it before continuing. Press the Run ( ) button in the upper left. The current measured by the power supply should jump to approximately 1.0A. Set the spectrum analyzer to center at 843MHz, with a 24MHz span, and 30kHz resolution bandwidth. Four tones should now be visible, at 834MHz, 840MHz, 846MHz, and 852MHz. Click on the PARMNEW button in the SPI controller. It should turn red. Click Run again. The LOCK indicator in the upper left of the screen should now be green.

The part is now ready to receive data. Open DPGDownloader on your PC (Start > Programs > Analog Devices > DPG > DPGDownloader). Under the Evaluation Board drop down list, the AD9789 should already be selected (if it is not, select it). For the Port Configuration, select LVDS. Once the configuration download is complete, it should be setup as shown in Figure 7. Now load in the included example vector of random data by clicking Add Data File. The vector can be found in *C:\Program Files\Analog Devices\HSDAC\AD9789\Random Data.hex*.

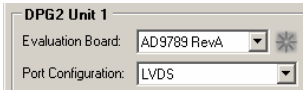

Figure 7

Once the file has been processed by DPGDownloader, the software must be setup to match the settings in the AD9789. Select 32-Bit for the Bus Width, 8-bit for the Data Width, and Real for the Data Format. Select the check boxes next to each channel (4 in all). For the Real Data Vector in Channel 1, select *Random Data.hex* from the drop down list. Leave the other channels with *None* as the vector. Figure 8 show the DPGDownloader software configured.

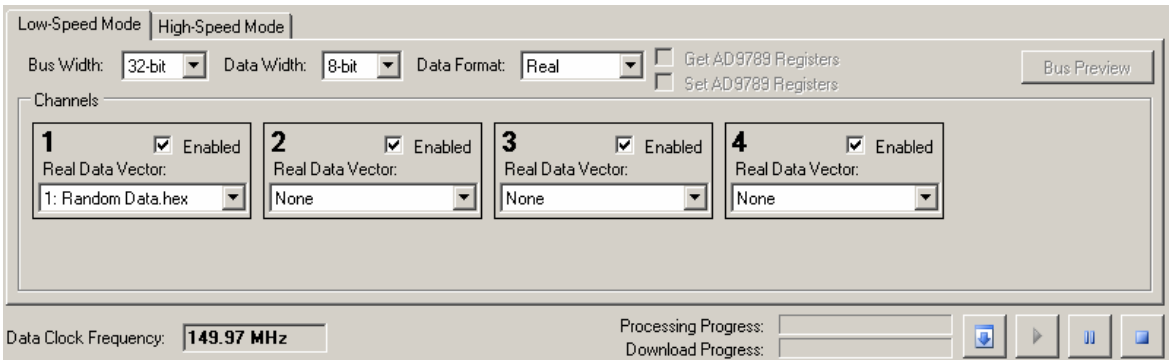

Figure 8

To begin streaming the data into the AD9789, press the Download button ( ), and then the Play button ( ). On the spectrum analyzer, the first carrier (at 834 MHz) should disappear, with a 6MHz wide channel of data in its place. This is the random data from the vector file being mapped into symbols by the QAM Mapper inside the AD9789.

SPI CONTROLLER

This section discusses several parts of the SPI controller interface, as they affect this evaluation system. For complete descriptions of each SPI register, see the AD9789 datasheet. In the interest of continuous quality improvements, the images below may not exactly match your version of the software.

SPI Setup and Reset/Power Down

This section allows for changing the SPI format, as well as soft resetting and powering down the AD9789. Do not change the SDIO_DIR or LSB_FIRST controls. Changing these bits will make the USB hardware unable to communicate with the AD9789. If these bits become set, a hard reset (power cycle) will be required to restore their original settings.

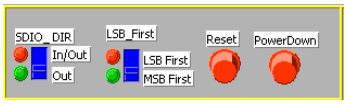

Figure 9

Interrupt Request Controls

These controls enable and disable the various interrupts available on the AD9789. These settings will not affect the evaluation system, although the LOCK and LOCKLOST indicators are useful when debugging clock issues.

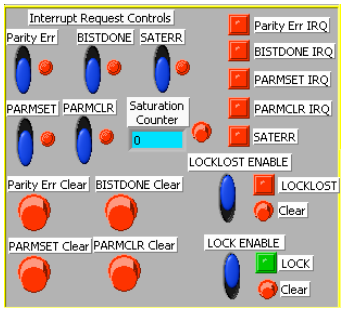

Figure 10

Interface Control

These controls affect the interface between the AD9789 and the DPG2. The DCO_INV switch should stay off. The I/F_MODE switch selects between Channelizer Mode and QDUC Mode. When changing this switch, be sure to select the correct tab in DPGDownloader.

The CHANRPI switch affects the order in which the AD9789 expects the data for each channel (Channelizer Mode only). When this switch is high, all four channels in DPGDownloader need to be enabled. Channels that are turned off in the SPI controller should be set to *None* as the vector in DPGDownloader. When this switch is low, only the channels that are enabled in the SPI controller should be enabled in DPGDownloader.

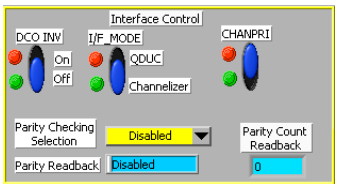

Figure 11

Data Control

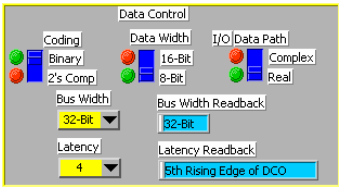

Figure 12

These bits control how the data is interpreted by the AD9789. The Coding switch selects between Binary (unsigned) and 2's Comp (signed, 2's compliment format). Both options are valid for this evaluation system. Ensure that the vectors used are in the correct format.

The Bus Width, Data With, and Data Path switches control how the data is sent over the bus. Regardless of what these are set to, the DPGDownloader settings must match for proper data transfer. The Latency switch controls when the AD9789 beings sampling data. For the DPG2, this should be left at 4, for LVDS bus mode, or 5 for CMOS bus mode.

Channel Select

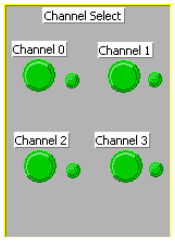

Figure 13

The four switches in this section control which of the four data channels are enabled. If the CHANPRI bit is high (see *Interface Control* section), all four channels in DPGDownloader should be enabled, regardless of the setting of these switches. However, if CHANRPI is low, then the channels in DPGDownloader should be enable or disabled in accordance with these switches.

In QDUC Mode, all channels will get identical data. It is common in this case to turn off all but one channel.

Bypass Controls

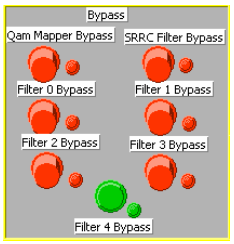

Figure 14

The switches in this section determine which of the functional blocks in the data path are enabled. Red indicates that the block is enabled (and thus not bypassed), while green indicates the block is disabled (bypassed). Each of the filters (the SRRC and Filter 0 through Filter 4) will drop the frequency of the frame sync by two (and thus the effective sample rate). They will not affect the DCO frequency (which is displayed in DPGDownloader). The QAM Mapper must be disabled in QDUC Mode.

Numerically Controlled Oscillator (NCO) Frequency Controls

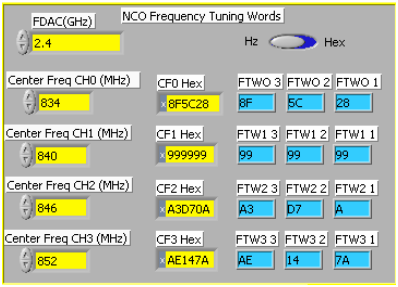

Figure 15

The controls in this section affect where the four carriers will be placed, using the internal modulators. First, enter the frequency of the input clock in the FDAC box. Then, enter the desired carrier frequencies. Note that all four carriers must appear in ascending order, 6MHz apart. For example, in Figure 15, the first carrier is at 834MHz. The next carrier is 6MHz above this, at 840MHz. The next carriers fall at 846MHz and 852MHz, each 6MHz above the previous carrier. The SPI controller software will automatically calculate the required register value in hex for the desired frequency. To input the hex value directly, move the horizontal switch to *Hex*.

Reference/Sample/Sync Clock Control

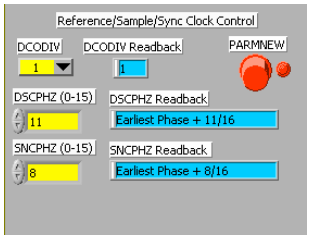

Figure 16

The DCODIV control determines the frequency of the Data Clock Out (DCO) clock. This clock is provided to the DPG2, and is used as the data sample clock. The DCO frequency will always be 1/16th of the input clock, in addition to whatever division is selected in this section.

The DSCPHZ and SNCPHZ controls affect when the AD9789 samples the data on the bus. Refer to the datasheet for detailed information on the proper setting of these options. The default values of 11 and 8 are correct for using the AD9789-EBZ with the DPG2 with a clock in the 2GHz range.

After any of the options in this section are changed, the PARMNEW bit must be cycled. Enabled it (green), run the SPI controller to apply it, and then disable it (red) and run the SPI controller again.

Summing Junction Scalar and Input Scalar Controls

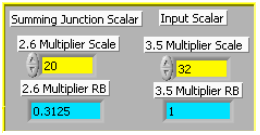

Figure 17

These options will not affect the evaluation system per-se. However, if these are set too high, the AD9789 will saturate internally, leading to a very poor output spectrum. Refer to the datasheet for recommended values. The *Interrupt Request Controls* contain a saturation counter to aid in determining if saturation has occurred. If

this counter is greater than zero, these Multiplier values should be adjusted. The counter should then be reset by cycling the switch to the right of the count.

Rate Converter Controls

The Rate Converter will affect the frequency of the Frame Sync signal. If the rate converter ratio is too large, certain modes that require many clock cycles may not be able to function.

The Center Frequency BPF should be set to center frequency of all active channels. This will ensure that the band-pass filter is centered on where the carriers are.

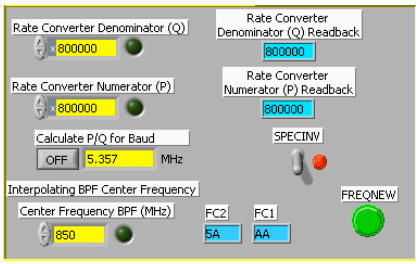

Figure 18

USING THE AD9516 AS THE CLOCK SOURCE

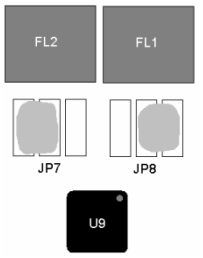

Figure 19

The AD9789-EBZ has an AD9516 Clock Generator on board to allow evaluation without a high frequency, low jitter clock source. To enable this, several steps must be performed on the stock board. First, JP8, a three-way solder jumper, must be soldered to the right position, as shown in Figure 19. This will connect the AD9789's clock input to one of the outputs of the AD9516. Note that this will prevent the HF_DACCLK SMA jack from functioning.

Next, move JP11 to position 2-3. This enables the AD9516. The current measured from the +5Vdc power supply will increase by approximately 300mA. Run the AD9516 Load application (Start > Programs > Analog Devices > AD9789-EBZ > AD9516 Load). When prompted, select *AD9516_SPI_settings_out0_out2_ref_95MHz.txt* as the file to read. Once the application has finished writing to the AD9516, it can be closed.

Connect the clock source to S6 (REF_CLK_IN), and set it to generate a 95.573MHz clock with 0dBm amplitude. This will generate a 2.29376GHz clock for the AD9789. This signal is also available at S10/S11 for debugging the AD9516.

ELECTRICAL INTERFACE SELECTION

The AD9789-EBZ is designed to allow evaluation of both the CMOS and LVDS modes of the AD9789. For LVDS mode, the selection jumpers JP9 and JP10 should be placed closer to the DPG2 connector (labeled LVDS_BUS and LVDS_CTRL on the board). For CMOS, the jumpers should be reversed. In DPGDownloader, select the corresponding Configuration. Note that mixing modes (for example, CMOS_BUS and LVDS_CTRL) is not supported on this evaluation board.

In CMOS mode, the CMOS_DCO (S3) and CMOS_FS (S2) SMA jacks are enabled. They are for observation only; they do not need to be cabled to the DPG2. Both signals are also routed through the main DPG2 connector.

Between CMOS and LVDS modes, the register settings can remain the same, with the exception of the Latency register in the Data Control section. This should be 4 in LVDS mode, and 5 in CMOS mode (when used with the DPG2).