Precision, Ultralow Noise, RRIO, Zero-Drift Op Amp

Data Sheet

ADA4528-1

FEATURES

Low offset: 2.5 μV maximum
Low offset voltage drift: 0.015 μV/°C maximum
Low noise
  5.6 nV/√Hz at f = 1 kHz, A_V = +100
  97 nV p-p at f = 0.1 Hz to 10 Hz, A_V = +100
Open-loop voltage gain: 130 dB minimum
CMRR: 135 dB minimum
PSRR: 130 dB minimum
Gain bandwidth product: 4 MHz
Single-supply operation: 2.2 V to 5.5 V
Dual-supply operation: ±1.1 V to ±2.75 V
Rail-to-rail input and output
Unity-gain stable

APPLICATIONS

Thermocouple/thermopile
Load cell and bridge transducer
Precision instrumentation
Electronic scales
Medical instrumentation
Handheld test equipment

GENERAL DESCRIPTION

The ADA4528-1 is an ultralow noise, zero-drift operational amplifier featuring rail-to-rail input and output swing. With an offset voltage of 2.5 μV, offset voltage drift of 0.015 μV/°C, and typical noise of 97 nV p-p (0.1 Hz to 10 Hz, A_V = +100), the ADA4528-1 is well suited for applications in which error sources cannot be tolerated.

The ADA4528-1 has a wide operating supply range of 2.2 V to 5.5 V, high gain, and excellent CMRR and PSRR specifications that make it ideal for precision amplification of low level signals, such as position and pressure sensors, strain gages, and medical instrumentation.

The ADA4528-1 is specified over the extended industrial temperature range (−40°C to +125°C) and is available in an 8-lead MSOP and an 8-lead LFCSP package.

For more information on the ADA4528-1, refer to AN-1114 *Lowest Noise Zero-Drift Amplifier Has 5.6 nV/√Hz Voltage Noise Density.*

PIN CONFIGURATIONS

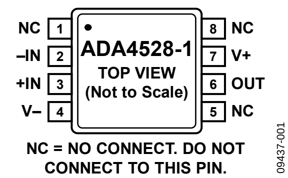

Figure 1. 8-Lead MSOP

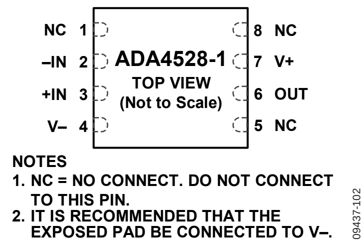

Figure 2. 8-Lead LFCSP

Table 1. Analog Devices, Inc., Zero-Drift Op Amp Portfolio[1]

Type	Ultralow Noise	Micropower (<20 μA)	Low Power (<1 mA)	16 V Operating Voltage
Single	ADA4528-1	ADA4051-1	AD8628	AD8638
			AD8538	
Dual		ADA4051-2	AD8629	AD8639
			AD8539	
Quad			AD8630	

[1] See www.analog.com for a selection of zero-drift operational amplifiers.

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TABLE OF CONTENTS

REVISION HISTORY

9/11—Rev. 0 to Rev. A

Added 8-Lead LFCSP_WD Package ... Universal
Changes to General Description Section ... 1
Added Figure 2; Renumbered Sequentially ... 1
Changes to Offset Voltage, Offset Voltage Drift, Power Supply Rejection Ratio, and Settling Time to 0.1% Parameters, Table 2 ... 3
Changes to Thermal Resistance Section and Table 5 ... 5
Changes to Figure 41 and Figure 44 ... 12
Changes to Figure 45 and Figure 48 ... 13
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

1/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

V_S = 2.5 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 2.5 V		0.3	2.5	µV
		−40°C ≤ T_A ≤ +125°C; MSOP package			4	µV
		−40°C ≤ T_A ≤ +125°C; LFCSP package			4.3	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C; MSOP package		0.002	0.015	µV/°C
		−40°C ≤ T_A ≤ +125°C; LFCSP package			0.018	µV/°C
Input Bias Current	I_B			220	400	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current	I_{OS}			440	800	pA
		−40°C ≤ T_A ≤ +125°C			1	nA
Input Voltage Range			0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	135	158		dB
		−40°C ≤ T_A ≤ +125°C	116			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 2.4 V	130	140		dB
		−40°C ≤ T_A ≤ +125°C	126			dB
		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	125	132		dB
		−40°C ≤ T_A ≤ +125°C	121			dB
Input Resistance, Differential Mode	R_{INDM}			225		kΩ
Input Resistance, Common Mode	R_{INCM}			1		GΩ
Input Capacitance, Differential Mode	C_{INDM}			15		pF
Input Capacitance, Common Mode	C_{INCM}			30		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.49	2.495		V
		−40°C ≤ T_A ≤ +125°C	2.485			V
		R_L = 2 kΩ to V_{CM}	2.46	2.48		V
		−40°C ≤ T_A ≤ +125°C	2.44			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		5	10	mV
		−40°C ≤ T_A ≤ +125°C			15	mV
		R_L = 2 kΩ to V_{CM}		20	40	mV
		−40°C ≤ T_A ≤ +125°C			60	mV
Short-Circuit Current	I_{SC}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +10		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.2 V to 5.5 V	130	150		dB
		−40°C ≤ T_A ≤ +125°C	127			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		1.4	1.7	mA
		−40°C ≤ T_A ≤ +125°C			2.1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		0.45		V/µs
Settling Time to 0.1%	t_s	V_{IN} = 1.5 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = −1		7		µs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		4		MHz
Phase Margin	Φ_M	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		57		Degrees
Overload Recovery Time		R_L = 10 kΩ, C_L = 100 pF, A_V = −10		50		µs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		97		nV p-p
Voltage Noise Density	e_n	f = 1 kHz, A_V = +100		5.6		nV/√Hz
		f = 1 kHz, A_V = +100, V_{CM} = 2.0 V		5.5		nV/√Hz
Current Noise	i_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		10		pA p-p
Current Noise Density	i_n	f = 1 kHz, A_V = +100		0.7		pA/√Hz

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_S = 5 V, V_{CM} = V_{SY}/2 V, T_A = +25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 5 V		0.3	2.5	μV
		−40°C ≤ T_A ≤ +125°C			4	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.002	0.015	μV/°C
Input Bias Current	I_B			90	200	pA
		−40°C ≤ T_A ≤ +125°C			300	pA
Input Offset Current	I_{OS}			180	400	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	137	160		dB
		−40°C ≤ T_A ≤ +125°C	122			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4.9 V	127	139		dB
		−40°C ≤ T_A ≤ +125°C	125			dB
		R_L = 2 kΩ, V_O = 0.1 V to 4.9 V	121	131		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Input Resistance, Differential Mode	R_{INDM}			190		kΩ
Input Resistance, Common Mode	R_{INCM}			1		GΩ
Input Capacitance, Differential Mode	C_{INDM}			16.5		pF
Input Capacitance, Common Mode	C_{INCM}			33		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.99	4.995		V
		−40°C ≤ T_A ≤ +125°C	4.98			V
		R_L = 2 kΩ to V_{CM}	4.96	4.98		V
		−40°C ≤ T_A ≤ +125°C	4.94			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		5	10	mV
		−40°C ≤ T_A ≤ +125°C			20	mV
		R_L = 2 kΩ to V_{CM}		20	40	mV
		−40°C ≤ T_A ≤ +125°C			60	mV
Short-Circuit Current	I_{SC}			±40		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +10		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.2 V to 5.5 V	130	150		dB
		−40°C ≤ T_A ≤ +125°C	127			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		1.5	1.8	mA
		−40°C ≤ T_A ≤ +125°C			2.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		0.5		V/μs
Settling Time to 0.1%	t_s	V_{IN} = 4 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = −1		10		μs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		4		MHz
Phase Margin	Φ_M	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		57		Degrees
Overload Recovery Time		R_L = 10 kΩ, C_L = 100 pF, A_V = −10		50		μs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		99		nV p-p
Voltage Noise Density	e_n	f = 1 kHz, A_V = +100		5.9		nV/√Hz
		f = 1 kHz, A_V = +100, V_{CM} = 4.5 V		5.3		nV/√Hz
Current Noise	i_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		10		pA p-p
Current Noise Density	i_n	f = 1 kHz, A_V = +100		0.5		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$\pm V_{SY} \pm 0.3$ V
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.5 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

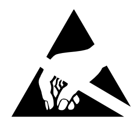
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a 4-layer JEDEC thermal board with the exposed pad soldered to the PCB.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-12)	80	14	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

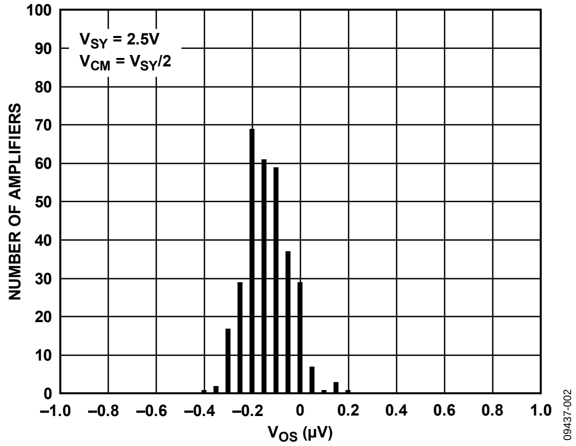


Figure 3. Input Offset Voltage Distribution

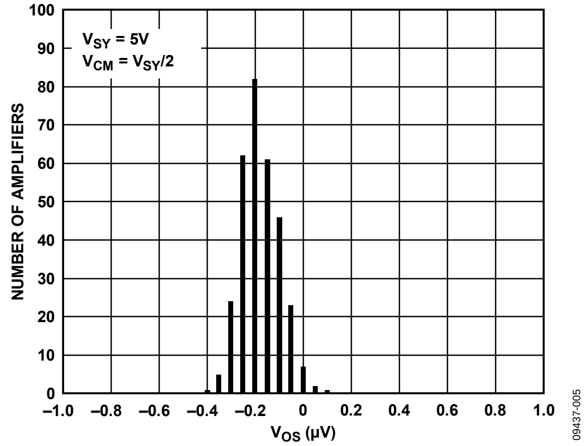


Figure 6. Input Offset Voltage Distribution

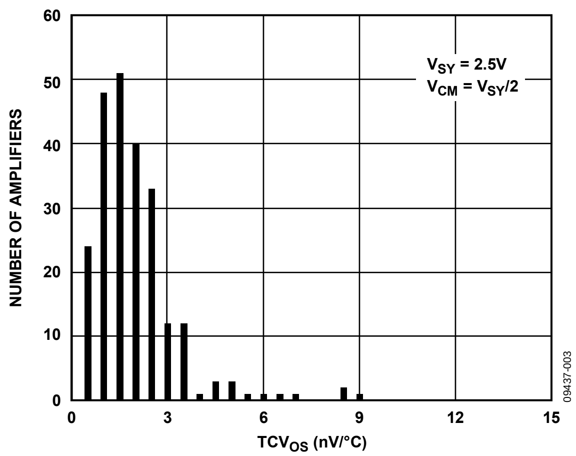


Figure 4. Input Offset Voltage Drift Distribution

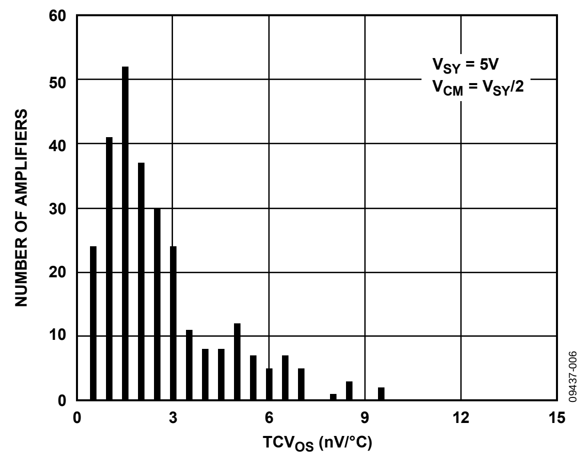


Figure 7. Input Offset Voltage Drift Distribution

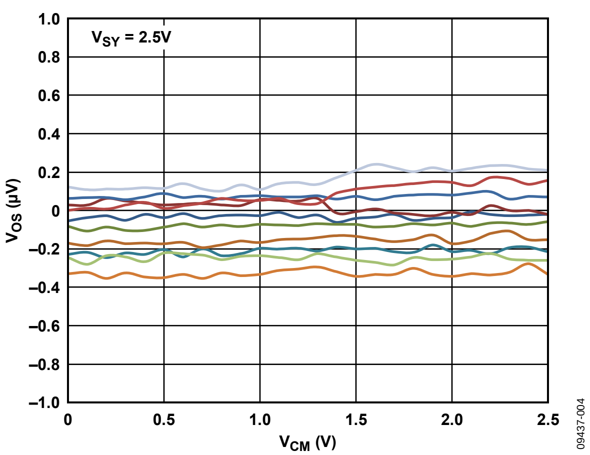


Figure 5. Input Offset Voltage vs. Common-Mode Voltage

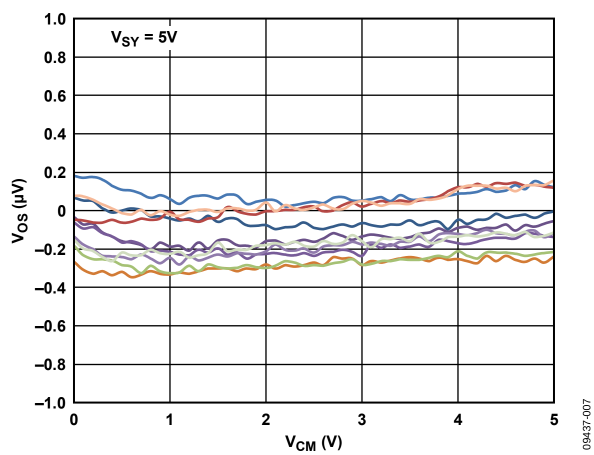


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

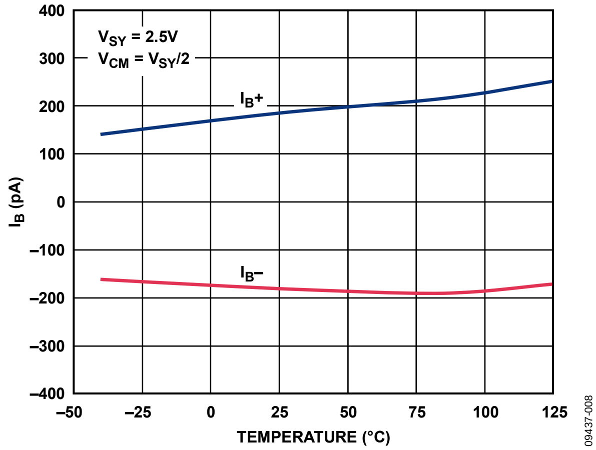


Figure 9. Input Bias Current vs. Temperature

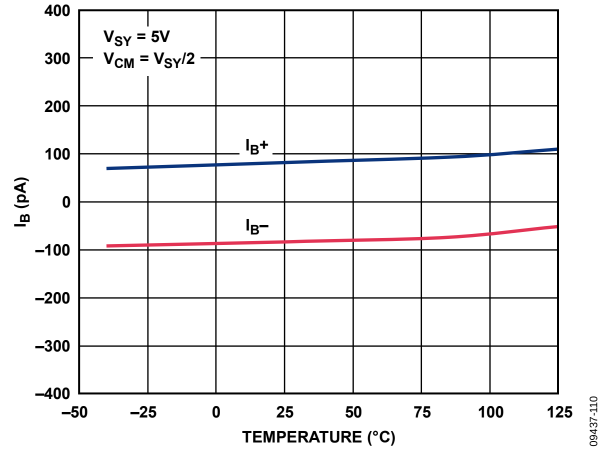


Figure 12. Input Bias Current vs. Temperature

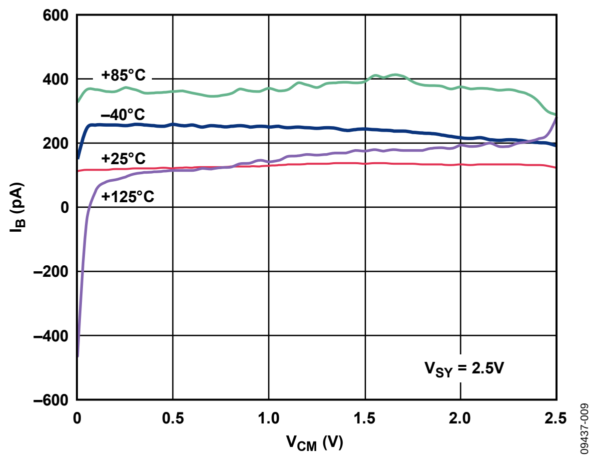


Figure 10. Input Bias Current vs. Common-Mode Voltage

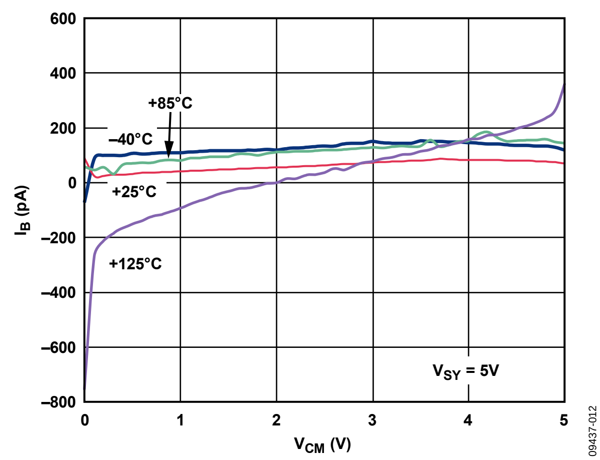


Figure 13. Input Bias Current vs. Common-Mode Voltage

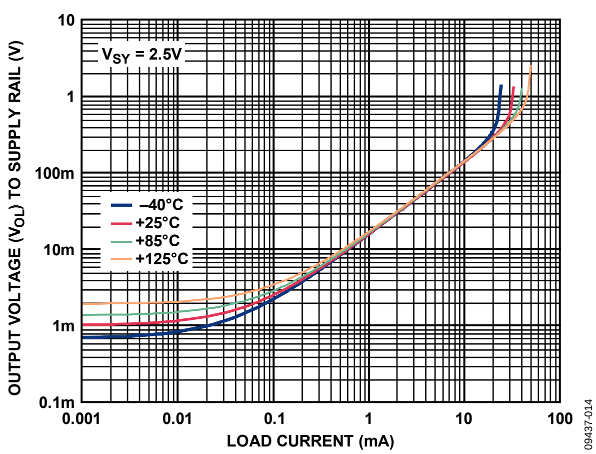


Figure 11. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

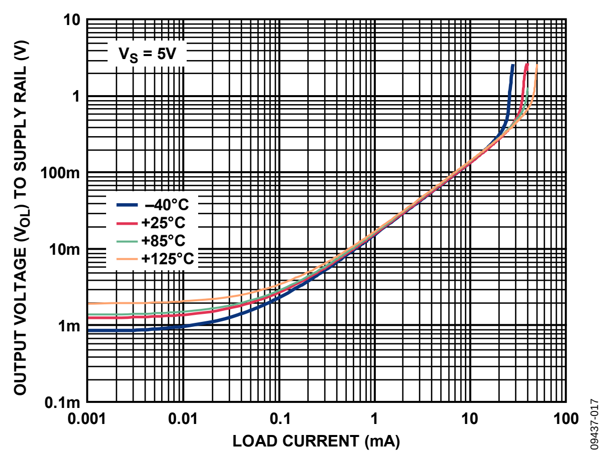


Figure 14. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

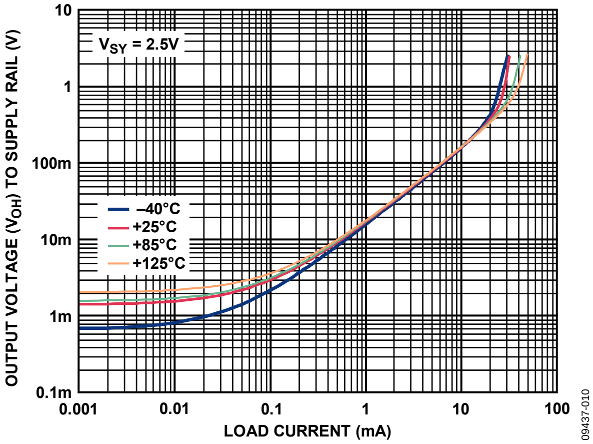


Figure 15. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

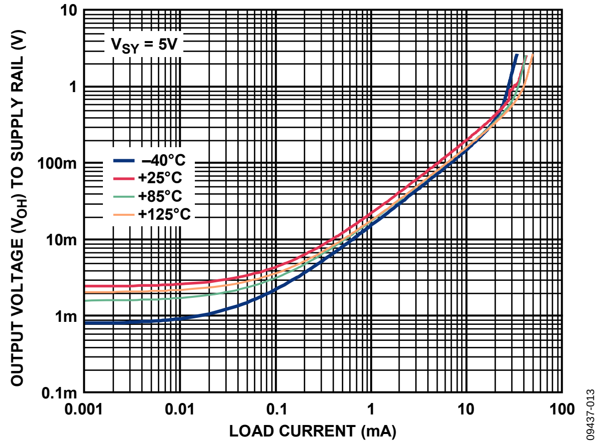


Figure 18. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

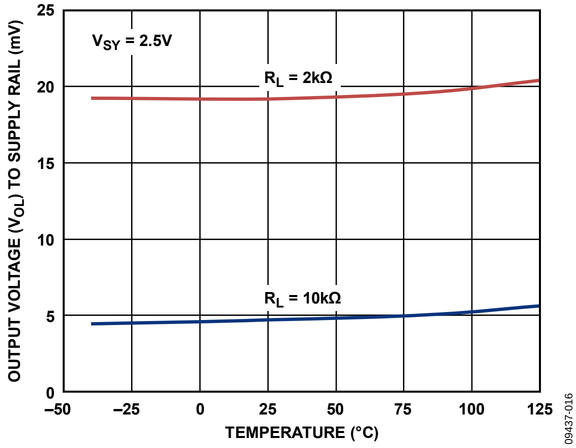


Figure 16. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

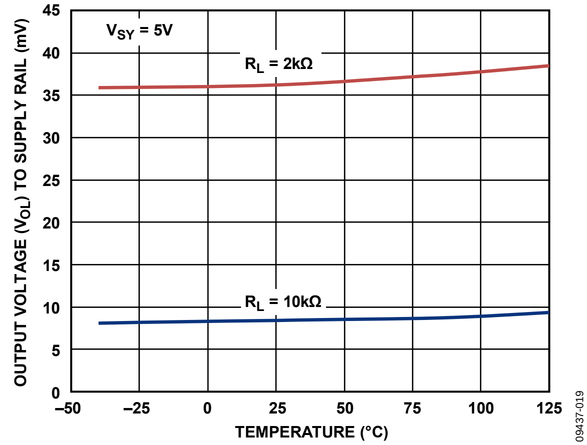


Figure 19. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

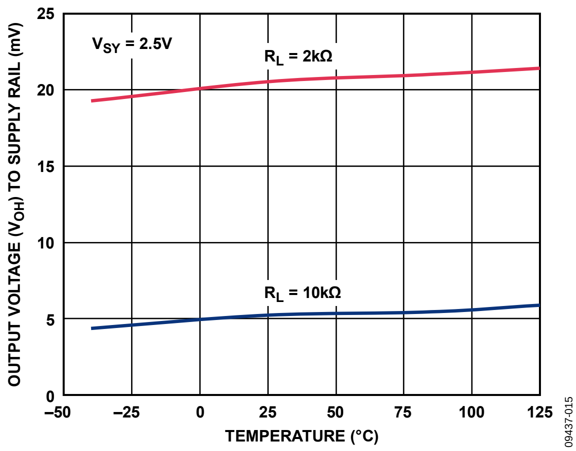


Figure 17. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

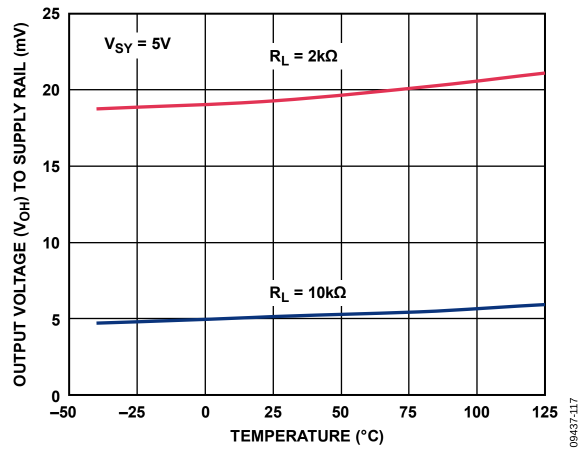


Figure 20. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

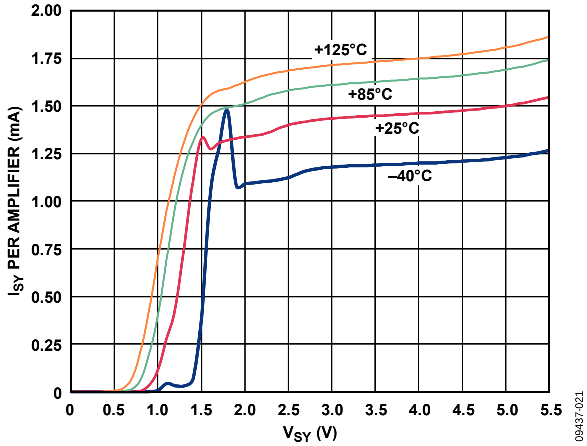


Figure 21. Supply Current vs. Supply Voltage

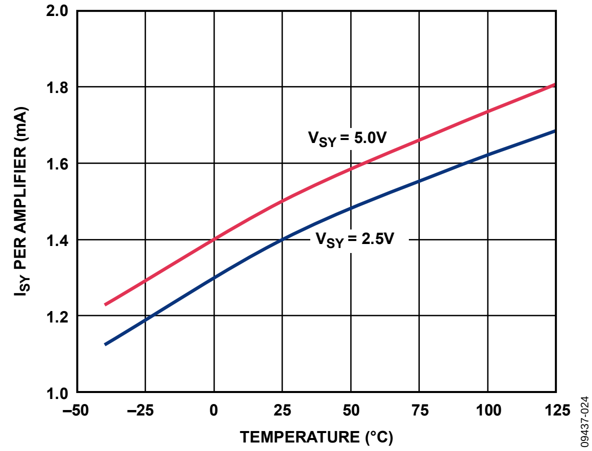


Figure 24. Supply Current vs. Temperature

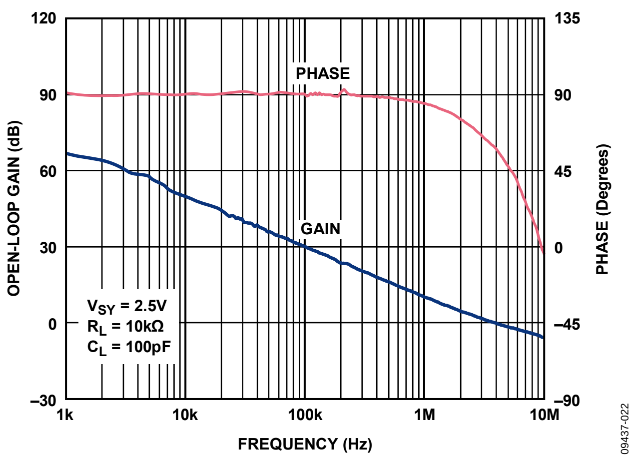


Figure 22. Open-Loop Gain and Phase vs. Frequency

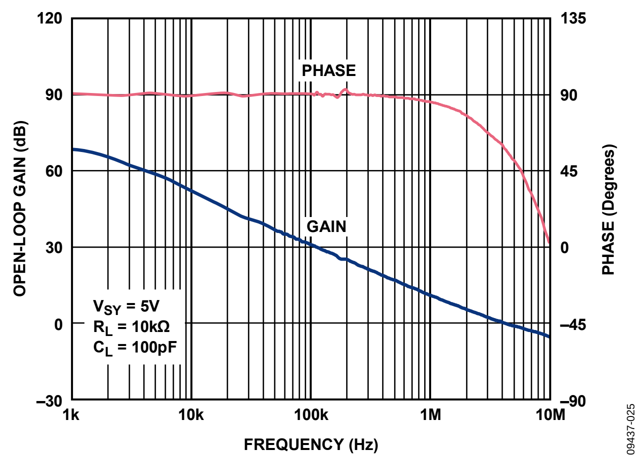


Figure 25. Open-Loop Gain and Phase vs. Frequency

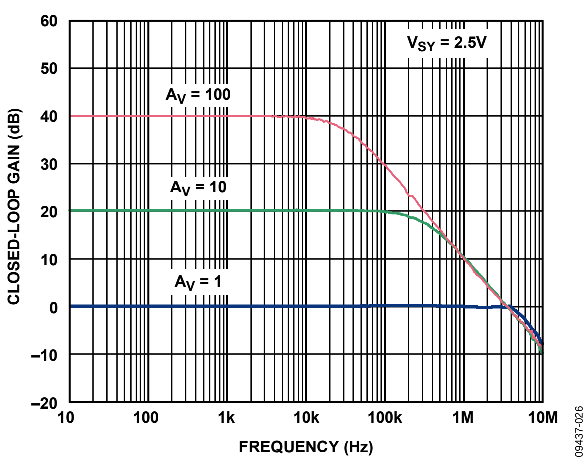


Figure 23. Closed-Loop Gain vs. Frequency

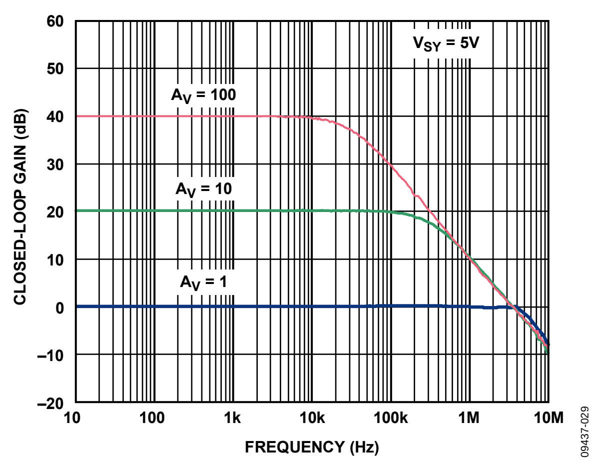


Figure 26. Closed-Loop Gain vs. Frequency

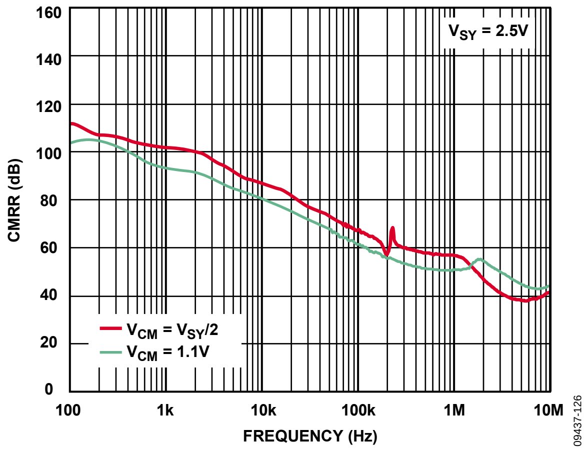


Figure 27. CMRR vs. Frequency

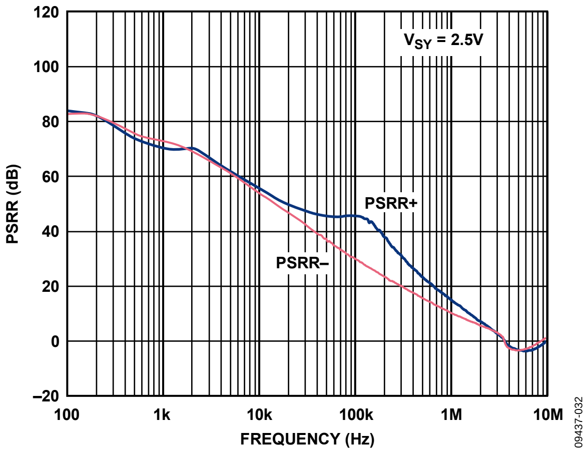


Figure 28. PSRR vs. Frequency

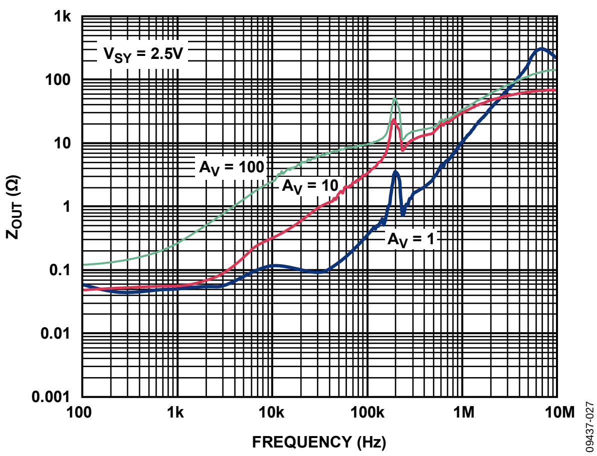


Figure 29. Output Impedance vs. Frequency

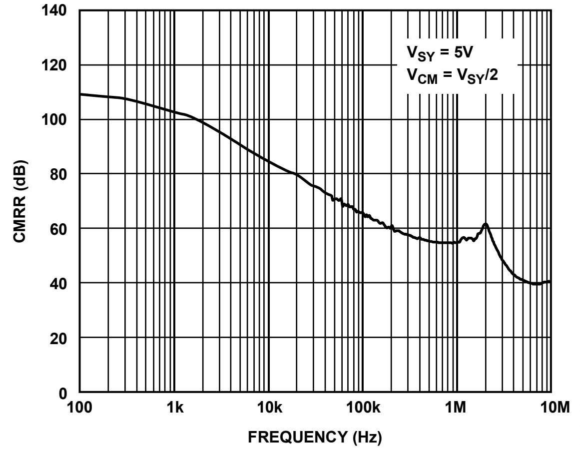


Figure 30. CMRR vs. Frequency

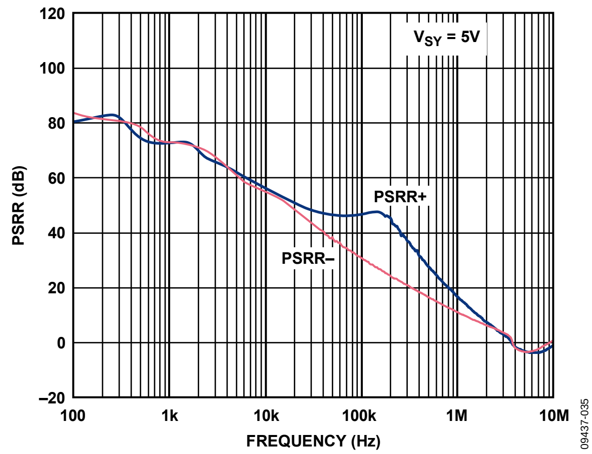


Figure 31. PSRR vs. Frequency

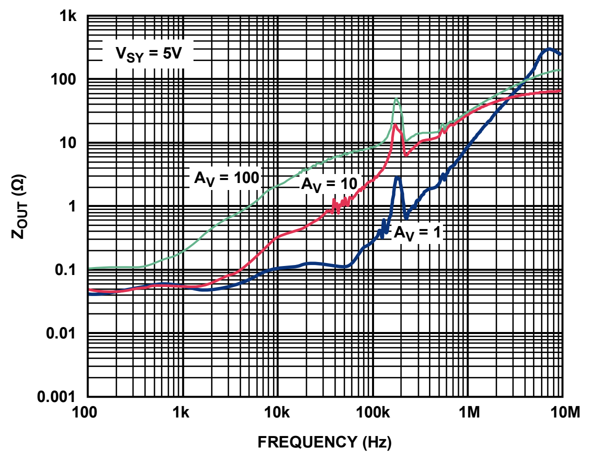


Figure 32. Output Impedance vs. Frequency

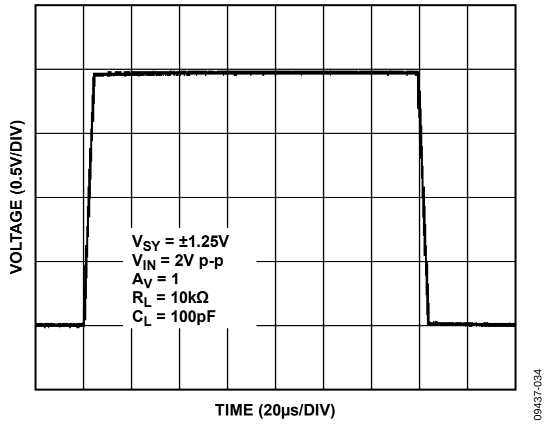


Figure 33. Large Signal Transient Response

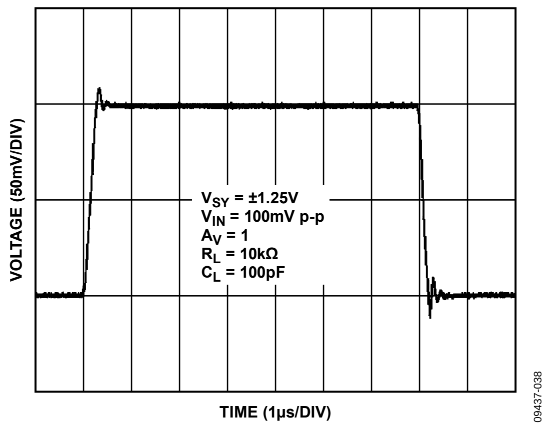


Figure 34. Small Signal Transient Response

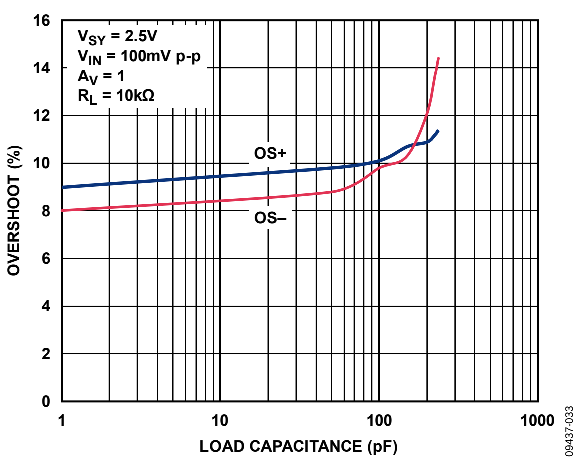


Figure 35. Small Signal Overshoot vs. Load Capacitance

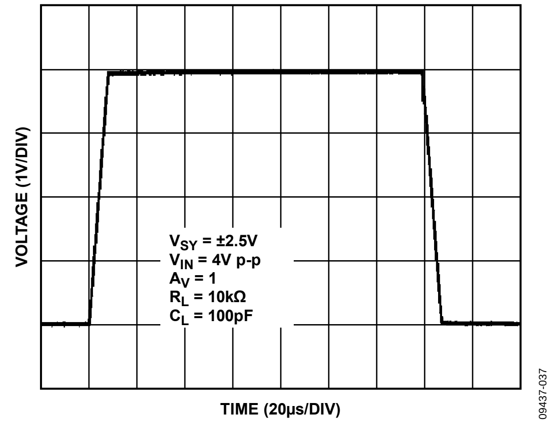


Figure 36. Large Signal Transient Response

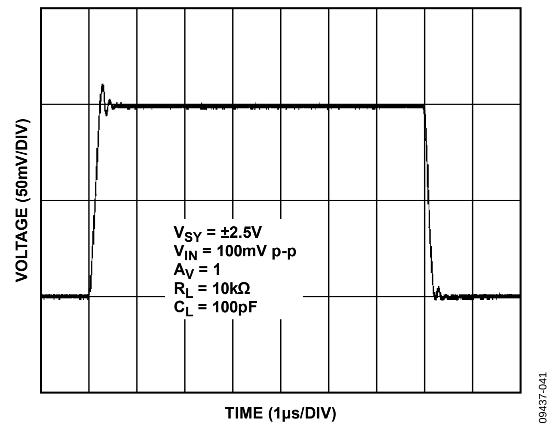


Figure 37. Small Signal Transient Response

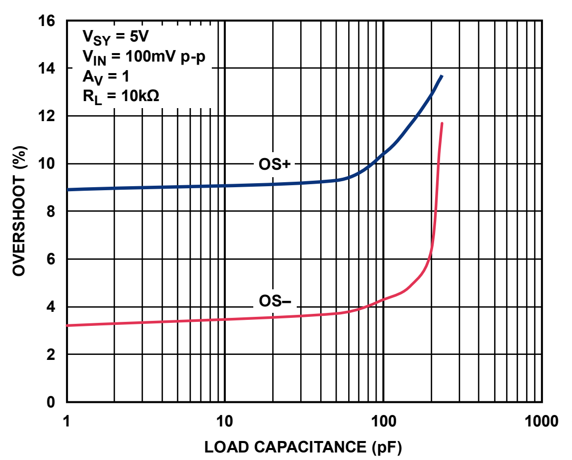


Figure 38. Small Signal Overshoot vs. Load Capacitance

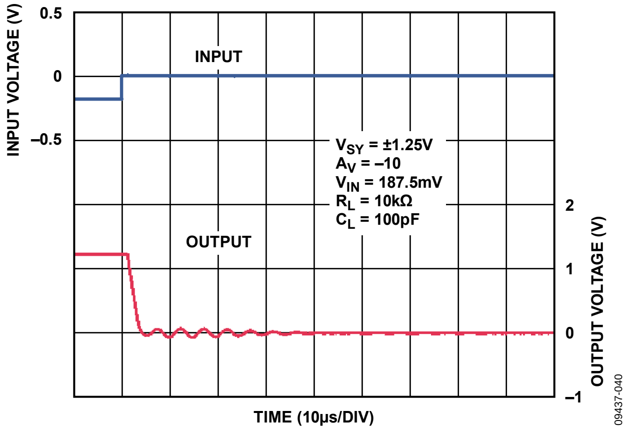


Figure 39. Positive Overload Recovery

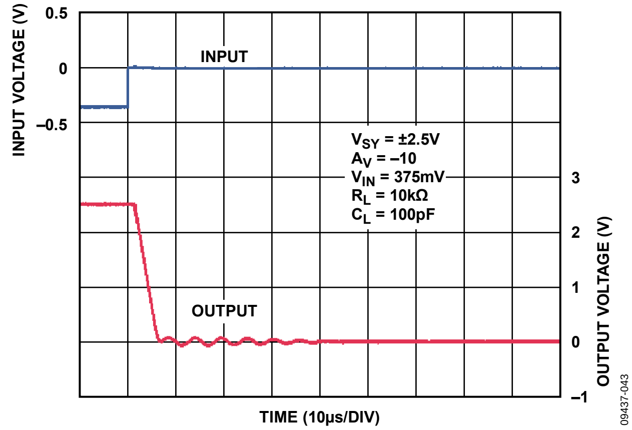


Figure 42. Positive Overload Recovery

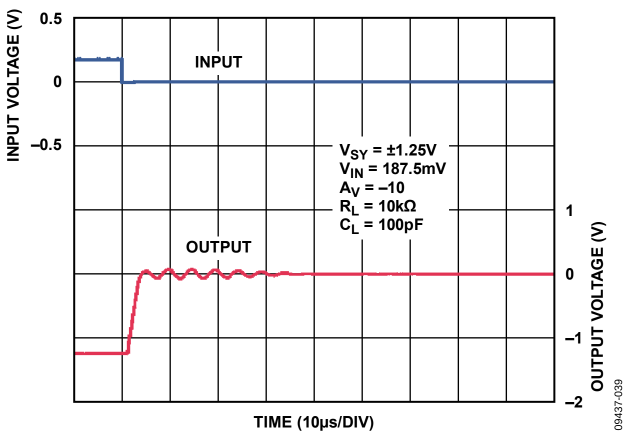


Figure 40. Negative Overload Recovery

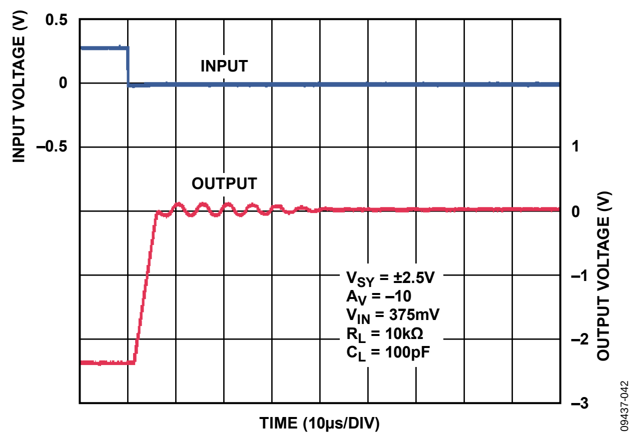


Figure 43. Negative Overload Recovery

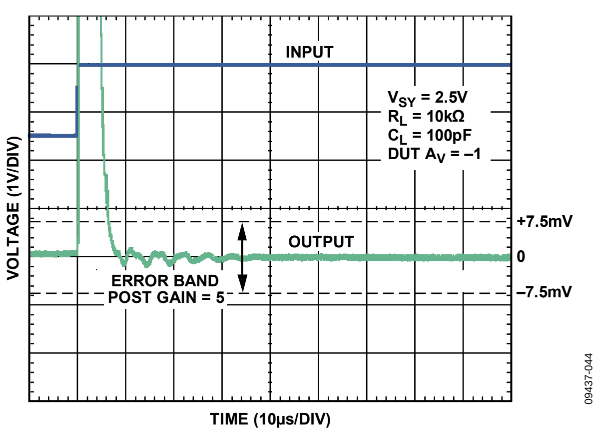


Figure 41. Positive Settling Time to 0.1%

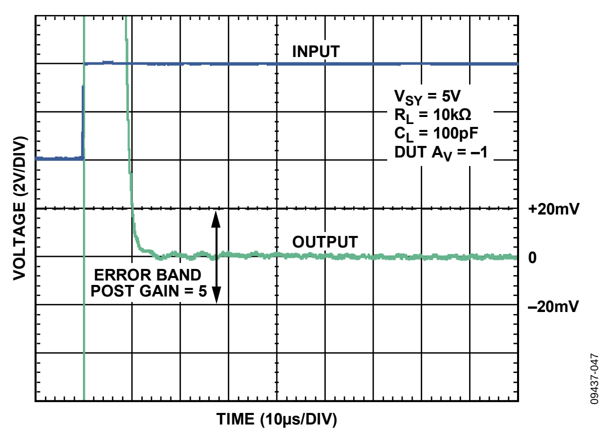


Figure 44. Positive Settling Time to 0.1%

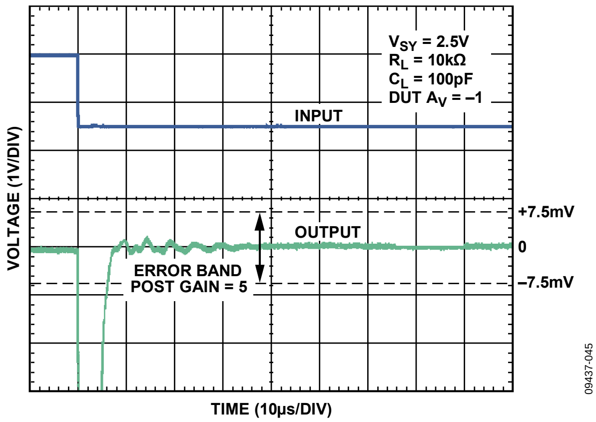


Figure 45. Negative Settling Time to 0.1%

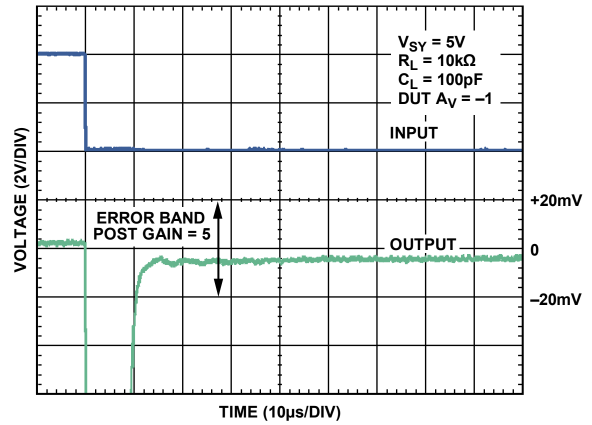


Figure 48. Negative Settling Time to 0.1%

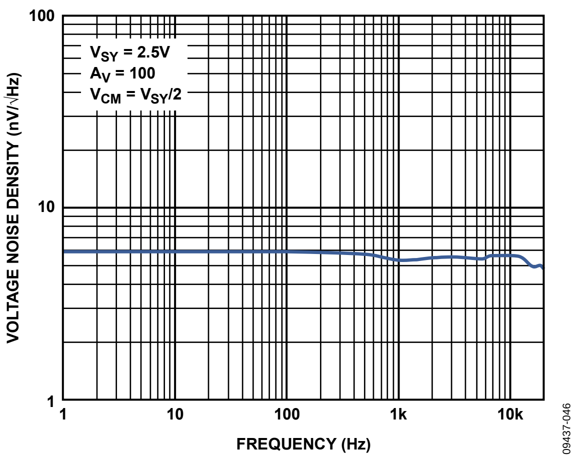


Figure 46. Voltage Noise Density vs. Frequency

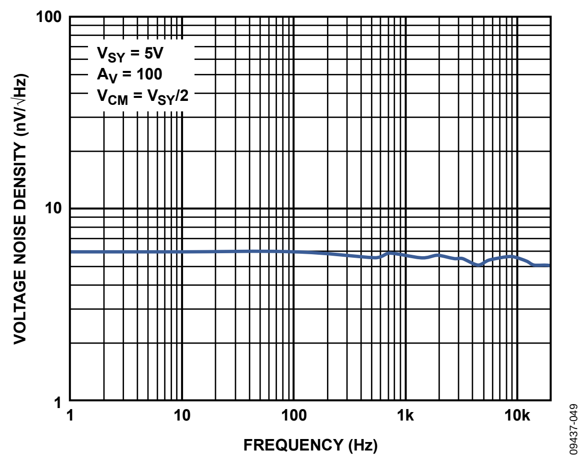


Figure 49. Voltage Noise Density vs. Frequency

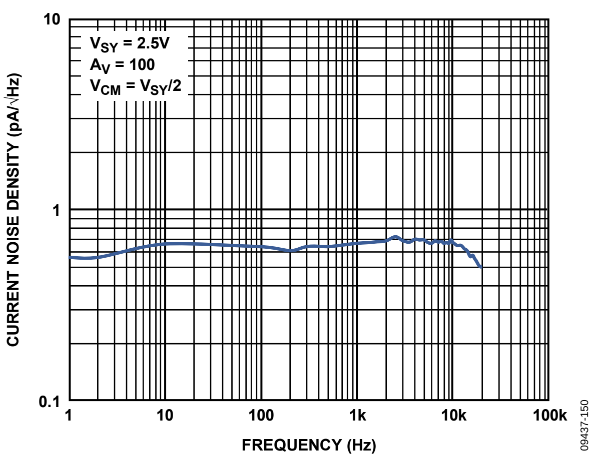


Figure 47. Current Noise Density vs. Frequency

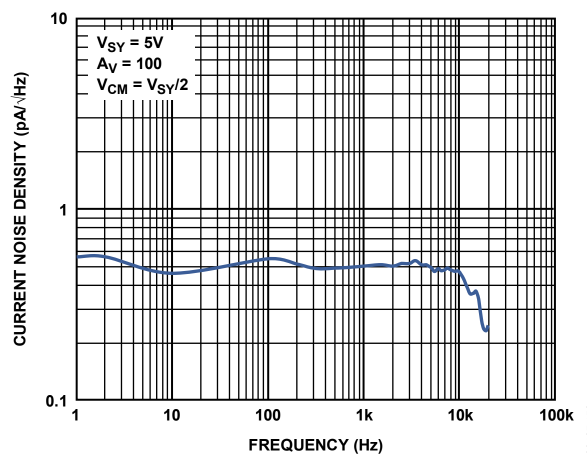


Figure 50. Current Noise Density vs. Frequency

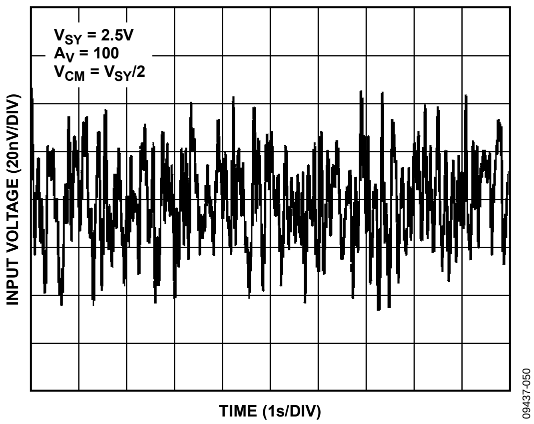


Figure 51. 0.1 Hz to 10 Hz Noise

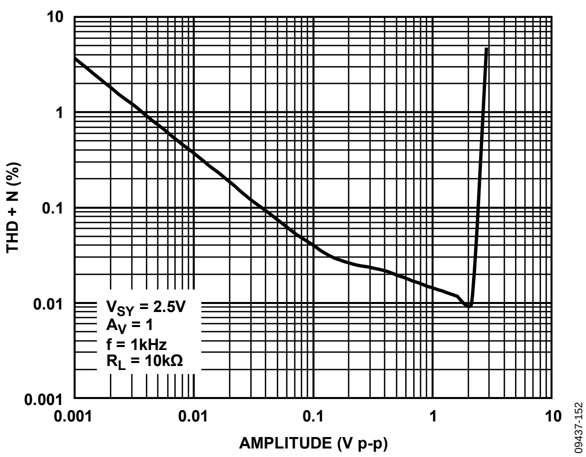


Figure 52. THD + Noise vs. Amplitude

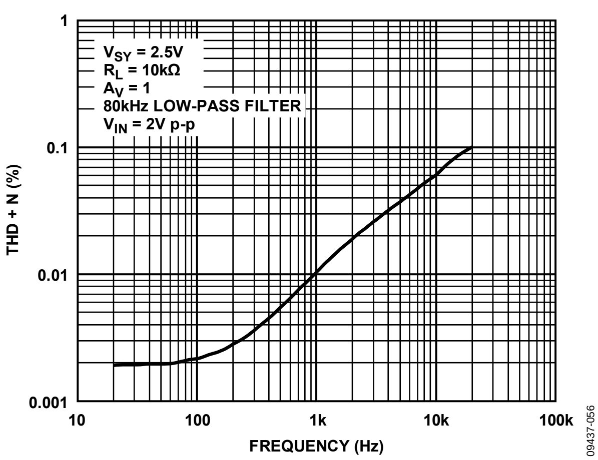


Figure 53. THD + Noise vs. Frequency

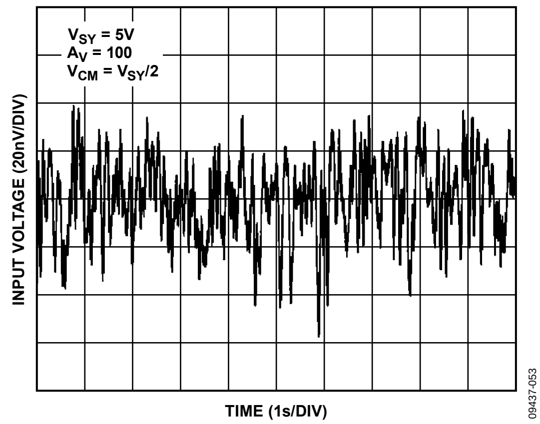


Figure 54. 0.1 Hz to 10 Hz Noise

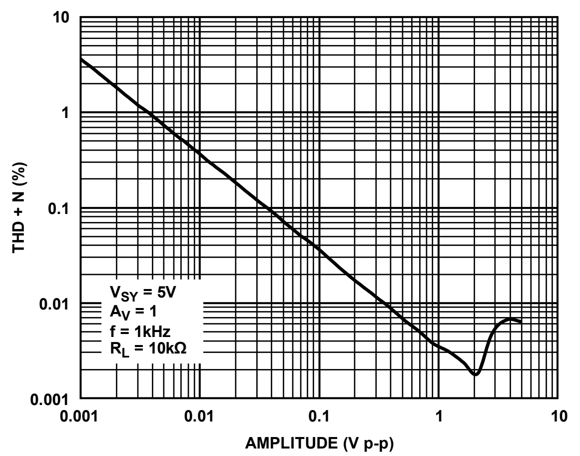


Figure 55. THD + Noise vs. Amplitude

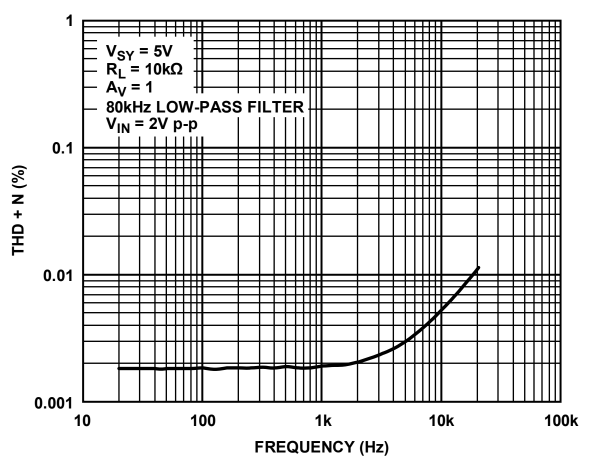


Figure 56. THD + Noise vs. Frequency

APPLICATIONS INFORMATION

The ADA4528-1 is a precision, ultralow noise, zero-drift operational amplifier that features a patented chopping technique. This chopping technique offers ultralow input offset voltage of 0.3 µV typical and input offset voltage drift of 0.002 µV/°C typical.

Offset voltage errors due to common-mode voltage swings and power supply variations are also corrected by the chopping technique, resulting in a typical CMRR figure of 158 dB and a PSRR figure of 150 dB at 2.5 V supply voltage. The ADA4528-1 has low broadband noise of 5.6 nV/√Hz (at f = 1 kHz, A_V = +100, V_{SY} = 2.5 V) and no 1/f noise component. These features are ideal for amplification of low level signals in dc or subhertz high precision applications.

INPUT PROTECTION

The ADA4528-1 has internal ESD protection diodes that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse-biased during normal operation. This protection scheme allows voltages as high as approximately 300 mV beyond the rails to be applied at the input of either terminal without causing permanent damage. Refer to Table 4 in the Absolute Maximum Ratings section.

When either input exceeds one of the supply rails by more than 300 mV, these ESD diodes become forward-biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. If the inputs are expected to be subject to overvoltage conditions, insert a resistor in series with each input to limit the input current to 10 mA maximum. However, consider the resistor thermal noise effect on the entire circuit.

At a 5 V supply voltage, the broadband voltage noise of the ADA4528-1 is approximately 6 nV/√Hz (at unity gain), and a 1 kΩ resistor has thermal noise of 4 nV/√Hz. Adding a 1 kΩ resistor increases the total noise by 30% root sum square (rss).

RAIL-TO-RAIL INPUT AND OUTPUT

The ADA4528-1 features rail-to-rail input and output with a supply voltage from 2.2 V to 5.5 V. Figure 57 shows the input and output waveforms of the ADA4528-1 configured as a unity-gain buffer with a supply voltage of ±2.5 V and a resistive load of 10 kΩ. With an input voltage of ±2.5 V, the ADA4528-1 allows the output to swing very close to both rails. Additionally, it does not exhibit phase reversal.

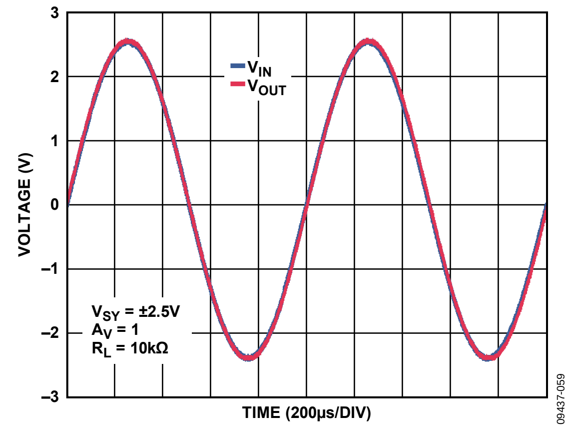


Figure 57. Rail-to Rail Input and Output

NOISE CONSIDERATIONS

1/f noise

1/f noise, also known as pink noise or flicker noise, is inherent in semiconductor devices and increases as frequency decreases. At low frequency, 1/f noise is a major noise contributor and causes a significant output voltage offset when amplified by the noise gain of the circuit. However, the ADA4528-1 eliminates the 1/f noise internally, thus making it an excellent choice for dc or subhertz high precision applications. The 0.1 Hz to 10 Hz amplifier voltage noise is only 97 nV p-p (A_V = +100) at 2.5 V of supply voltage.

The low frequency 1/f noise appears as a slow varying offset to the ADA4528-1 and is greatly reduced by the chopping technique. This allows the ADA4528-1 to have a much lower noise at dc and low frequency in comparison to standard low noise amplifiers that are susceptible to 1/f noise. Figure 46 and Figure 49 show the voltage noise density of the amplifier with no 1/f noise.

Source Resistance

The ADA4528-1 is one of the lowest noise zero drift amplifiers with 5.6 nV/√Hz of broadband noise at 1 kHz (V_{SY} = 2.5 V and A_V = +100) currently available in the industry. Therefore, it is important to consider the input source resistance of choice to maintain a total low noise. The total input referred broadband noise (e_N total) from any amplifier is primarily a function of three types of noise: input voltage noise, input current noise, and thermal (Johnson) noise from the external resistors. These uncorrelated noise sources can be summed up in a root sum squared (rss) manner by using the following equation:

$$e_N\ total = [e_n^2 + 4\,kTR_S + (i_n \times R_S)^2]^{1/2}$$

where:
e_n is the input voltage noise of the amplifier (V/√Hz).
I_n is the input current noise of the amplifier (A/√Hz).
R_S is the total input source resistance (Ω).
k is the Boltzmann's constant (1.38×10^{-23} J/K).
T is the temperature in Kelvin (K).

The total equivalent rms noise over a specific bandwidth is expressed as

$$e_{N,RMS} = e_N\ total\ \sqrt{BW}$$

where *BW* is the bandwidth in hertz.

This analysis is valid for broadband noise calculation. If the bandwidth of concern includes the chopping frequency, more complicated calculations must be made to include the effect of the noise spike at the chopping frequency (see Figure 60).

With a low source resistance of R_S < 1 kΩ, the voltage noise of the amplifier dominates. As source resistance increases, the thermal noise of R_S dominates. As the source resistance further increases, where R_S > 100 kΩ, the current noise becomes the main contributor of the total input noise. A good selection table for low noise op amps can be found in the AN-940 Application Note, *Low Noise Amplifier Selection Guide for Optimal Noise Performance.*

Voltage Noise Density with Different Gain Configurations

Figure 58 shows the voltage noise density vs. closed-loop gain of a zero-drift amplifier from Competitor A. The voltage noise density of the amplifier increases from 11 nV/√Hz to 21 nV/√Hz as closed-loop gain decreases from 1000 to 1. Figure 59 shows the voltage noise density vs. frequency of the ADA4528-1 for three different gain configurations. The ADA4528-1 offers lower input voltage noise density of 6 nV/√Hz to 7 nV/√Hz regardless of gain configurations.

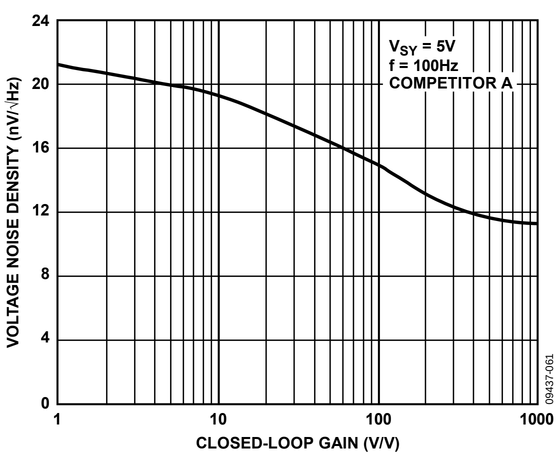


Figure 58. Competitor A: Voltage Noise Density vs. Closed-Loop Gain

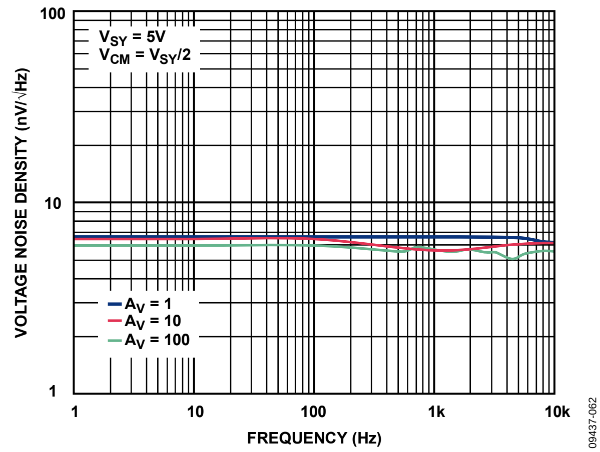


Figure 59. Voltage Noise Density vs. Frequency

Residual Ripple

Although the ACFB suppresses the chopping related ripples, there exists higher noise spectrum at the chopping frequency and its harmonics due to the remaining ripples. Figure 60 shows the voltage noise density of the ADA4528-1 configured in unity gain. A noise spike of 50 nV/√Hz can be seen at the chopping frequency of 200 kHz. This noise spike is significant when the op amp has a closed-loop frequency that is higher than the chopping frequency. To further suppress the noise to a desired level, it is recommended to have a post filter at the output of the amplifier.

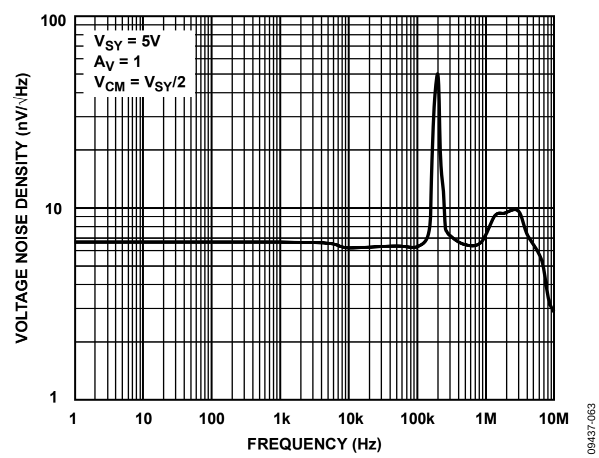


Figure 60. Voltage Noise Density

PRINTED CIRCUIT BOARD LAYOUT

The ADA4528-1 is a high precision device with ultralow offset voltage and noise. Therefore, care must be taken in the design of the printed circuit board (PCB) layout to achieve optimum performance of the ADA4528-1 at board level.

To avoid leakage currents, keep the surface of the board clean and free of moisture. Coating the board surface creates a barrier to moisture accumulation and reduces parasitic resistance on the board.

Properly bypassing the power supplies and keeping the supply traces short minimizes power supply disturbances caused by output current variation. Connect bypass capacitors as close as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at a distance of at least 5 mm from supply lines to minimize coupling.

A potential source of offset error is the Seebeck voltage on the circuit board. The Seebeck voltage occurs at the junction of two dissimilar metals and is a function of the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. Figure 61 shows a cross section of a surface-mount component soldered to a PCB. A variation in temperature across the board (where $T_{A1} \neq T_{A2}$) causes a mismatch in the Seebeck voltages at the solder joints, thereby resulting in thermal voltage errors that degrade the performance of the ultralow offset voltage of the ADA4528-1.

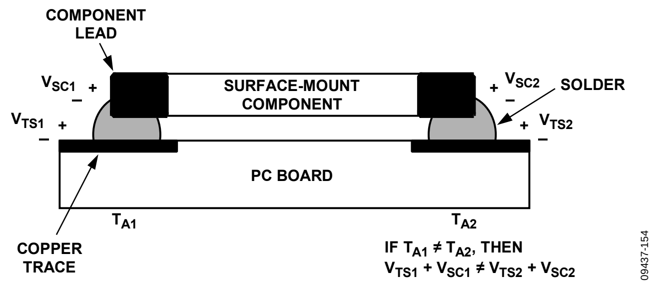


Figure 61. Mismatch in Seebeck Voltages Causes Seebeck Voltage Error

To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Where possible, the input signal paths should contain matching numbers and types of components to match the number and type of thermocouple junctions. For example, dummy components, such as zero value resistors, can be used to match the thermoelectric error source (real resistors in the opposite input path). Place matching components in close proximity and orient them in the same manner to ensure equal Seebeck voltages, thus cancelling thermal errors. Additionally, use leads that are of equal length to keep thermal conduction in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

It is highly recommended to use a ground plane. A ground plane helps distribute heat throughout the board, maintains a constant temperature across the board, and reduces EMI noise pickup.

OUTLINE DIMENSIONS

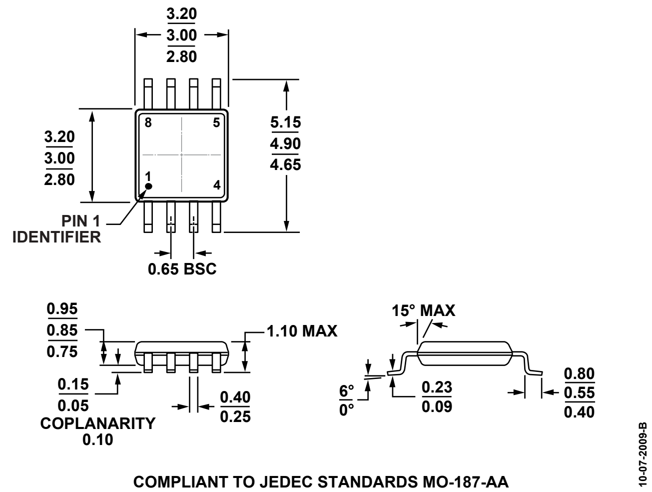


Figure 62. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

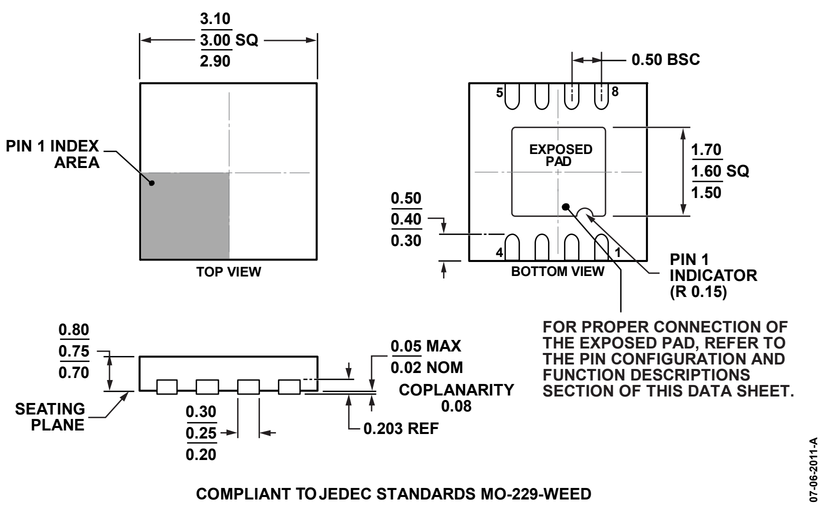


Figure 63.8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4528-1ARMZ	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2R
ADA4528-1ARMZ-R7	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2R
ADA4528-1ARMZ-RL	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2R
ADA4528-1ACPZ-R7	–40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-12	A2R
ADA4528-1ACPZ-RL	–40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-12	A2R

[1] Z = RoHS Compliant Part.

NOTES

NOTES