High IP3, 10 MHz to 6 GHz, Active Mixer

Data Sheet

ADL5801

FEATURES

- **Broadband upconverter/downconverter**
- **Power conversion gain of 1.8 dB**
- **Broadband RF, LO, and IF ports**
- **SSB noise figure (NF) of 9.75 dB**
- **Input IP3: 28.5 dBm**
- **Input P1dB: 13.3 dBm**
- **Typical LO drive: 0 dBm**
- **Single-supply operation: 5 V at 130 mA**
- **Adjustable bias for low power operation**
- **Exposed paddle, 4 mm × 4 mm, 24-lead LFCSP package**

APPLICATIONS

- **Cellular base station receivers**
- **Radio link downconverters**
- **Broadband block conversion**
- **Instrumentation**

FUNCTIONAL BLOCK DIAGRAM

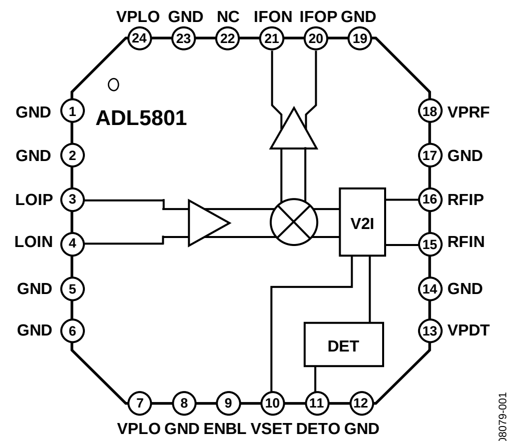

Figure 1.

GENERAL DESCRIPTION

The ADL5801 uses a high linearity, doubly balanced, active mixer core with integrated LO buffer amplifier to provide high dynamic range frequency conversion from 10 MHz to 6 GHz. The mixer benefits from a proprietary linearization architecture that provides enhanced input IP3 performance when subject to high input levels. A bias adjust feature allows the input linearity, SSB noise figure, and dc current to be optimized using a single control pin. An optional input power detector is provided for adaptive bias control. The high input linearity allows the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in degradation in dynamic performance. The adaptive bias feature allows the part to provide high input IP3 performance when presented with large blocking signals. When blockers are removed, the ADL5801 can automatically bias down to provide low noise figure and low power consumption.

The balanced active mixer arrangement provides superb LO-to-RF and LO-to-IF leakage, typically better than −40 dBm. The IF outputs are designed to provide a typical voltage conversion gain of 7.8 dB when loaded into a 200 Ω load. The broad frequency range of the open-collector IF outputs allows the ADL5801 to be applied as an upconverter for various transmit applications.

The ADL5801 is fabricated using a SiGe high performance IC process. The device is available in a compact 4 mm × 4 mm, 24-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. C **Document Feedback**

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Technical Support **www.analog.com**

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2/10—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{RF} = 900 MHz, f_{LO} = (f_{RF} − 153 MHz), LO power = 0 dBm, Z_0[1] = 50 Ω, VSET = 3.6 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		12		dB
Input Impedance			50		Ω
RF Frequency Range		10		6000	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		230		Ω
IF Frequency Range	Can be matched externally to 3000 MHz	LF		600	MHz
DC Bias Voltage[2]	Externally generated	4.75	V_S	5.25	V
LO INTERFACE					
LO Power		−10	0	+10	dBm
Return Loss			15		dB
Input Impedance			50		Ω
LO Frequency Range		10		6000	MHz
POWER INTERFACE					
Supply Voltage		4.75	5	5.25	V
Quiescent Current	Resistor programmable		130	200	mA
Disable Current	ENBL pin high to disable the device		50		mA
Disable Voltage	ENBL pin high to disable the device	2.5		5	V
Enable Voltage	ENBL pin low to enable the device	0		1.8	V
Enable Time	Time from ENBL pin low to enable		182		ns
Disable Time	Time from ENBL pin high to disable		28		ns
DYNAMIC PERFORMANCE at f_{RF} = 900 MHz/1900 MHz[3]					
Power Conversion Gain[4]	f_{RF} = 900 MHz		1.8		dB
	f_{RF} = 1900 MHz		1.8		dB
Voltage Conversion Gain[5]	f_{RF} = 900 MHz		7.8		dB
	f_{RF} = 1900 MHz		7.8		dB
SSB Noise Figure	f_{CENT} = 900 MHz, VSET = 2.0 V		9.75		dB
	f_{CENT} = 1900 MHz, VSET = 2.0 V		11.5		dB
SSB Noise Figure Under Blocking[6]	f_{CENT} = 900 MHz		19.5		dB
	f_{CENT} = 1900 MHz		20		dB
Input Third-Order Intercept[7]	f_{CENT} = 900 MHz		28.5		dBm
	f_{CENT} = 1900 MHz		26.4		dBm
Input Second-Order Intercept[8]	f_{CENT} = 900 MHz		63		dBm
	f_{CENT} = 1900 MHz		49.7		dBm
Input 1 dB Compression Point	f_{RF} = 900 MHz		13.3		dBm
	f_{RF} = 1900 MHz		12.7		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−27		dBm
LO-to-RF Input Leakage			−30		dBm
RF-to-IF Output Isolation			−35		dBc
IF/2 Spurious[9]	0 dBm input power, f_{RF} = 900 MHz		−67.5		dBc
	0 dBm input power, f_{RF} = 1900 MHz		−53		dBc
IF/3 Spurious[9]	0 dBm input power, f_{RF} = 900 MHz		−65.5		dBc
	0 dBm input power, f_{RF} = 1900 MHz		−72.6		dBc

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE at f_{RF} = 2500 MHz[10]					
Power Conversion Gain[11]			−0.1		dB
Voltage Conversion Gain[5]			−6.1		dB
SSB Noise Figure	f_{CENT} = 2500 MHz, VSET = 2.0 V		10.6		dB
Input Third-Order Intercept[12]	f_{CENT} = 2500 MHz		25.5		dBm
Input Second-Order Intercept[13]	f_{CENT} = 2500 MHz		45.3		dBm
Input 1 dB Compression Point	f_{CENT} = 2500 MHz		13.8		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−31.5		dBm
LO-to-RF Input Leakage			−31.2		dBm
RF-to-IF Output Isolation			−42.5		dBc
IF/2 Spurious[9]	0 dBm input power, f_{RF} = 2600 MHz		−50.6		dBc
IF/3 Spurious[9]	0 dBm input power, f_{RF} = 2600 MHz		−59.8		dBc
DYNAMIC PERFORMANCE at f_{RF} = 3500 MHz[14]					
Power Conversion Gain[15]			−0.44		dB
Voltage Conversion Gain[5]			−6.44		dB
SSB Noise Figure	f_{CENT} = 3500 MHz, VSET = 3.6 V		15.8		dB
Input Third-Order Intercept[7]	f_{CENT} = 3500 MHz, VSET = 3.6 V		26.5		dBm
Input Second-Order Intercept[8]	f_{CENT} = 3500 MHz, VSET = 3.6 V		42.3		dBm
Input 1 dB Compression Point			12.5		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−30.2		dBm
LO-to-RF Input Leakage			−29.4		dBm
RF-to-IF Output Isolation			−29.7		dBc
IF/2 Spurious[9]	0 dBm input power, f_{RF} = 3800 MHz		−47.1		dBc
IF/3 Spurious[9]	0 dBm input power, f_{RF} = 3800 MHz		−57.8		dBc
DYNAMIC PERFORMANCE at f_{RF} = 5500 MHz[16]					
Power Conversion Gain[17]			0.8		dB
Voltage Conversion Gain[5]			−5.2		dB
SSB Noise Figure	f_{CENT} = 5500 MHz, VSET = 3.6 V		16.2		dB
Input Third-Order Intercept[7]	f_{CENT} = 5500 MHz, VSET = 3.6 V		22.7		dBm
Input Second-Order Intercept[8]	f_{CENT} = 5500 MHz, VSET = 3.6 V		35.4		dBm
Input 1 dB Compression Point			11.3		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−42.6		dBm
LO-to-RF Input Leakage			−28.9		dBm
RF-to-IF Output Isolation			−46.7		dBc
IF/2 Spurious[9]	0 dBm input power, f_{RF} = 5800 MHz		−44		dBc
IF/3 Spurious[9]	0 dBm input power, f_{RF} = 5800 MHz		−47		dBc
DYNAMIC PERFORMANCE at f_{IF} = 900 MHz[18]					
Power Conversion Gain[19]			0		dB
Voltage Conversion Gain[5]			−6		dB
SSB Noise Figure	f_{IF} = 900 MHz, f_{RF} = 250 MHz, VSET = 2.0 V		10.6		dB
Output Third-Order Intercept[20]	f_{CENT} = 153 MHz, VSET = 3.6 V		30.6		dBm
Output Second-Order Intercept[21]	f_{CENT} = 153 MHz, VSET = 3.6 V		68.7		dBm
Output 1 dB Compression Point			11.1		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−33.8		dBm
LO-to-RF Input Leakage			−33.4		dBm
IF/2 Spurious[9]	0 dBm input power, f_{RF} = 140 MHz, f_{IF} = 806 MHz		−62.6		dBc
IF/3 Spurious[9]	0 dBm input power, f_{RF} = 140 MHz, f_{IF} = 806 MHz		−68.9		dBc

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE at f_{IF} = 2140 MHz[22]					
Power Conversion Gain[23]			−1.25		dB
Voltage Conversion Gain[5]			−7.25		dB
SSB Noise Figure	f_{IF} = 2140 MHz, f_{RF} = 190 MHz, VSET = 2.0 V		13.6		dB
Output Third-Order Intercept[24]	f_{CENT} = 170 MHz, VSET = 3.6 V		24		dBm
Output Second-Order Intercept[25]	f_{CENT} = 170 MHz, VSET = 3.6 V		70		dBm
Output 1 dB Compression Point			9.9		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−23.8		dBm
LO-to-RF Input Leakage			−33.2		dBm
IF/2 Spurious[9]	0 dBm input power, f_{RF} = 140 MHz, f_{IF} = 2210 MHz		−51.5		dBc

[1] Z_0 is the characteristic impedance assumed for all measurements and the PCB.
[2] Supply voltage must be applied from an external circuit through choke inductors
[3] V_S = 5 V, T_A = 25°C, f_{RF} = 900 MHz/1900 MHz, f_{LO} = (f_{RF} – 153 MHz), LO power = 0 dBm, Z_0[1]= 50 Ω, VSET = 3.8 V, unless otherwise noted.
[4] Excluding 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (TC1-1-13M+), and PCB loss.
[5] Z_{SOURCE} = 50 Ω, differential; Z_{LOAD} = 200 Ω differential; Z_{SOURCE} is the impedance of the source instrument; Z_{LOAD} is the load impedance at the output.
[6] f_{RF} = f_{CENT}, $f_{BLOCKER}$ = (f_{CENT} − 5) MHz, f_{LO} = (f_{CENT} − 153) MHz, blocker level = 0 dBm.
[7] f_{RF1} = (f_{CENT} − 1) MHz, f_{RF2} = (f_{CENT}) MHz, f_{LO} = (f_{CENT} – 153) MHz, each RF tone at −10 dBm.
[8] f_{RF1} = (f_{CENT}) MHz, f_{RF2} = (f_{CENT} + 100) MHz, f_{LO} = (f_{CENT} – 153) MHz, each RF tone at −10 dBm.
[9] For details, see the Spur Performance section.
[10] V_S = 5 V, T_A = 25°C, f_{RF} = 2500 MHz, f_{LO} = (f_{RF} – 211 MHz), LO power = 0 dBm, Z_0[1] = 50 Ω, VSET = 3.8 V, unless otherwise noted.
[11] Including 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (TC1-1-43M+ and TC1-1-13M+ respectively), and PCB loss.
[12] f_{RF1} = (f_{CENT} − 1) MHz, f_{RF2} = (f_{CENT}) MHz, f_{LO} = (f_{CENT} – 211) MHz, each RF tone at −10 dBm.
[13] f_{RF1} = (f_{CENT}) MHz, f_{RF2} = (f_{CENT} + 100) MHz, f_{LO} = (f_{CENT} – 211) MHz, each RF tone at −10 dBm
[14] V_S = 5 V, T_A = 25°C, f_{RF} = 3500 MHz, f_{LO} = (f_{RF} – 153 MHz), LO power = 0 dBm, Z_0[1] = 50 Ω, VSET = 3.6 V, unless otherwise noted.
[15] Including 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (3600BL14M050), and PCB loss.
[16] V_S = 5 V, T_A = 25°C, f_{RF} = 5500 MHz, f_{LO} = (f_{RF} – 153 MHz), LO power = 0 dBm, Z_0[1] = 50 Ω, VSET = 3.6 V, unless otherwise noted.
[17] Including 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (5400BL14B050), and PCB loss.
[18] V_S = 5 V, T_A = 25°C, f_{RF} = 153 MHz, f_{LO} = (f_{RF} + 900 MHz), LO power = 0 dBm, Z_0[1] = 50 Ω, VSET = 3.6 V, unless otherwise noted.
[19] Including 4:1 IF port transformer (TC4-14+), RF and LO transformers (TC1-1-13M+), and PCB loss.
[20] f_{RF1} = (f_{CENT} − 1) MHz, f_{RF2} = (f_{CENT}) MHz, f_{LO} = (f_{CENT} + 900 MHz), each RF tone at −10 dBm.
[21] f_{RF1} = (f_{CENT}) MHz, f_{RF2} = (f_{CENT} + 100) MHz, f_{LO} = (f_{CENT} + 900) MHz, each RF tone at −10 dBm.
[22] V_S = 5 V, T_A = 25°C, f_{RF} = 153MHz, f_{LO} = (f_{RF} + 2140 MHz), LO power = 0 dBm, Z_0[1] = 50 Ω, VSET = 4 V, unless otherwise noted.
[23] Including 4:1 IF port transformer (1850BL15B200), RF and LO port transformers (TC1-1-13M+), and PCB loss.
[24] f_{RF1} = (f_{CENT} − 1) MHz, f_{RF2} = (f_{CENT}) MHz, f_{LO} = (f_{CENT} + 2140 MHz), each RF tone at −10 dBm.
[25] f_{RF1} = (f_{CENT}) MHz, f_{RF2} = (f_{CENT} + 100) MHz, f_{LO} = (f_{CENT} + 2140) MHz, each RF tone at −10 dBm.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
VSET, ENBL	5.5 V
IFOP, IFON	5.5 V
RFIN Power	20 dBm
Internal Power Dissipation	1.2 W
θ_{JA} (Exposed Paddle Soldered Down)[1]	26.5°C/W
θ_{JC} (at Exposed Paddle)	8.7°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] As measured on the evaluation board. For details, see the Evaluation Board section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

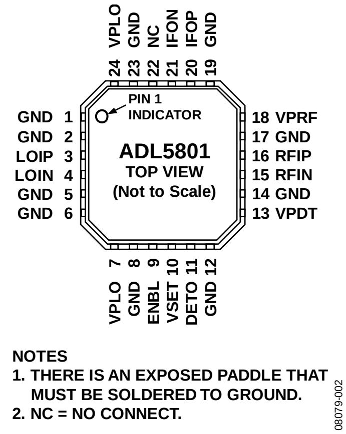

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 5, 6, 8, 12, 14, 17, 19, 23	GND	Device Common (DC Ground).
3, 4	LOIP, LOIN	Differential LO Input Terminal. Internally matched to 50 Ω. Must be ac-coupled.
7, 24	VPLO	Positive Supply Voltage for LO System.
9	ENBL	Device Enable. Pull high to disable the device; pull low to enable.
10	VSET	Input IP3 Bias Adjustment. The voltage presented to the VSET pin sets the internal bias of the mixer core and allows for adaptive control of the input IP3 and NF characteristics of the mixer core.
11	DETO	Detector Output. The DETO pin should be loaded with a capacitor to ground. The developed voltage is proportional to the rms input level. When the DETO output voltage is connected to the VSET input pin, the part auto biases and increases input IP3 performance when presented with large signal input levels.
13	VPDT	Positive Supply Voltage for Detector.
15, 16	RFIN, RFIP	Differential RF Input Terminal. Internally matched to 50 Ω differential input impedance. Must be ac-coupled.
18	VPRF	Positive Supply Voltage for RF Input System.
20, 21	IFOP, IFON	Differential IF Output Terminal. Bias must be applied through pull-up choke inductors or the center tap of the IF transformer.
22	NC	Not Connected.
	EPAD	The exposed paddle must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

DOWNCOVERTER MODE WITH A BROADBAND BALUN

V_S = 5 V, T_A = 25°C, VSET = 3.8 V, IF = 153 MHz, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

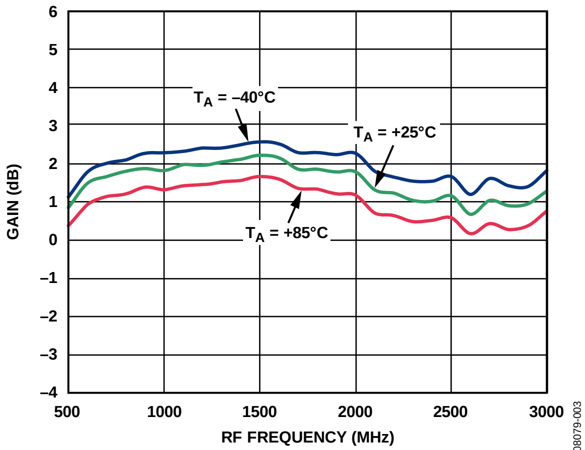

Figure 3. Power Conversion Gain vs. RF Frequency

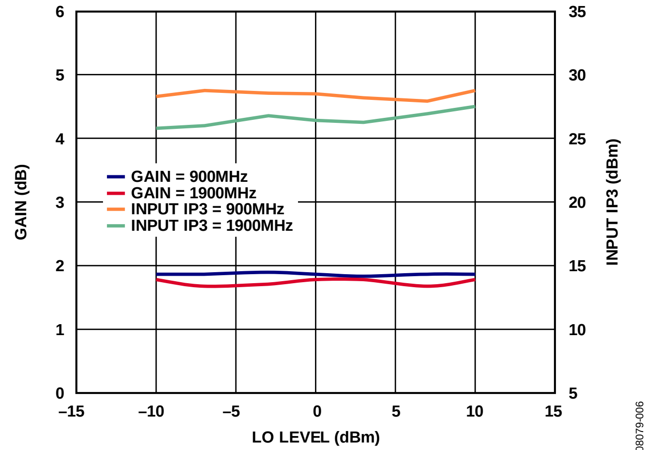

Figure 6. Power Conversion Gain and Input IP3 vs. LO Power

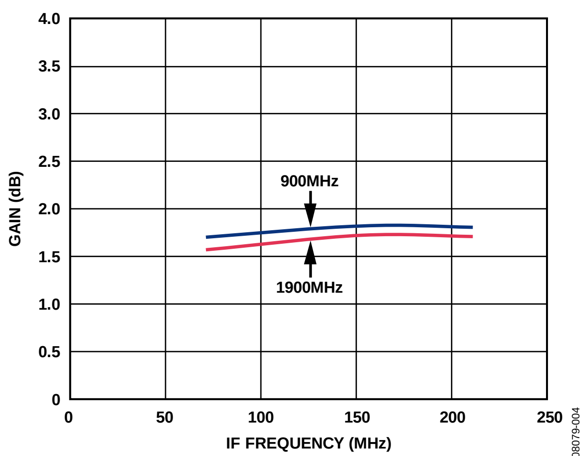

Figure 4. Power Conversion Gain vs. IF Frequency

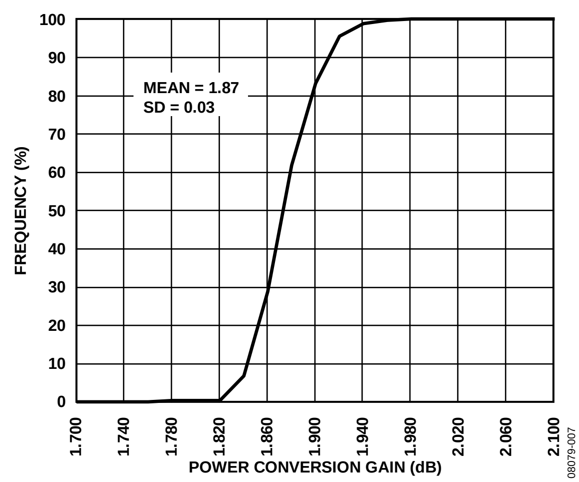

Figure 7. Power Conversion Gain Distribution

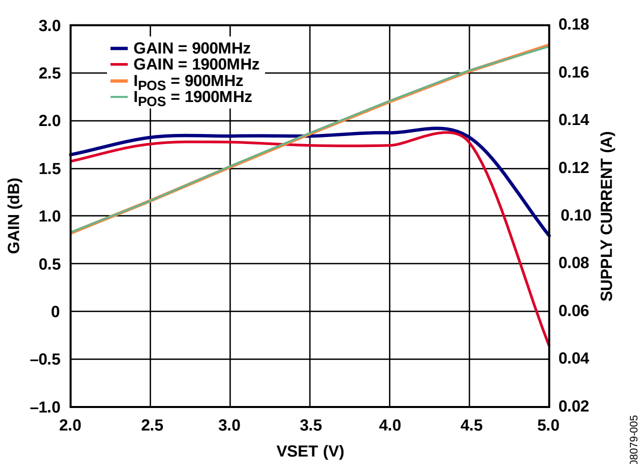

Figure 5. Power Conversion Gain and Supply Current vs. VSET

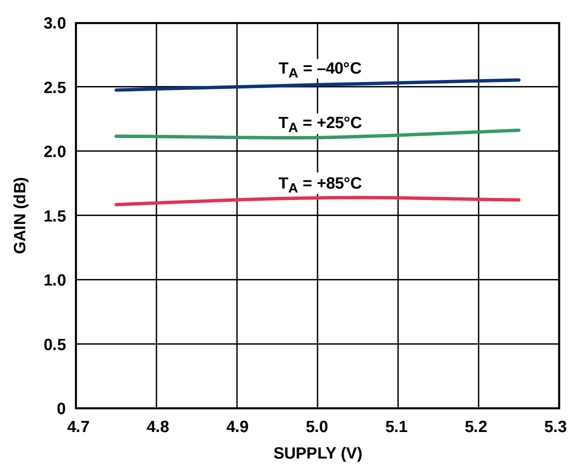

Figure 8. Power Conversion Gain vs. Supply Voltage

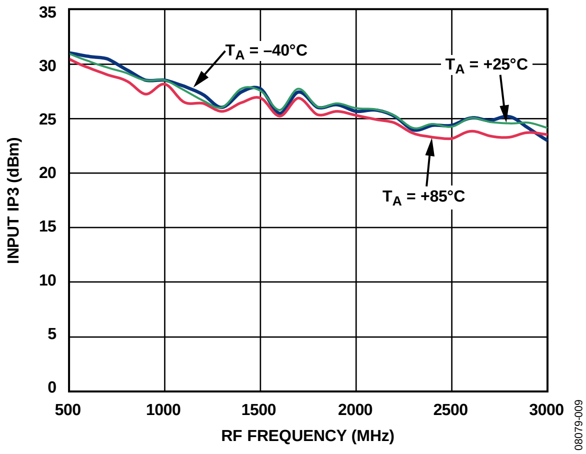

Figure 9. Input IP3 vs. RF Frequency

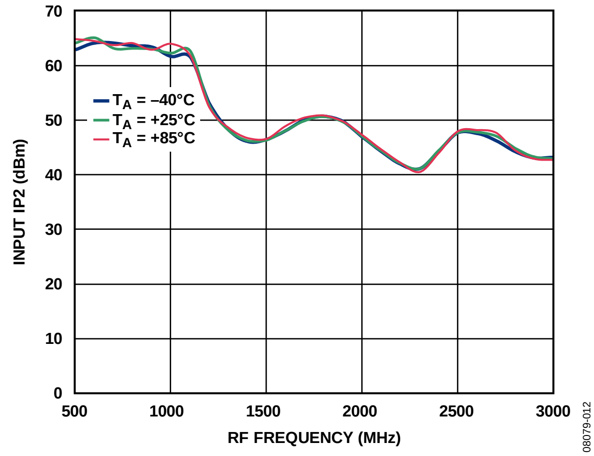

Figure 12. Input IP2 vs. RF Frequency

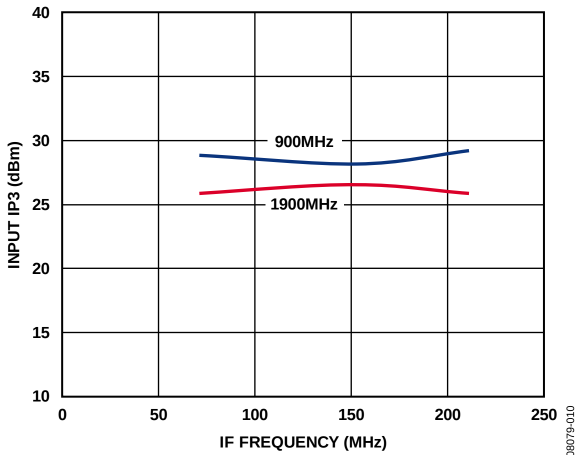

Figure 10. Input IP3 vs. IF Frequency

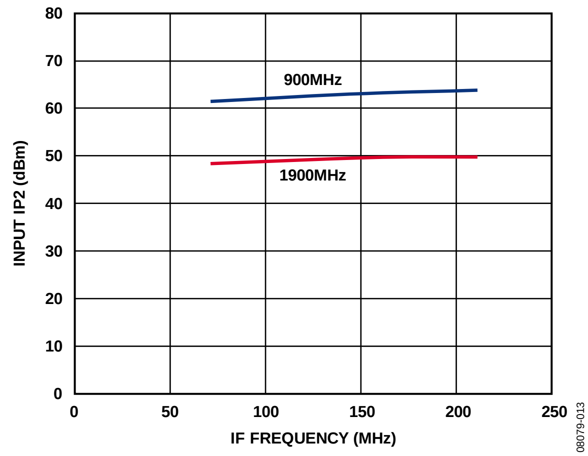

Figure 13. Input IP2 vs. IF Frequency

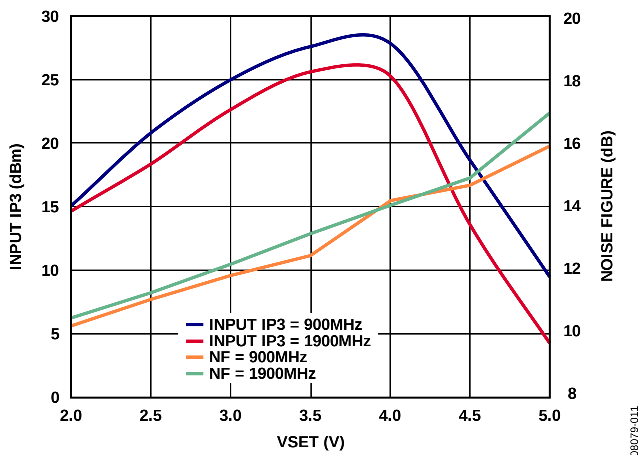

Figure 11. Input IP3 and Noise Figure vs. VSET

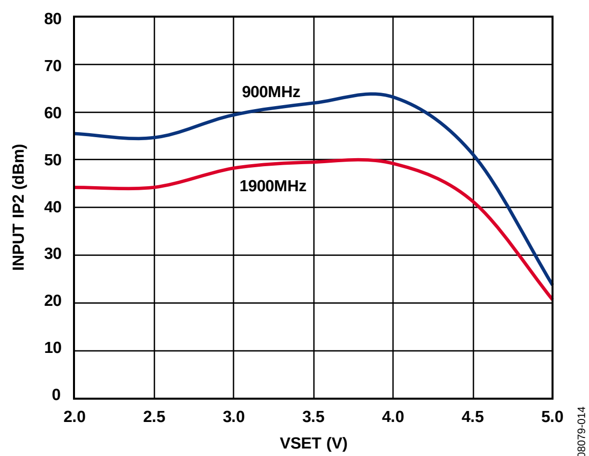

Figure 14. Input IP2 vs. VSET

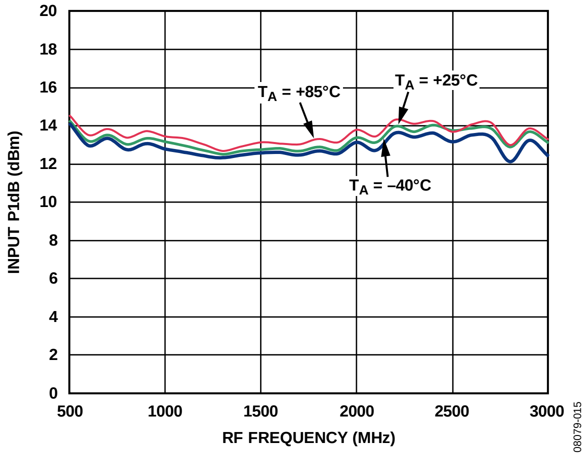

Figure 15. Input P1dB vs. RF Frequency

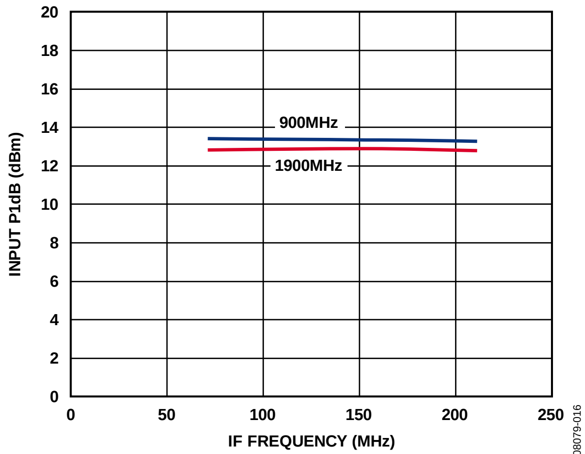

Figure 16. Input P1dB vs. IF Frequency

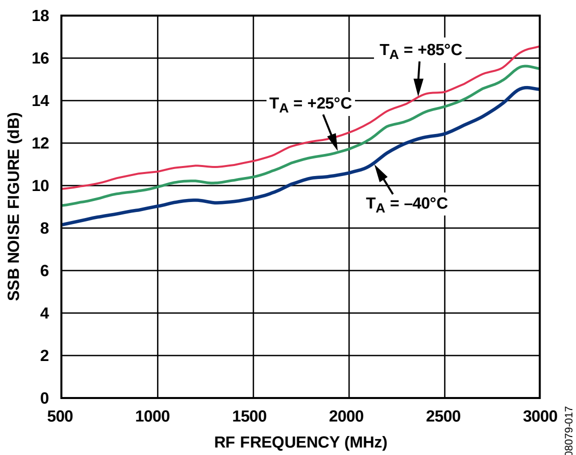

Figure 17. SSB Noise Figure vs. RF Frequency (VSET = 2.0 V)

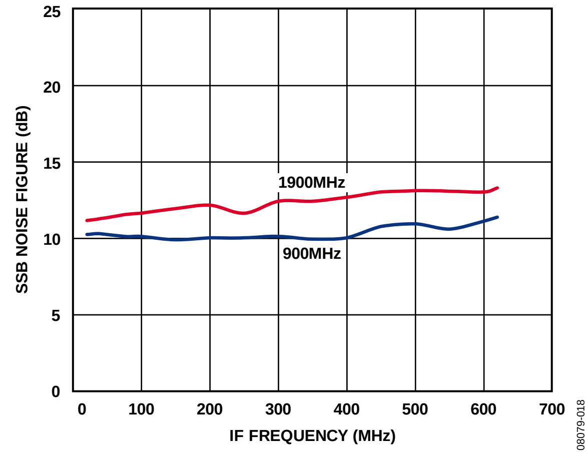

Figure 18. SSB Noise Figure vs. IF Frequency (VSET = 2.0 V)

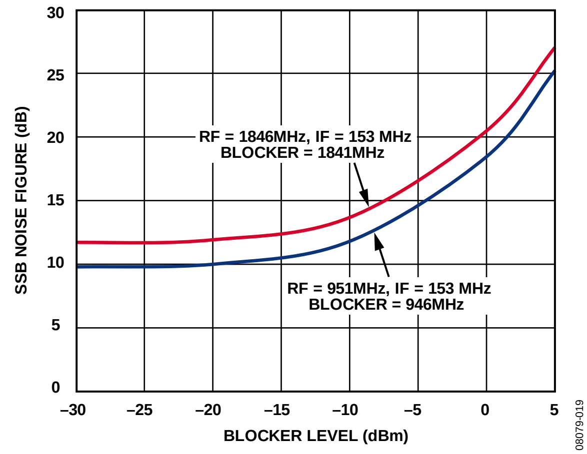

Figure 19. SSB Noise Figure vs. Blocker Level (VSET = 2.0 V)

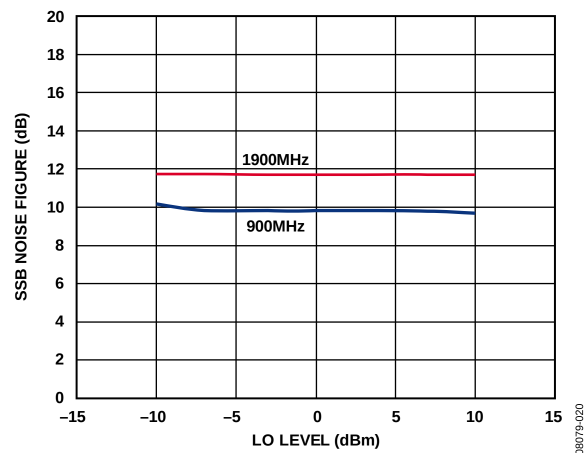

Figure 20. SSB Noise Figure vs. LO Power (VSET = 2.0 V)

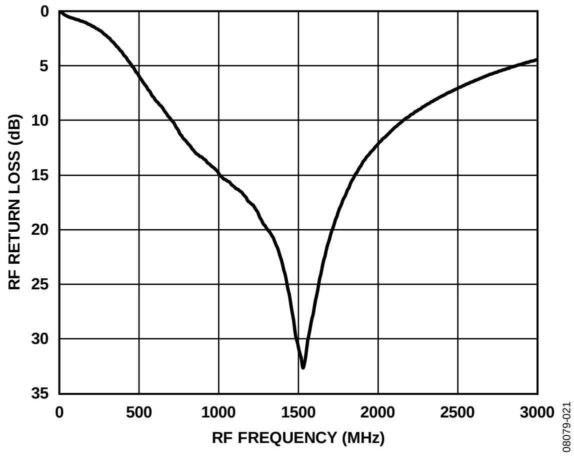

Figure 21. RF Return Loss vs. RF Frequency

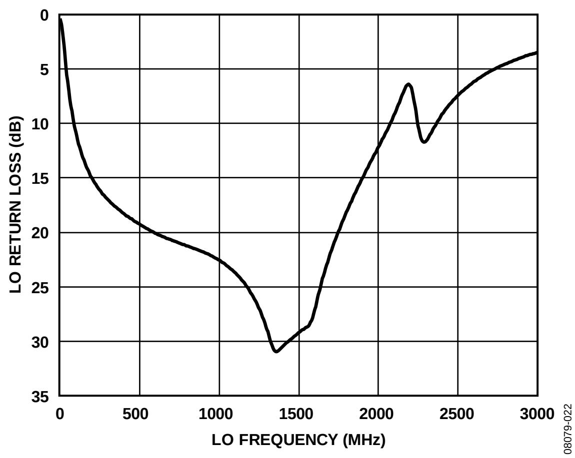

Figure 22. LO Return Loss vs. LO Frequency

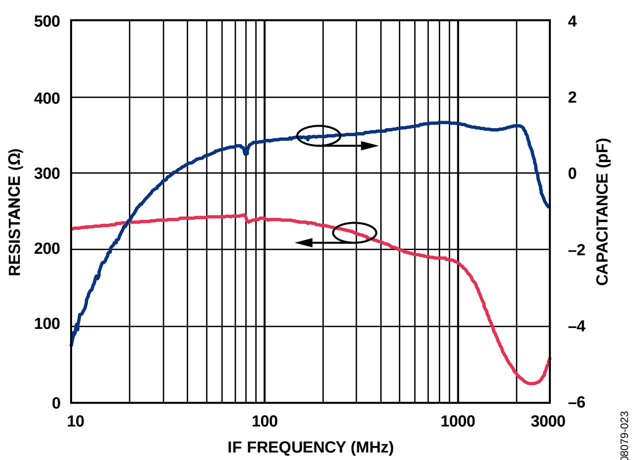

Figure 23. IF Differential Output Impedance (R Parallel C Equivalent)

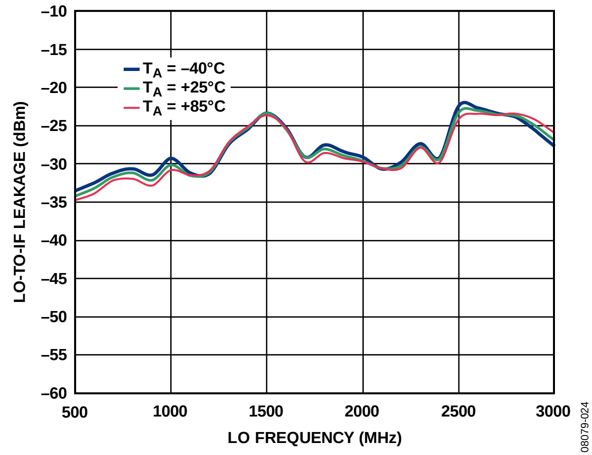

Figure 24. LO-to-IF Leakage vs. LO Frequency

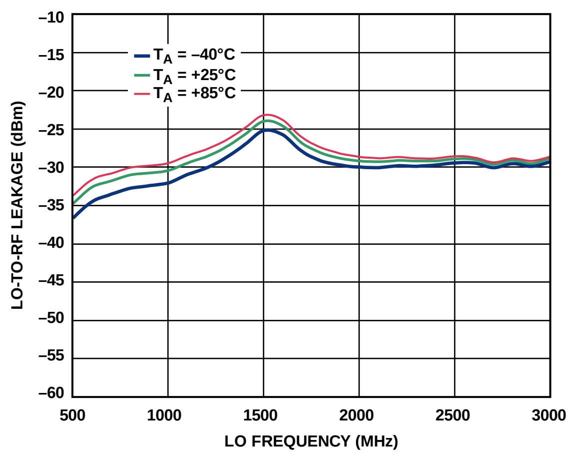

Figure 25. LO-to-RF Leakage vs. LO Frequency

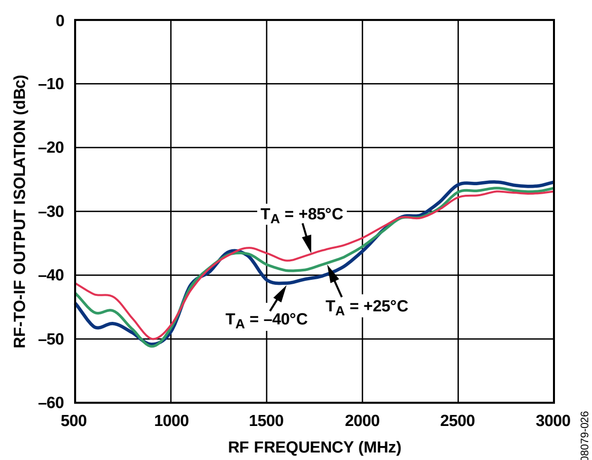

Figure 26. RF-to-IF Leakage vs. RF Frequency

DOWNCONVERTER MODE WITH A MINI-CIRCUITS® TC1-1-43M+ INPUT BALUN

V_S = 5 V, T_A = 25°C, VSET = 3.8 V, IF = 211 MHz, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-43M+, TC4-1W+) is included in the gain measurement.

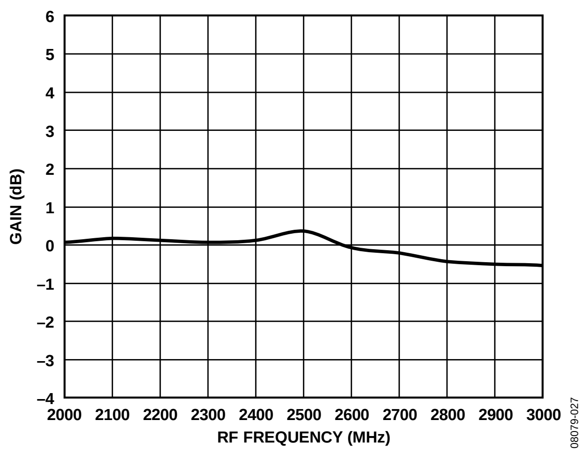

Figure 27. Power Conversion Gain vs. RF Frequency

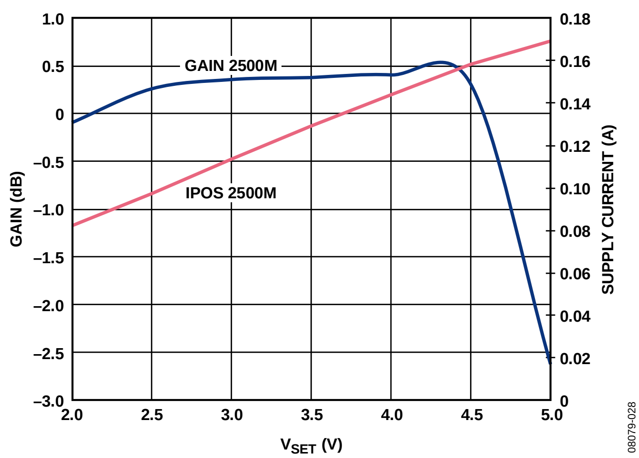

Figure 28. Power Conversion Gain and IPOS vs. V_{SET}

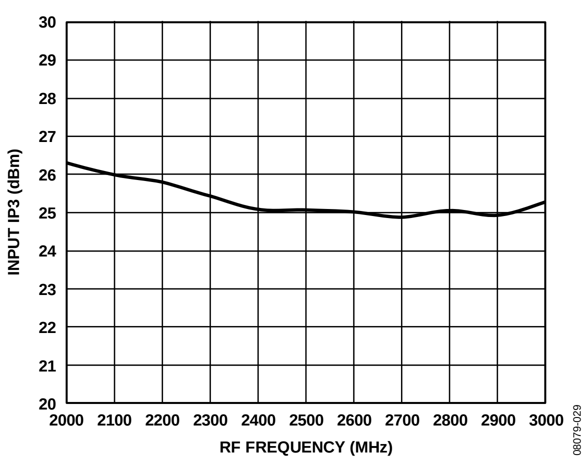

Figure 29. Input IP3 vs. RF Frequency

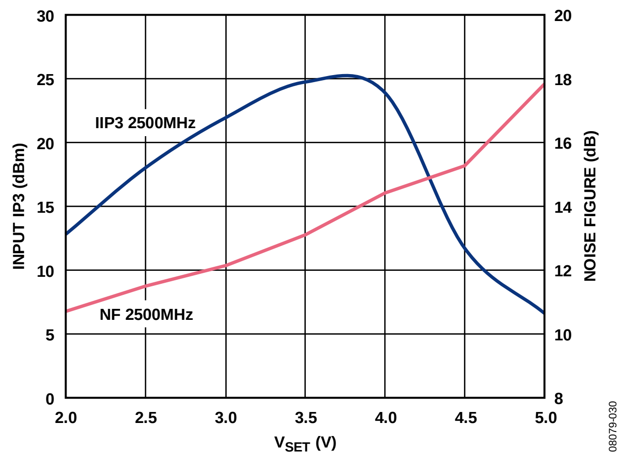

Figure 30. Input IP3 and Noise Figure vs. V_{SET}

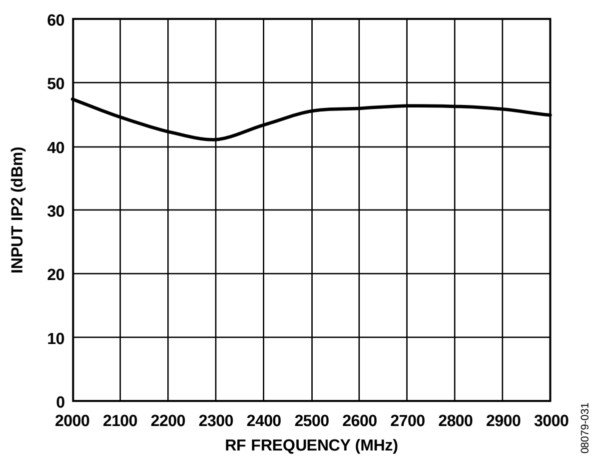

Figure 31. Input IP2 vs. RF Frequency

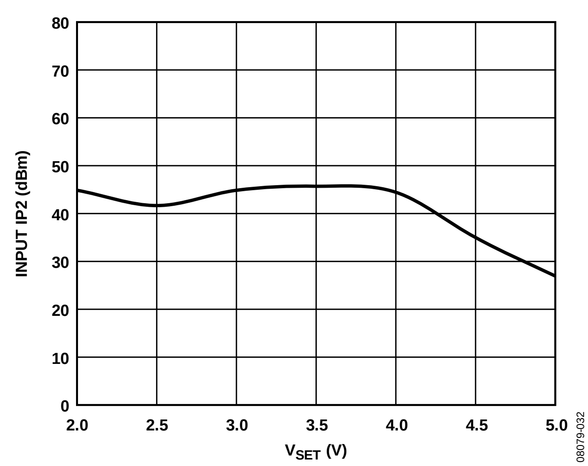

Figure 32. Input IP2 vs. V_{SET}

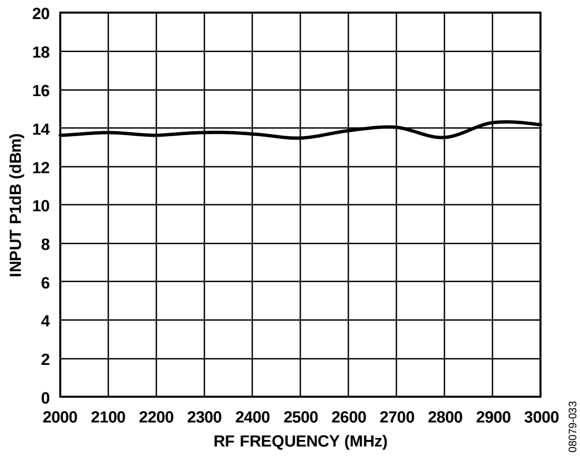

Figure 33. Input P1dB vs. RF Frequency

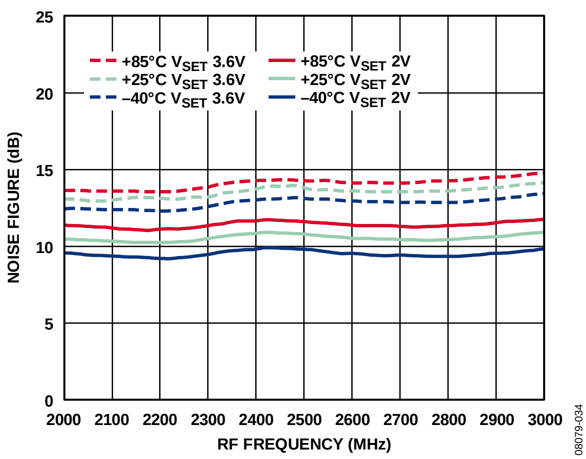

Figure 34. Noise Figure vs. RF Frequency

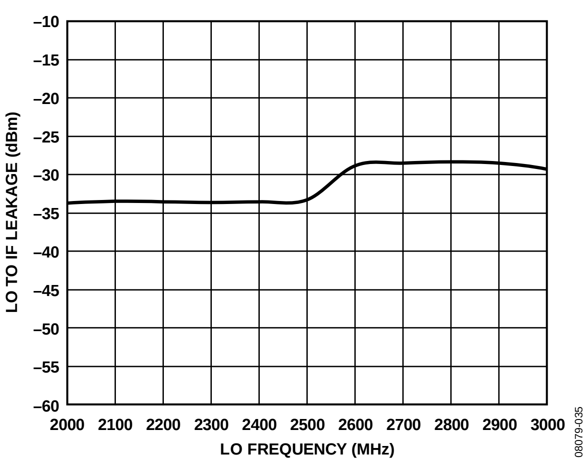

Figure 35. LO to IF Leakage vs. LO Frequency

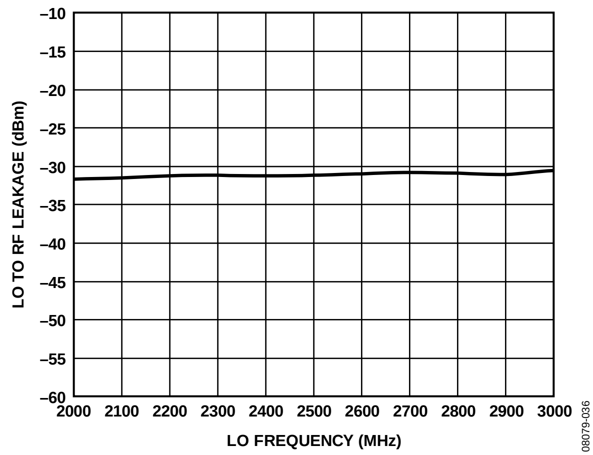

Figure 36.LO to RF Leakage vs. LO Frequency

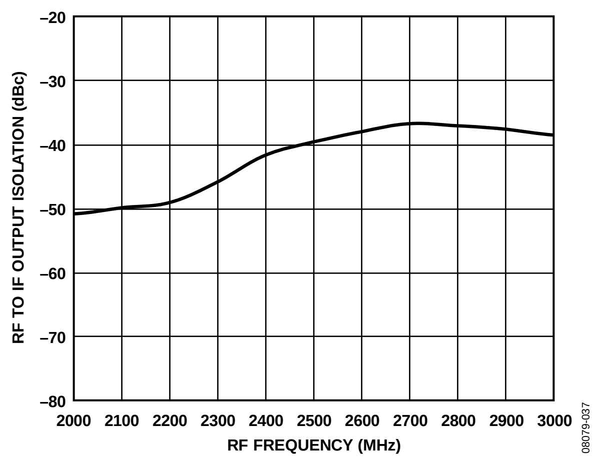

Figure 37. RF to IF Output Isolation vs. RF Frequency

DOWNCONVERTER MODE WITH A JOHANSON 3.5 GHZ INPUT BALUN

V_S = 5 V, T_A = 25°C, VSET = 3.6 V, IF = 153 MHz, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (3600BL14M050, TC4-1W+) is included in the gain measurement.

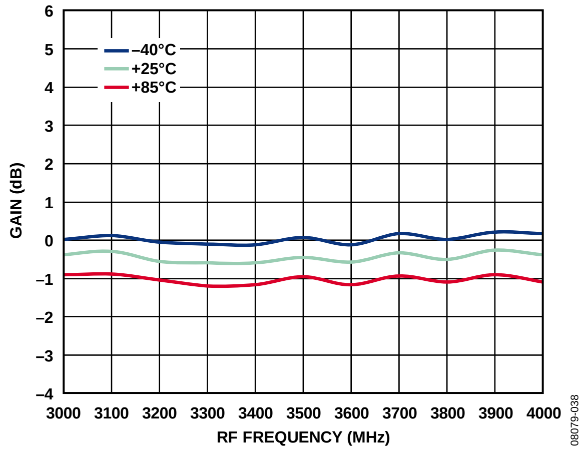

Figure 38. Power Conversion Gain vs. RF Frequency

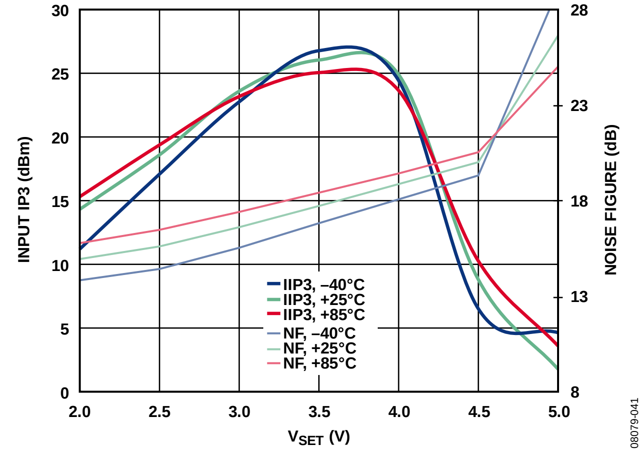

Figure 41. Input IP3 and Noise Figure vs. V_{SET}

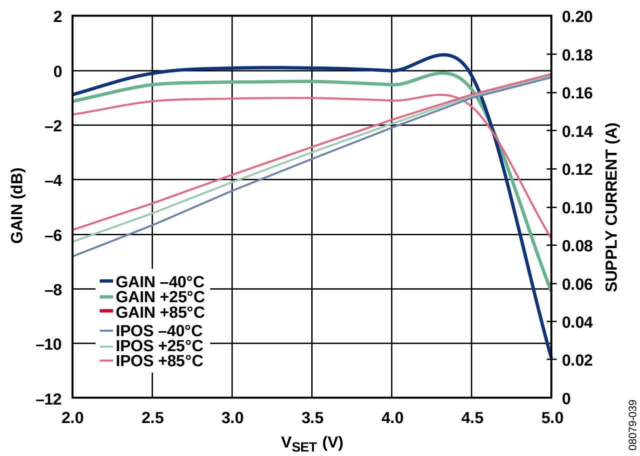

Figure 39. Power Conversion Gain and IPOS vs. V_{SET}

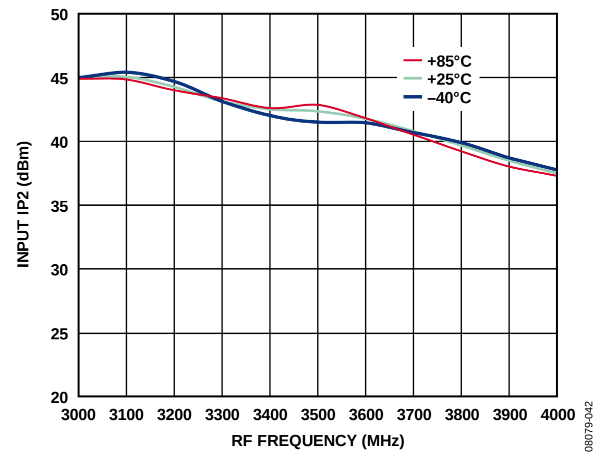

Figure 42. Input IP2 vs. RF Frequency

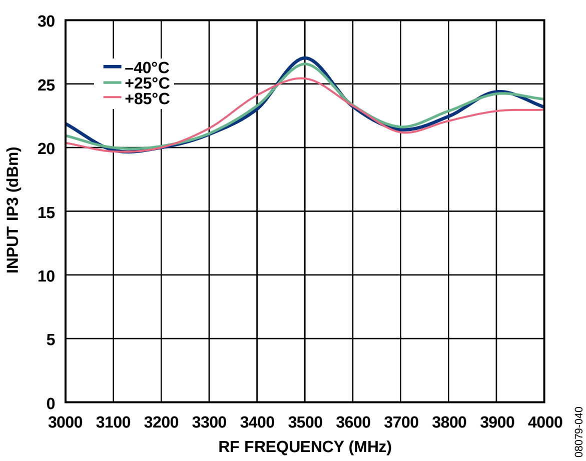

Figure 40. Input IP3 vs. RF Frequency

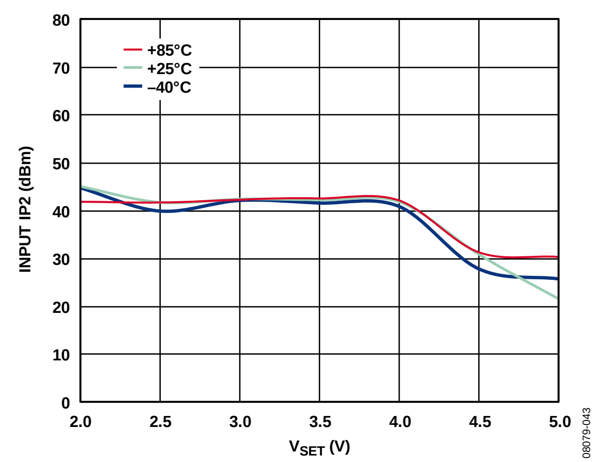

Figure 43. Input IP2 vs. V_{SET}

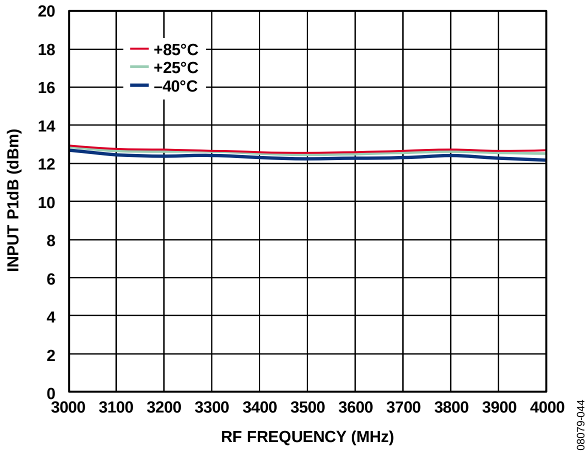

Figure 44. Input P1dB vs. RF Frequency

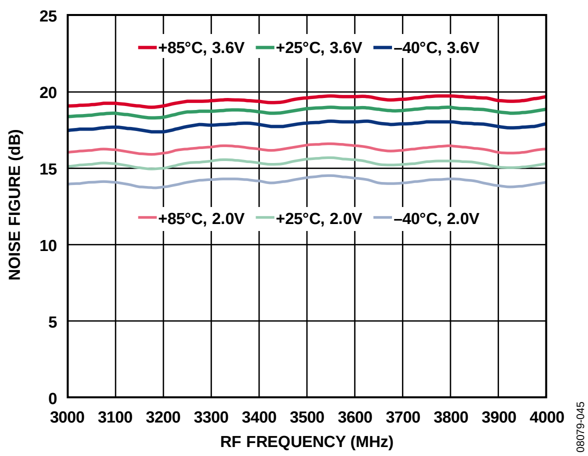

Figure 45. Noise Figure vs. RF Frequency

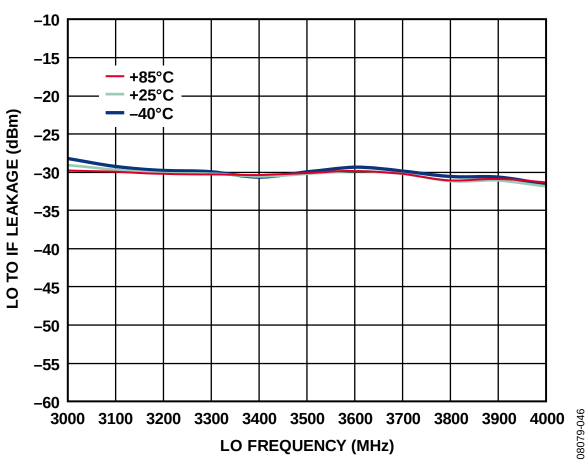

Figure 46. LO to IF Leakage vs. LO Frequency

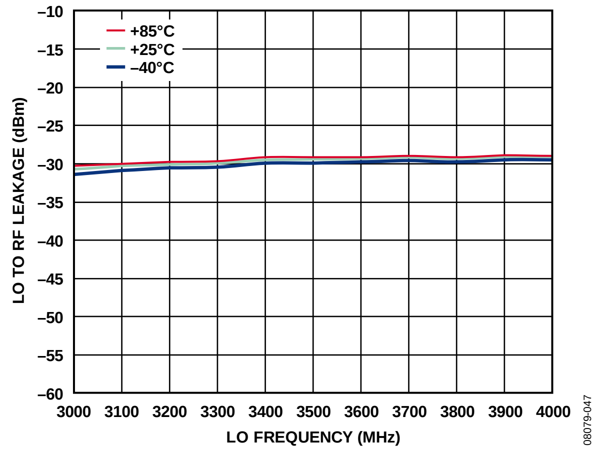

Figure 47. LO to RF Leakage vs. LO Frequency

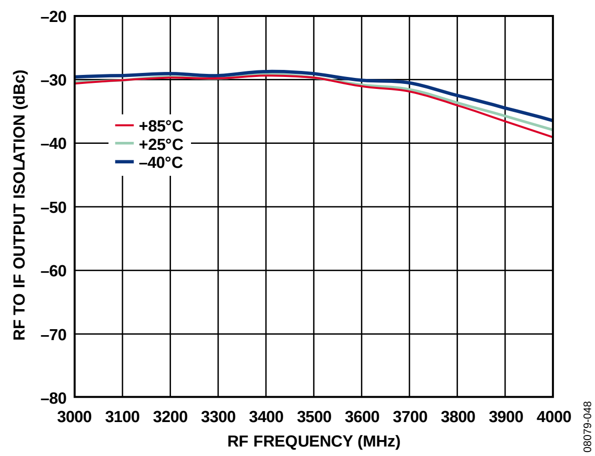

Figure 48. RF to IF Output Isolation vs. RF Frequency

DOWNCONVERTER MODE WITH A JOHANSON 5.7 GHZ INPUT BALUN

V_S = 5 V, T_A = 25°C, VSET = 3.6 V, IF = 153 MHz, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (5400BL14B050, TC4-1W+) is included in the gain measurement.

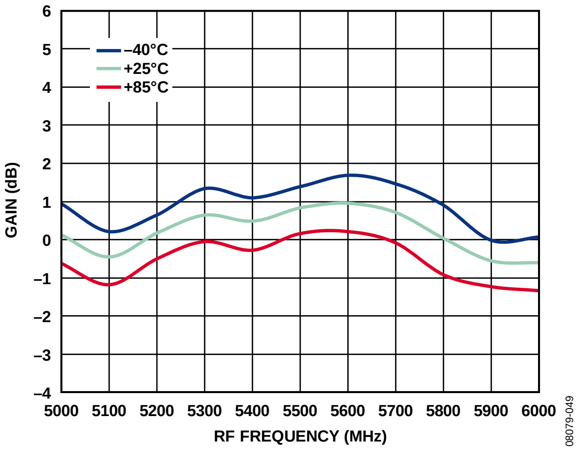

Figure 49. Power Conversion Gain vs. RF Frequency

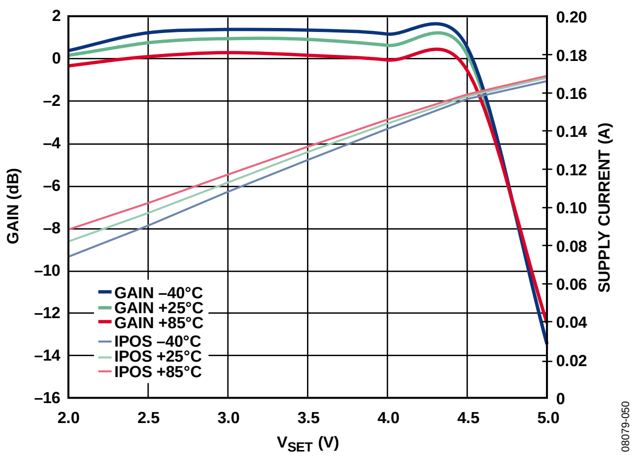

Figure 50. Power Conversion Gain and IPOS vs V_{SET}

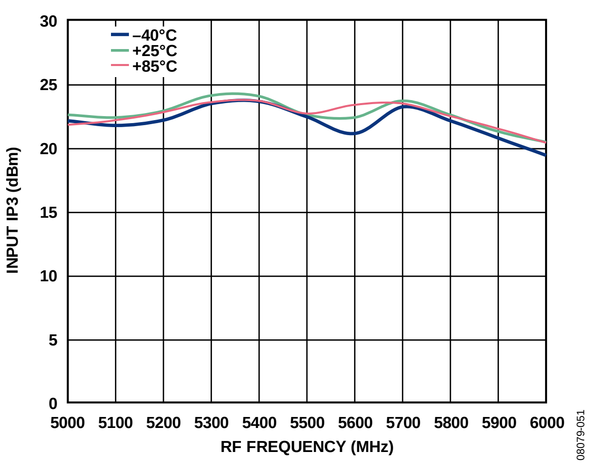

Figure 51. Input IP3 vs. RF Frequency

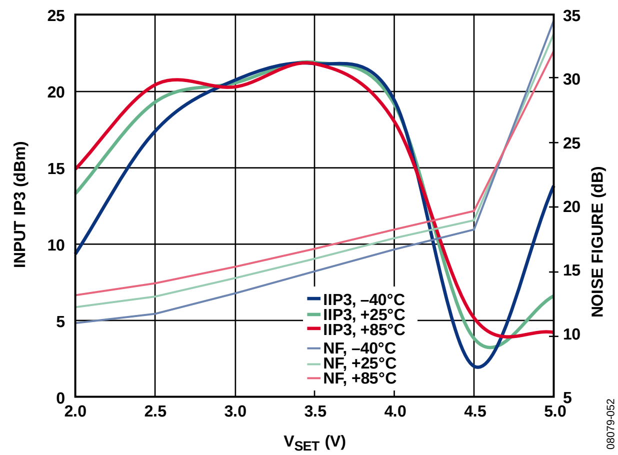

Figure 52. Input IP3 and Noise Figure vs. V_{SET}

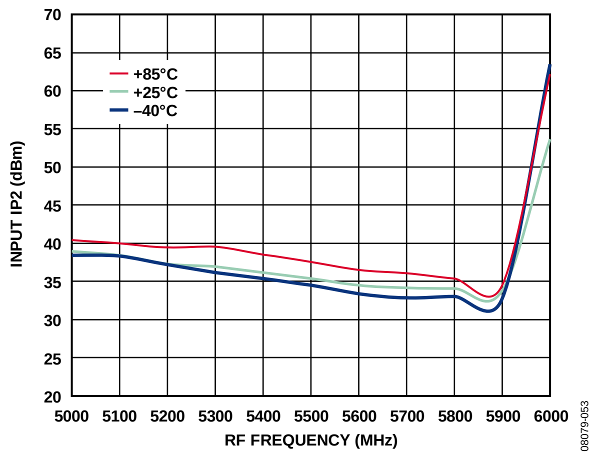

Figure 53. Input IP2 vs. RF Frequency

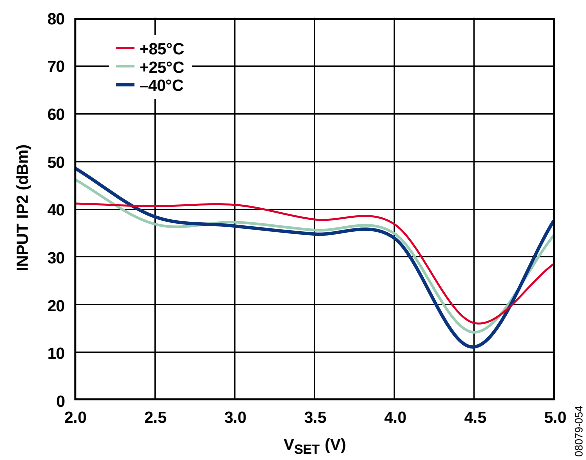

Figure 54.Input IP2 vs. V_{SET}

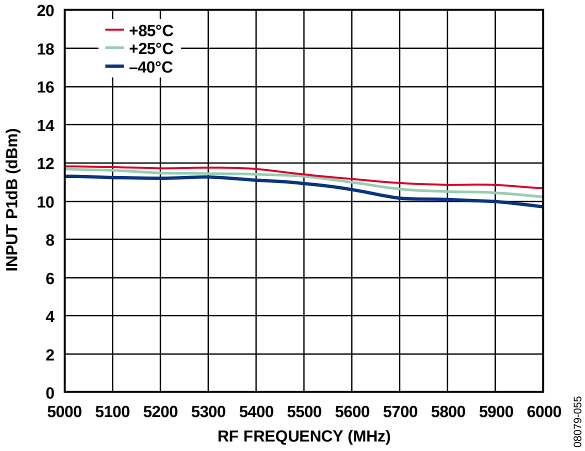

Figure 55. Input P1dB vs. RF Frequency

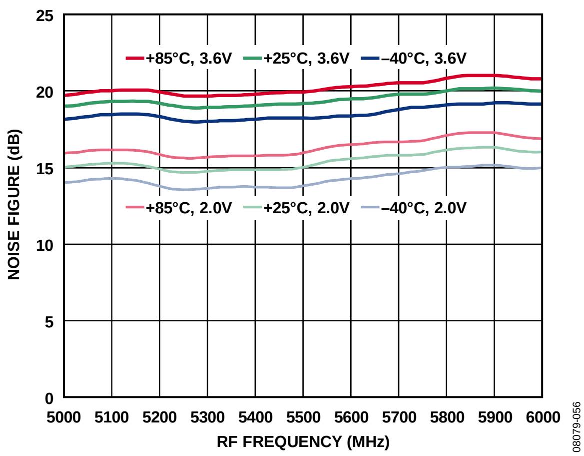

Figure 56. Noise Figure vs. RF Frequency, V_{SET} = 3.6 V

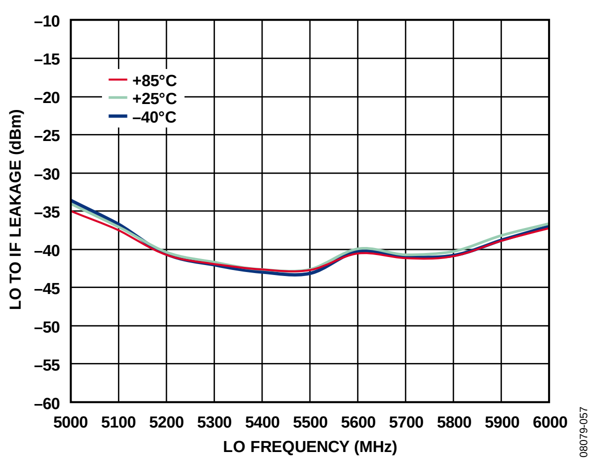

Figure 57. LO to IF Leakage vs. LO Frequency

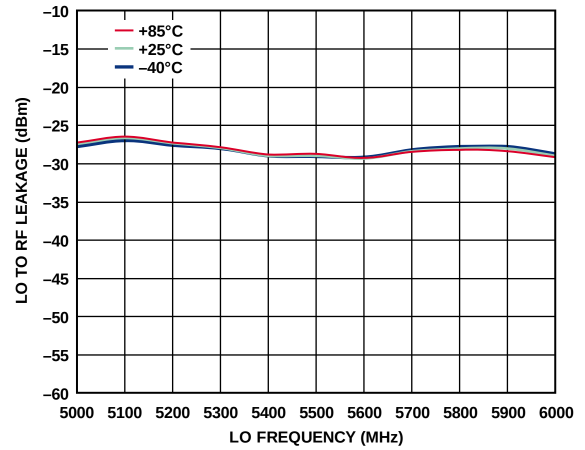

Figure 58. LO to RF Leakage vs. LO Frequency

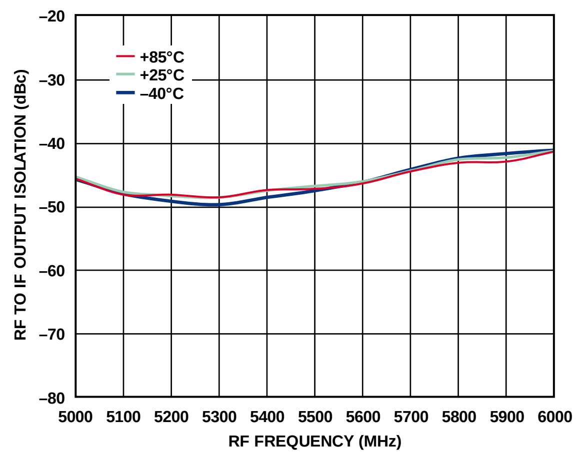

Figure 59. RF to IF Output Isolation vs. RF Frequency

UPCONVERTER MODE WITH A 900 MHZ OUTPUT MATCH

V_S = 5 V, T_A = 25°C, VSET = 3.6 V, RF = 153 MHz, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-14) is included in the gain measurement.

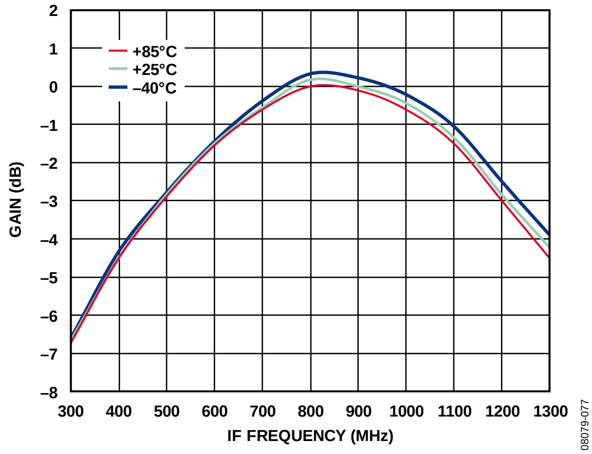

Figure 60. Power Conversion Gain vs. IF Frequency

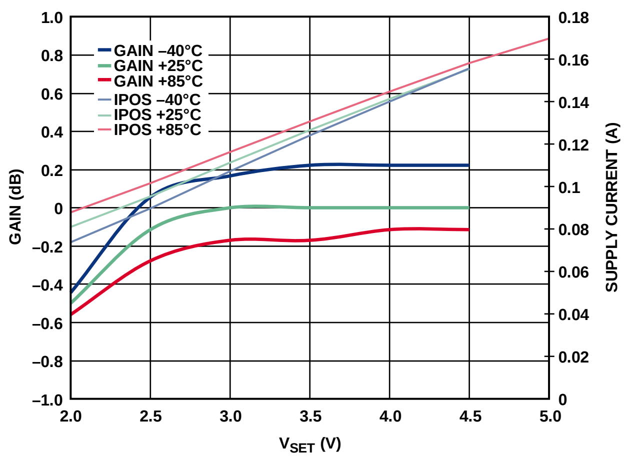

Figure 61. Power Conversion Gain and IPOS vs. V_{SET}

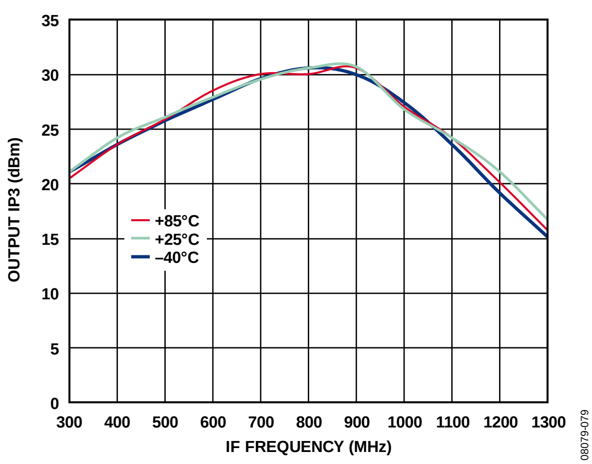

Figure 62. Output IP3 vs. IF Frequency

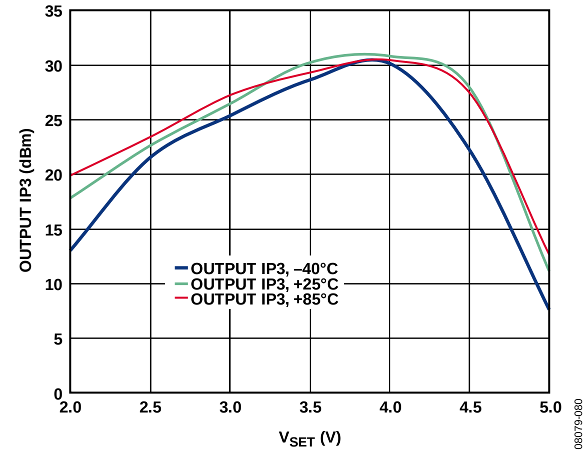

Figure 63. Output IP3 vs. V_{SET}

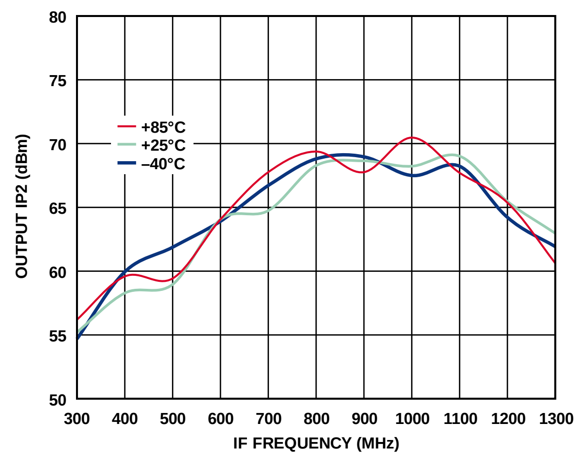

Figure 64. Output IP2 vs. IF Frequency

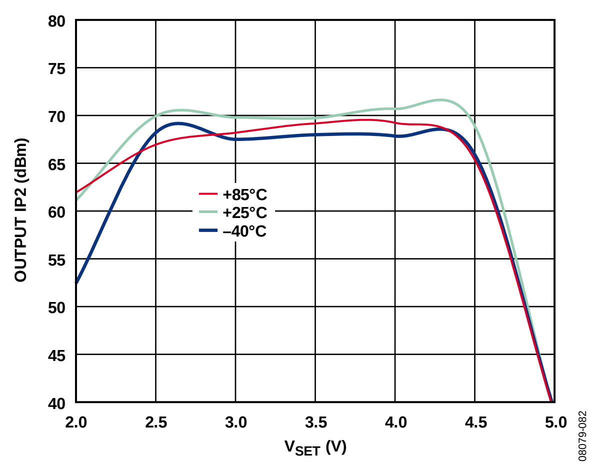

Figure 65. Output IP2 vs. V_{SET}

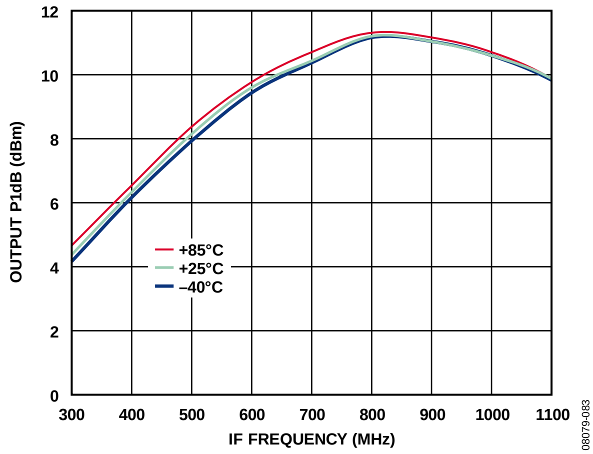

Figure 66. Output P1dB vs. IF Frequency

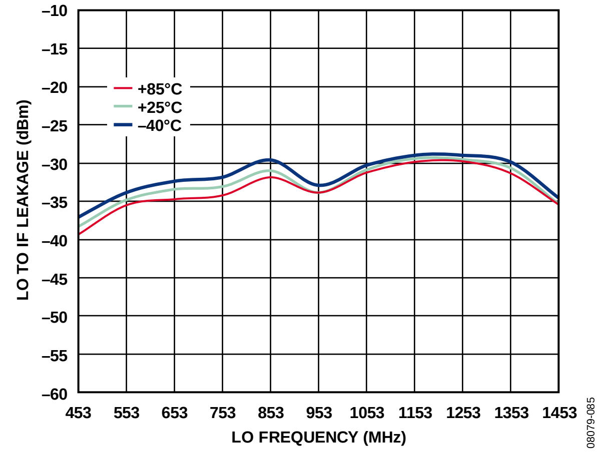

Figure 68. LO to IF Leakage vs. LO Frequency

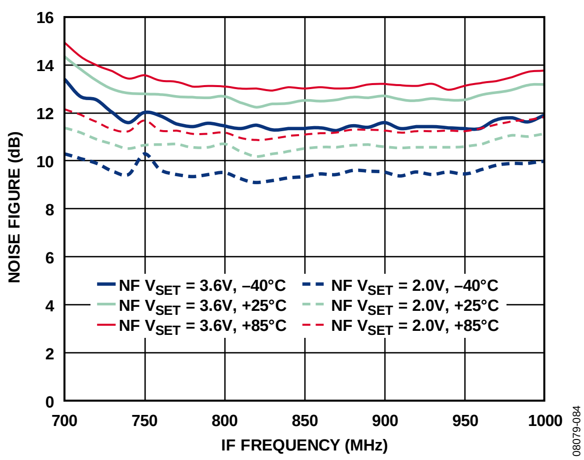

Figure 67. Noise Figure vs. IF Frequency, F_{LO} = 650 MHz

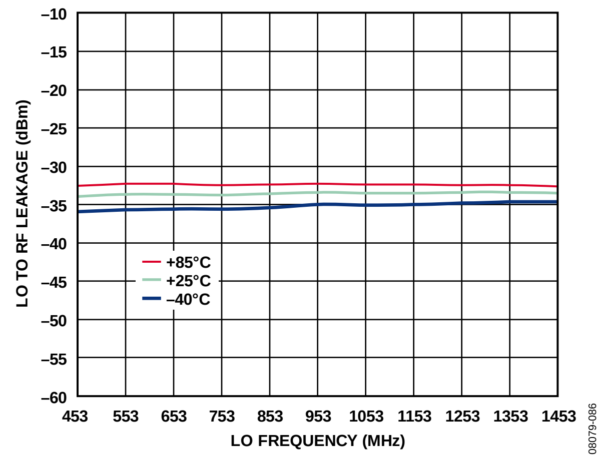

Figure 69. LO to RF Leakage vs. LO Frequency

UPCONVERTER MODE WITH A 2.1 GHZ OUTPUT MATCH

V_S = 5 V, T_A = 25°C, VSET = 4 V, RF = 170 MHz, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, 1850BL15B200) is included in the gain measurement.

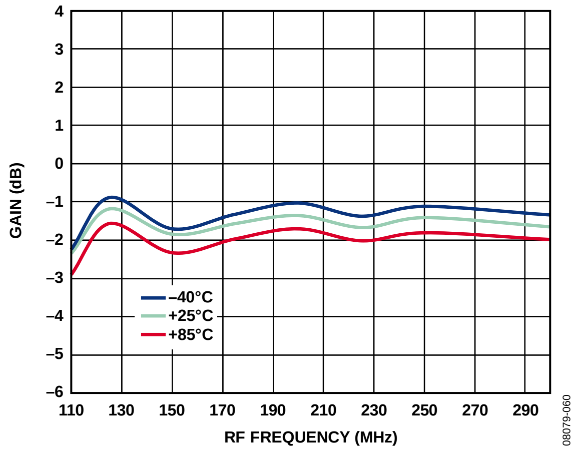

Figure 70. Power Conversion Gain vs. RF Frequency

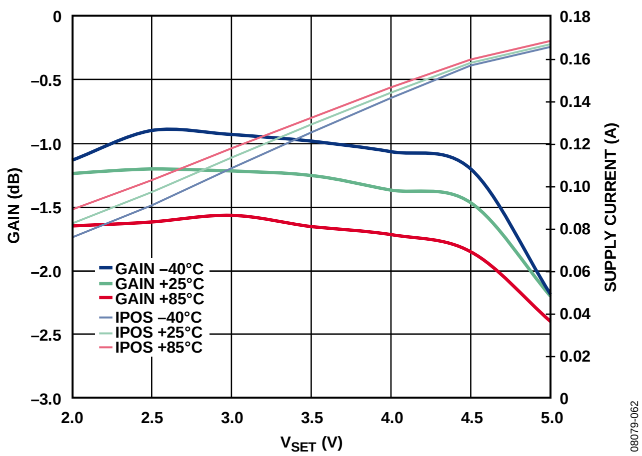

Figure 71. Power Conversion Gain and IPOS vs. V_{SET}

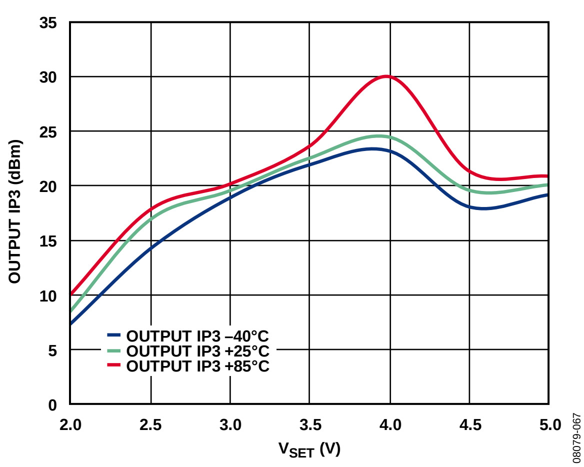

Figure 72. Output IP3 vs. V_{SET}

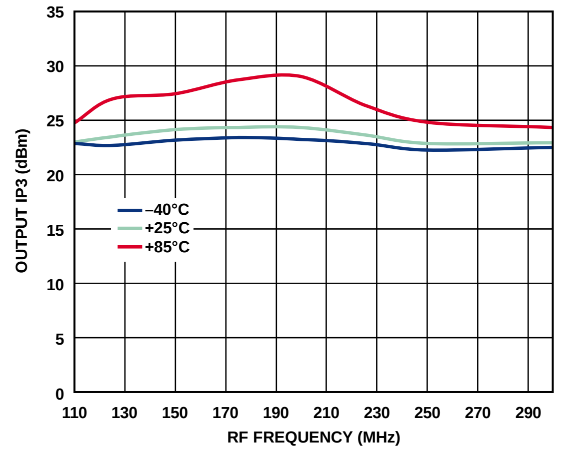

Figure 73. Output IP3 vs. RF Frequency

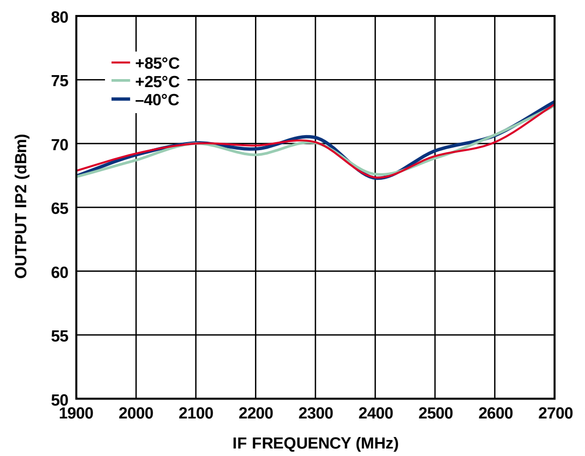

Figure 74. Output IP2 vs. IF Frequency

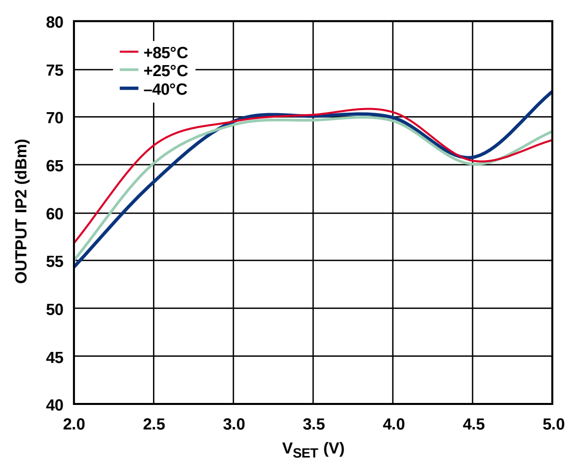

Figure 75. Output IP2 vs. V_{SET}

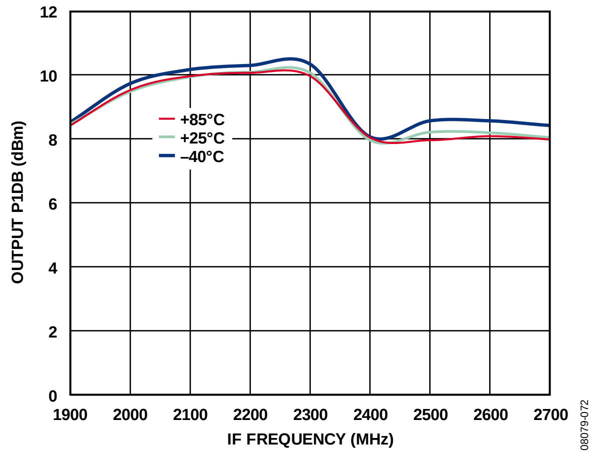

Figure 76. Output P1dB vs. IF Frequency

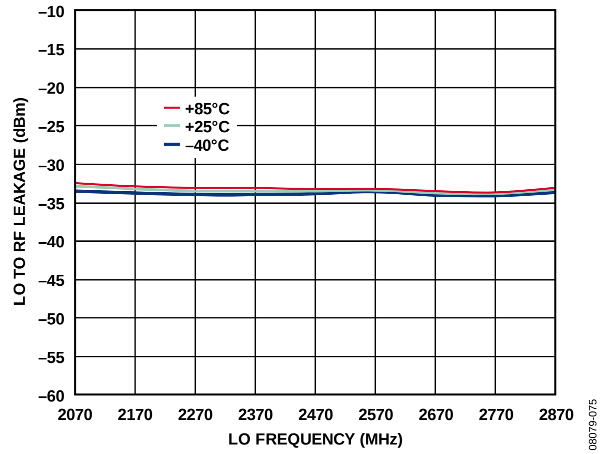

Figure 79. LO to RF Leakage vs. LO Frequency

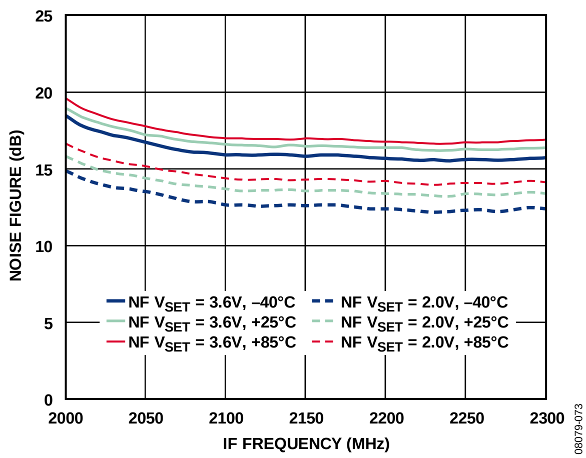

Figure 77. Noise Figure vs. IF Frequency, F_{LO} = 1950 MHz

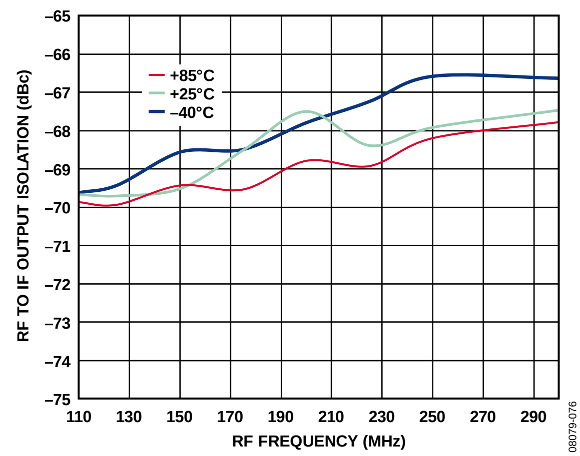

Figure 80. RF to IF Output Isolation vs. RF Frequency

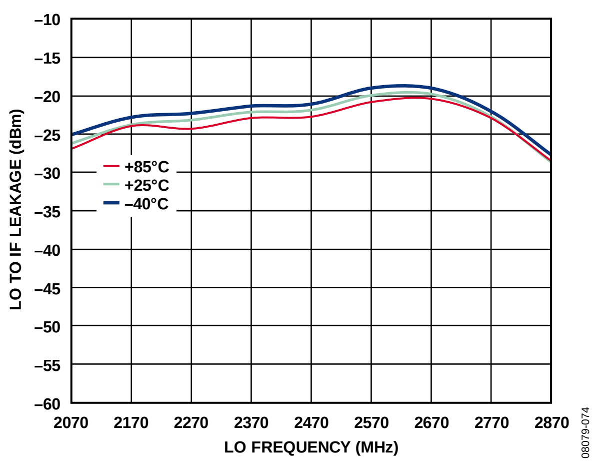

Figure 78. LO to IF Leakage vs. LO Frequency

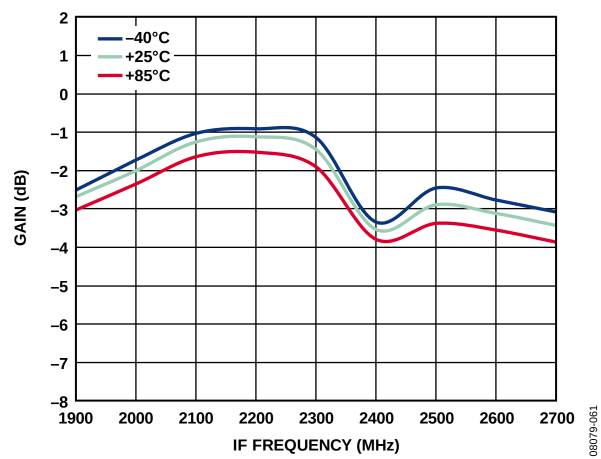

Figure 81. Power Conversion Gain vs. IF Frequency

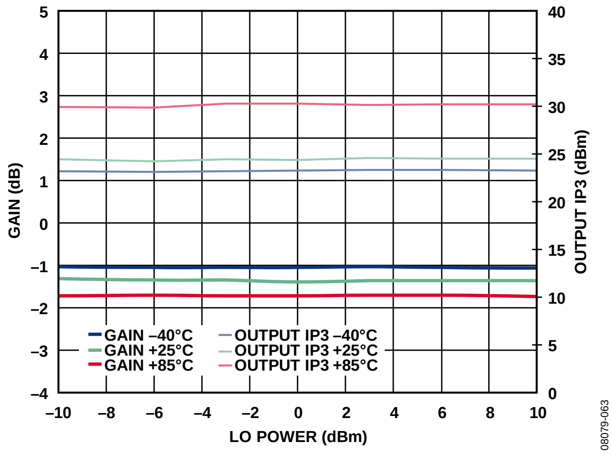

Figure 82. Power Conversion Gain and Output IP3 vs. LO Power

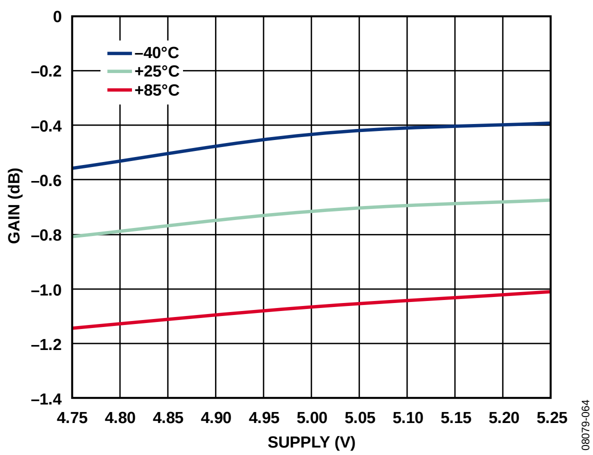

Figure 83. Power Conversion Gain vs. Supply

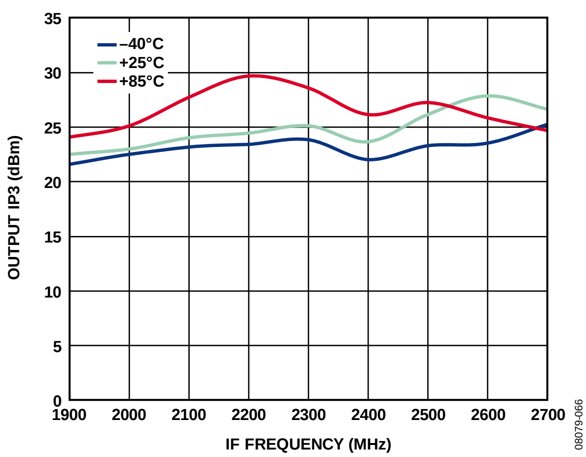

Figure 84. Output IP3 vs. IF Frequency

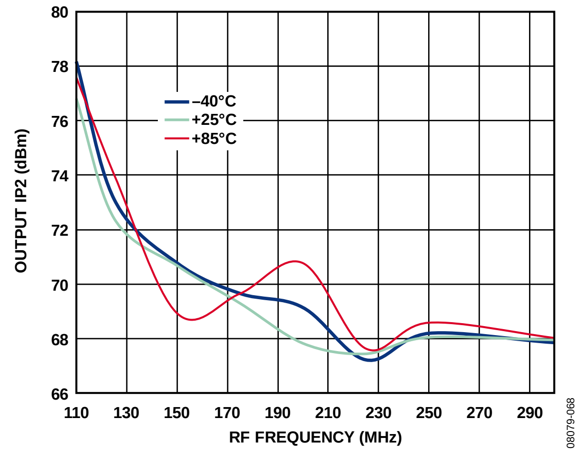

Figure 85. Output IP2 vs. RF Frequency

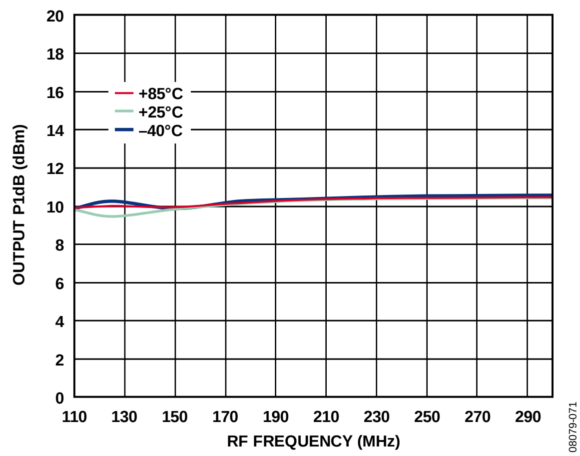

Figure 86. Output P1dB vs. RF Frequency

SPUR PERFORMANCE

All spur tables are (N × f_{RF}) − (M × f_{LO}) and were measured using the standard evaluation board (see the Evaluation Board section). Mixer spurious products are measured in decibels relative to the carrier (dBc) from the IF output power level. Data was measured for frequencies less than 6 GHz only. The typical noise floor of the measurement system is −100 dBm.

900 MHz Downconvert Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 900 MHz, f_{LO} = 703 MHz, Z_0 = 50 Ω.

		M														
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
	0		−33.1	−23.3	−45.8	−23.6	−45.9	−30.7	−55.4	−41.5						
	1	−48.8	0.0	−51.5	−19.0	−65.1	−29.6	−78.0	−50.3	−74.4	−57.7					
	2	−35.9	−74.9	−67.5	−66.1	−73.5	−80.5	−65.0	−89.8	−71.3	−88.5	−86.8	−98.8			
	3	−68.8	−64.8	−94.3	−65.9	−86.3	−70.2	−76.3	−70.6	−74.5	−81.4	≤−100	−99.6	≤−100		
	4	−47.5	−80.7	−78.0	−78.4	−95.1	−73.5	−89.4	−87.3	≤−100	−92.7	−99.5	−99.4	≤−100	≤−100	
	5	−95.6	−74.7	−89.8	−70.7	−84.8	−90.7	−86.7	−86.4	−83.1	−73.7	−78.7	−80.7	−91.1	≤−100	≤−100
	6	−85.7	−96.4	−83.1	−98.5	−83.3	−96.7	≤−100	−89.4	−99.6	−96.1	−96.1	−95.4	−95.5	≤−100	≤−100
N	**7**		≤−100	≤−100	−95.9	≤−100	−97.2	−83.1	−84.1	≤−100	≤−100	−99.7	−87.9	−88.8	−85.7	≤−100
	8			≤−100	≤−100	−99.0	−99.8	−86.0	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100
	9				≤−100	≤−100	≤−100	−90.9	−88.4	−83.5	−87.6	≤−100	≤−100	≤−100	≤−100	≤−100
	10						≤−100	≤−100	≤−100	−97.9	−95.5	−99.0	≤−100	≤−100	≤−100	≤−100
	11							≤−100	≤−100	−92.6	−87.4	−88.2	−92.3	−99.3	≤−100	≤−100
	12								≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100
	13										≤−100	≤−100	−95.1	−96.5	−90.4	≤−100
	14											≤−100	≤−100	≤−100	≤−100	≤−100
	15												≤−100	≤−100	≤−100	≤−100

1900 MHz Downconvert Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 1900 MHz, f_{LO} = 1703 MHz, Z_0 = 50 Ω.

		M														
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
	0		−31.4	−17.1	−51.4											
	1	−40.4	0.0	−53.6	−38.5	−71.0										
	2	−38.4	−66.0	−52.9	−68.1	−64.2	−86.8									
	3	≤−100	−66.2	−73.2	−72.6	−79.9	−65.2	−92.8								
	4		≤−100	−89.4	−86.4	−94.6	−87.4	−81.5	≤−100							
	5				−83.7	−66.2	−79.3	−89.0	−75.2	≤−100	≤−100					
	6					≤−100	−86.4	≤−100	−99.0	−87.7	≤−100	≤−100				
N	7						≤−100	−92.4	−92.7	≤−100	−98.4	≤−100	≤−100			
	8							≤−100	≤−100	−97.5	≤−100	−95.4	≤−100	≤−100		
	9								≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	
	10									≤−100	−97.2	−95.6	≤−100	≤−100	≤−100	≤−100
	11										≤−100	≤−100	≤−100	≤−100	≤−100	≤−100
	12											≤−100	≤−100	≤−100	≤−100	≤−100
	13												≤−100	≤−100	≤−100	≤−100
	14														≤−100	≤−100
	15															≤−100

2600 MHz Downconvert Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 2600 MHz, f_{LO} = 2350 MHz, Z_0 = 50 Ω.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−31.5	−30.3													
	1	−40.3	0.0	−55.8	−33.8												
	2	−71.7	−73.6	−50.6	−70.4	−64.8											
	3		−83.9	−66.5	−59.8	−71.3	−84.7										
	4			−94.7	−77.6	−92.6	−83.8	−90.6									
	5				−91.4	−71.1	−89.7	−98.2	−96.3	<100							
	6						−83.1	−90.3	−92.9	−97.3	<100						
	7							<100	−91.4	<100	<100	<100					
	8								<100	−96.6	<100	−91.8	<100				
	9									<100	−97.9	<100	−98.5	<100			
	10										<100	−93.5	<100	−98.8	<100		
	11											<100	<100	<100	<100	<100	
	12												<100	<100	<100	<100	<100
	13													<100	<100	<100	<100
	14														<100	<100	<100
	15																<100

3800 MHz Downconvert Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 3800 MHz, f_{LO} = 3500 MHz, Z_0 = 50 Ω.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−27.3														
	1	−33.7	0.0	−54.9													
	2		−78.5	−47.1	−66.4												
	3			−63.6	−57.8	−81.4											
	4				−89.6	−77.2	−72.2	−99.2									
	5					<100	−88.0	−80.4	<100								
	6						<100	−90.0	−90.4	<100							
	7							<100	−79.1	<100	<100						
	8								<100	−85.2	<100	<100					
	9										<100	<100	<100				
	10											<100	−95.9	<100			
	11												<100	<100	<100		
	12													<100	<100	<100	
	13														<100	<100	<100
	14															<100	<100
	15																<100

5800 MHz Downconvert Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 5800 MHz, f_{LO} = 5600 MHz, Z_0 = 50 Ω.

		M															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
	0		−44.9														
	1	−43.9	0.0	−68.9													
	2			−44.0	−78.0												
	3				−47.0	−93.3											
	4					−60.6	−87.8										
	5						−62.7	−85.7									
	6							−70.2	−97.8								
N	**7**								−79.5	−85.3							
	8									−71.2	<100						
	9										<100	<100					
	10											<100	<100				
	11												<100	<100			
	12													<100	<100		
	13														−100.3	<100	
	14															−95.6	−96.0
	15																<100

806 MHz Upconvert Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 140 MHz, f_{LO} = 946 MHz, Z_0 = 50 Ω.

		M															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
	0		−35.2	−22.9	−42.8	−28.4	−59.1	−40.1									
	1	−66.0	0.0	−67.7	−14.0	−70.0	−37.1	−74.3									
	2	−67.8	−66.0	−62.9	−65.3	−61.1	−84.1	−81.2									
	3	−99.2	−66.2	−92.2	−69.2	−84.9	−84.3	<100									
	4	−77.1	−97.2	−85.1	−97.8	−82.0	<100	<100									
	5	−88.7	<100	−88.5	−92.9	−96.4	−93.6	<100	<100								
	6	−86.1	<100	−92.7	−95.8	−87.5	−99.5	<100	<100								
N	**7**	−90.2	<100	<100	−84.6	<100	−88.0	<100	<100								
	8	−73.8	<100	−94.8	−96.4	−93.4	−99.6	<100	<100								
	9	−91.1	−96.3	<100	−91.5	−100.3	−93.3	<100	<100								
	10	−66.2	<100	<100	<100	−88.3	−100.0	<100	<100								
	11	−87.7	−93.6	<100	−95.9	<100	<100	<100	<100								
	12	−69.5	−89.1	<100	<100	−93.8	<100	<100	<100	<100							
	13	−85.2	−95.7	<100	<100	−97.7	−90.5	−96.0	<100	<100							
	14	−65.2	−85.9	<100	−93.1	−94.5	<100	<100	<100	<100							
	15	−91.3	−93.5	<100	−96.6	v98.7	−93.5	−99.6	<100	<100							

2210 MHz Upconvert Performance

V_S = 5 V, VSET = 4.0 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 140 MHz, f_{LO} = 2350 MHz, Z_0 = 50 Ω.

		M															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
N	**0**		−21.0	−12.8													
	1	−81.3	0.0	−70.1													
	2	−66.0	−58.8	−51.5													
	3	<100	−56.7	−78.2													
	4	−74.4	−86.3	−76.5													
	5	<100	−75.3	−88.0													
	6	−90.9	−81.4	−91.5													
	7	−96.4	−71.2	−85.9													
	8	−75.8	−89.7	−86.3	<100												
	9	−92.9	−86.2	−92.2	<100												
	10	−66.5	<100	−97.5	<100												
	11	−83.7	−98.4	−97.9	<100												
	12	−64.8	<100	−93.1	<100												
	13	−81.2	<100	<100	<100												
	14	−64.5	<100	−91.0	<100												
	15	−85.3	<100	<100	−95.4												

CIRCUIT DESCRIPTION

The ADL5801 includes a double-balanced active mixer with a 50 Ω input impedance and 250 Ω output impedance. In addition, the ADL5801 integrates a local oscillator (LO) amplifier and an RF power detector that can be used to optimize the mixer dynamic range. The RF and LO are differential, providing maximum usable bandwidth at the input and output ports. The LO also operates with a 50 Ω input impedance and can, optionally, be operated differentially or single ended. The input, output, and LO ports can be operated over an exceptionally wide frequency range. The ADL5801 can be configured as a downconvert mixer or as an upconvert mixer.

The ADL5801 can be divided into the following sections: the LO amplifier and splitter, the RF voltage-to-current (V-to-I) converter, the mixer core, the output loads, the RF detector, and the bias circuit. A simplified block diagram of the device is shown in Figure 87. The LO block generates a pair of differential LO signals to drive two mixer cores. The RF input power is converted into RF currents by the V-to-I converter that then feed into the two-mixer core. The internal differential load of the mixer provides a wideband 250 Ω output impedance from the mixer. Reference currents to each section are generated by the bias circuit, which can be enabled or disabled using the ENBL pin. A detailed description of each section of the ADL5801 follows.

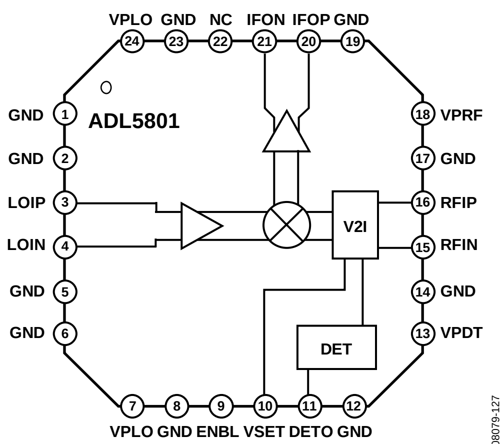

Figure 87. Block Diagram

LO AMPLIFIER AND SPLITTER

The LO input is conditioned by a series of amplifiers to provide a well controlled and limited LO swing to the mixer core, resulting in excellent input IP3. The LO input is amplified using a broadband low noise amplifier (LNA) and is then followed by LO limiting amplifiers. The LNA input impedance is nominally 50 Ω. The LO circuit exhibits low additive noise, resulting in an excellent mixer noise figure and output noise under RF blocking. For optimal performance, the LO inputs should be driven differentially but at lower frequencies; single-ended drive is acceptable.

RF VOLTAGE-TO-CURRENT (V-TO-I) CONVERTER

The differential RF input signal is applied to a V-to-I converter that converts the differential input voltage to output currents. The V-to-I converter provides a 50 Ω input impedance. The V-to-I section bias current can be adjusted up or down using the VSET pin. Adjusting the current up improves IP3 and P1dB input but degrades the SSB noise figure. Adjusting the current down improves the SSB noise figure but degrades IP3 and P1dB input. Conversion gain remains nearly constant over a wide range of VSET pin settings, allowing the part to be adjusted dynamically without affecting conversion gain.

Internally, the VSET pin features a series resistance and diode to ground; hence a simple voltage divider driving the pin is not sufficient. Current adjustment can be made by connecting a resistor from the VSET pin to the positive supply, however. Table 4 lists some typical values for this resistor and the resulting VSET value and supply current. Use Table 4 to select the appropriate value of R10 (see Figure 106) to achieve the desired mixer bias level. In this mode of operation, R7 and R9 should remain open.

Table 4. Suggested Values of R10 to Achieve the Desired Mixer Bias Level

R10 (Ω)	VSET (V)	I_{POS} (mA)[1]
226	4.5	160
562	4.01	146
568	4	145
659	3.9	142
665	3.89	142
694	3.85	142
760	3.8	139
768	3.79	139
1000	3.6	133
1100	3.53	131
1150	3.5	130
1200	3.47	129
1300	3.4	127
1400	3.35	126
1500	3.3	124
1600	3.26	122
1700	3.21	121
1800	3.17	120
1900	3.14	119
2000	3.1	118
2300	3	114
5900	2.5	98
Open	2.03	82

[1] I_{POS} is the mixer supply current.

Optionally, the VSET pin can be connected to the DETO pin to provide automatic setting of the mixer core current.

MIXER CORE

The ADL5801 has a double-balanced mixer that uses high performance SiGe NPN transistors. This mixer is based on the Gilbert cell design of four cross-connected transistors.

MIXER OUTPUT LOAD

The mixer load uses a pair of 125 Ω resistors connected to the positive supply. This provides a 250 Ω differential output resistance. The mixer output should be pulled to the positive supply externally using a pair of RF chokes or using an output transformer with the center tap connected to the positive supply. It is possible to exclude these components when the mixer core current is low, but both P1dB input and IP3 input are then reduced.

The mixer load output can operate from direct current (dc) up to approximately 600 MHz into a 200 Ω load. For upconversion applications, the mixer load can be matched using off-chip matching components. Transmit operation up to 3 GHz is possible. See the Applications Information section for matching circuit details.

RF DETECTOR

An RF power detector is buffered from the V-to-I converter section. This detector has a power response range from approximately −25 dBm up to 0 dBm and provides a current output. The output current is designed to be connected to the VSET pin to boost the mixer core current when large RF signals are present at the mixer input. An external capacitor can be used to adjust the response time of this function. If not used, the DETO pin can be left open or connected to ground.

The detector was characterized under the conditions specified in the Downcoverter Mode with a Broadband Balun section. Pin 11 (DETO) was connected to Pin 10 (VSET), and the voltage on these pins was plotted vs. the RF input power level over temperature and a number of devices.

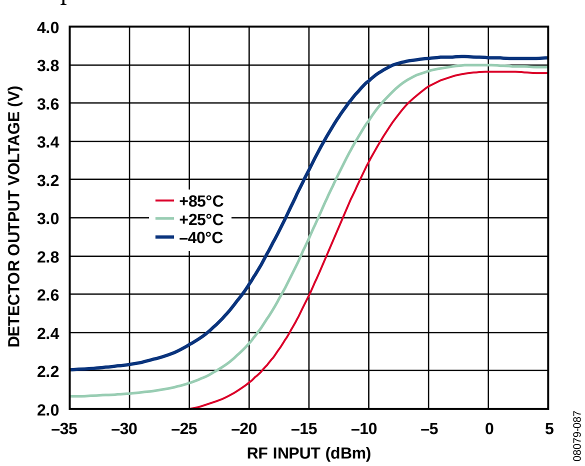

Figure 88. Detector Output Voltage vs. RF Input

The input IP3, gain and supply current were also recorded under these conditions. The result can be seen in Figure 89 through Figure 91.

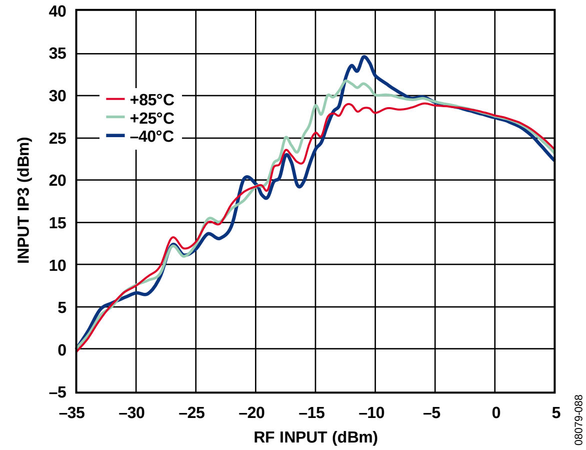

Figure 89. Input IP3 vs. RF Input

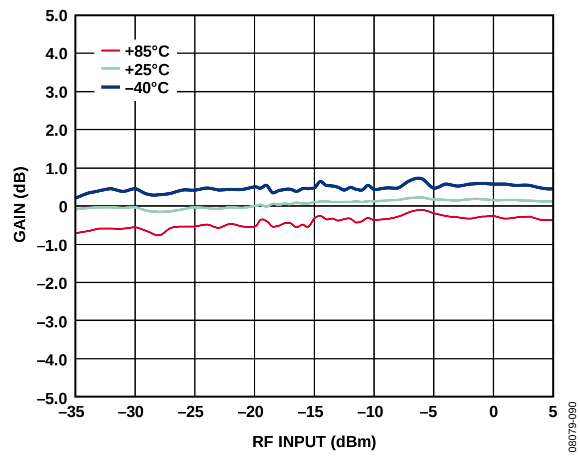

Figure 90.Power Conversion Gain vs. RF Input

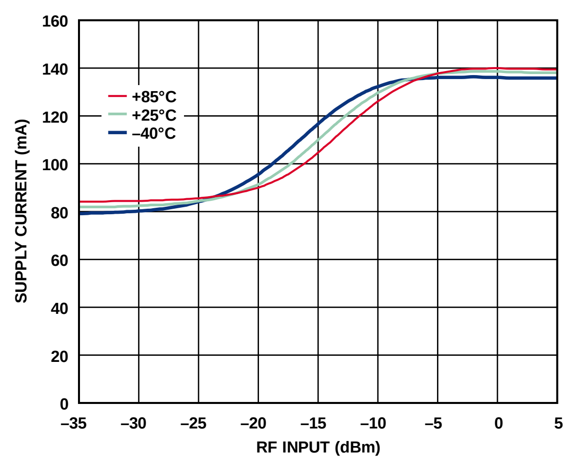

Figure 91. Supply Current vs. RF Input

BIAS CIRCUIT

A band gap reference circuit generates the reference currents used by mixers. The bias circuit can be enabled and disabled using the ENBL pin. If the ENBL pin is grounded or left open, the part is enabled. Pulling the ENBL pin high shuts off the bias circuit and disables the part. However, the ENBL pin does not alter the current in the LO section and, therefore, does not provide a true power-down feature. In addition, if the VSET pin is connected to the positive supply through a resistor to increase the mixer core current, this continues to provide bias current to the mixer core unless the resistor supply is also removed.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5801 is designed to translate between radio frequencies (RF) and intermediate frequencies (IF). For both upconversion and downconversion applications, RFIP (Pin 16) and RFIN (Pin 15) must be configured as the input interfaces. IFOP (Pin 20) and IFON (Pin 21) must be configured as the output interfaces. Individual bypass capacitors are needed in close proximity to each supply pin (Pin 7, Pin 13, Pin 18, and Pin 24), the VSET control pin (Pin 10), and the DETO detector output pin (Pin 11). When the on-chip detector is chosen to form a closed loop, automatically controlling the VSET pin, R7 can be populated with a 0 Ω resistor. Alternatively, simply use a jumper between the VSET and DETO test points for evaluation. Figure 92 illustrates the basic connections for ADL5801 operation.

RF AND LO PORTS

The RF and LO input ports are designed for a differential input impedance of approximately 50 Ω. Figure 93 and Figure 94 illustrate the RF and LO interfaces, respectively. It is recommended that each of the RF and LO differential ports be driven through a balun for optimum performance. It is also necessary to ac couple both RF and LO ports. Using proper value capacitors may help improve the input return loss over desired frequencies. Table 5 and Table 8 list the recommended components for various RF and LO frequency bands in upconvert and downconvert modes. The characterization data is available in the Typical Performance Characteristics section.

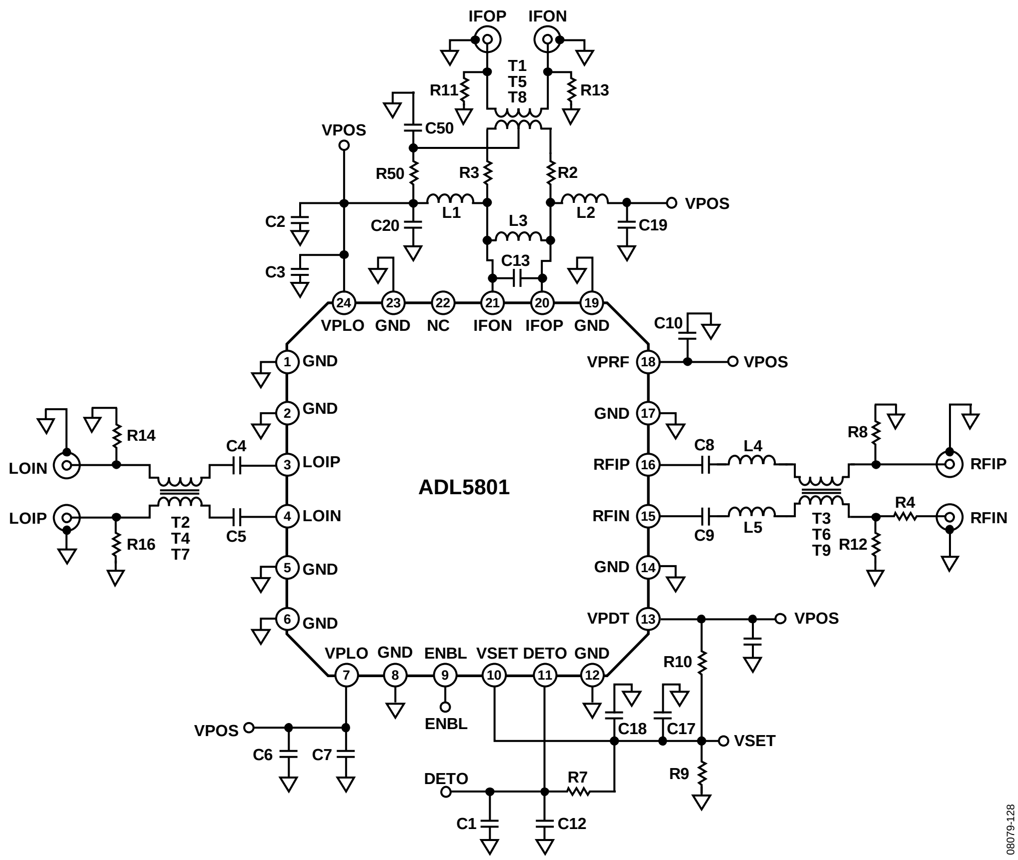

Figure 92. Basic Connections Schematic

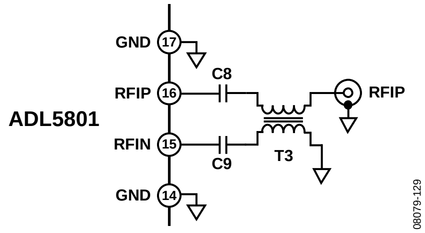

Figure 93. RF Interface

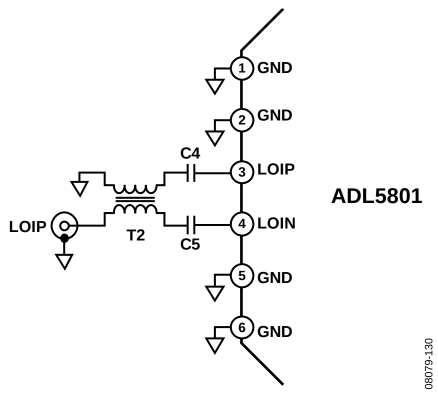

Figure 94. LO Interface

Table 5. Suggested Components for the RF and LO Interfaces in Downconvert Mode

RF and LO Frequency	T2, T3	C8, C9	C4, C5
10 MHz	Mini-Circuits TC1-1-13M+	1 nF	1 nF
900 MHz	Mini-Circuits TC1-1-13M+	5.6 pF	100 pF
1900 MHz	Mini-Circuits TC1-1-13M+	5.6 pF	100 pF
2500 MHz	Mini-Circuits TC1-1-43M+	2 pF	8 pF
3500 MHz	3600BL14M050	1.5 pF	1.5 pF
5500 MHz	5400BL14B050	3 pF	3 pF
10 MHz to 6000 MHz	Mini-Circuits TCM1-63AX+	1 nF	1 nF

Table 6. Suggested Components for the RF Interface in Upconvert Mode

RF Frequency	T3	C8, C9
153 MHz	TC1-1-13M+	470 pF

IF PORT

The IF port features an open-collector, differential output interface. It is necessary to bias the open collector outputs using one of the schemes presented in Figure 95 and Figure 96.

Figure 95 shows the use of center-tapped impedance transformers. The turns ratio of the transformer should be selected to provide the desired impedance transformation. In the case of a 50 Ω load impedance, a 4:1 impedance ratio transformer should be used to transform the 50 Ω load into a 200 Ω differential load at the IF output pins.

Figure 96 shows a differential IF interface where pull-up choke inductors are used to bias the open-collector outputs. The shunting impedance of the choke inductors used to couple dc current into the mixer core should be large enough at the IF frequency of operation not to load down the output current before it reaches the intended load. Additionally, the dc current handling capability of the selected choke inductors must be at least 45 mA.

The self-resonant frequency of the selected choke inductors must be higher than the intended IF frequency. A variety of suitable choke inductors is commercially available from manufacturers such as Coilcraft® and Murata. An impedance transforming network may be required to transform the final load impedance to 200 Ω at the IF outputs.

Table 7 lists suggested components for the IF port in the upconvert and downconvert modes.

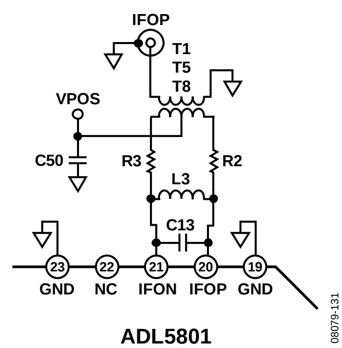

Figure 95. Biasing the IF Port Open-Collector Outputs Using a Center-Tapped Impedance Transformer

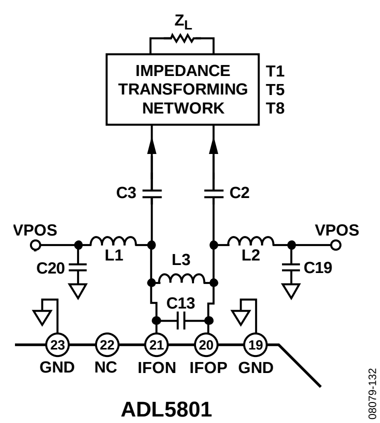

Figure 96. Biasing the IF Port Open-Collector Outputs Using Pull-Up Choke Inductors

Table 7. Suggested Components for the IF Port in Upconvert and Downconvert Modes

IF Frequency	Mode of Operation	T1	L3
0 MHz to 500 MHz	Downconvert	TC4-1W+	Open
900 MHz	Upconvert	TC4-14+	27 nH
2140 MHz	Upconvert	1850BL15B200	3.3 nH

DOWNCONVERTING TO LOW FREQUENCIES

For downconversion to lower frequencies, the device should be biased at the output with a resistor. The common-mode voltage at the IF output of the device should be 3.75 V to ensure optimal performance. Figure 97 provides a sample setup to downconvert a 900 MHz input signal down to 100 kHz. In the setup depicted in Figure 97, the output of the device is biased with 50 Ω resistors. In this mode of operation, the device exhibits 2.0 dB of conversion gain when a signal at 500 MHz was downcoverted to a 100 kHz, 10 kHz or 1 kHz.

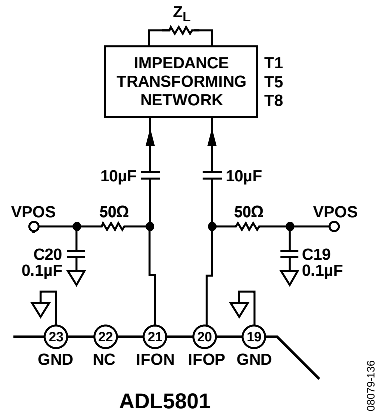

Figure 97. Resistive Bias Network to Downconvert Signals to Low Frequencies

BROADBAND OPERATION

The ADL5801 can support input frequencies from 10 MHz to 6 GHz. The device can be operated with a broadband balun such as the MiniCircuits TCM1-63AX+ for applications that need wideband frequency coverage. Figure 98 illustrates a sample setup configuration with the MiniCircuits TCM1-63AX+ balun populated on the RF and LO ports. This single setup solution provides the option to utilize the complete input frequency range of the device.

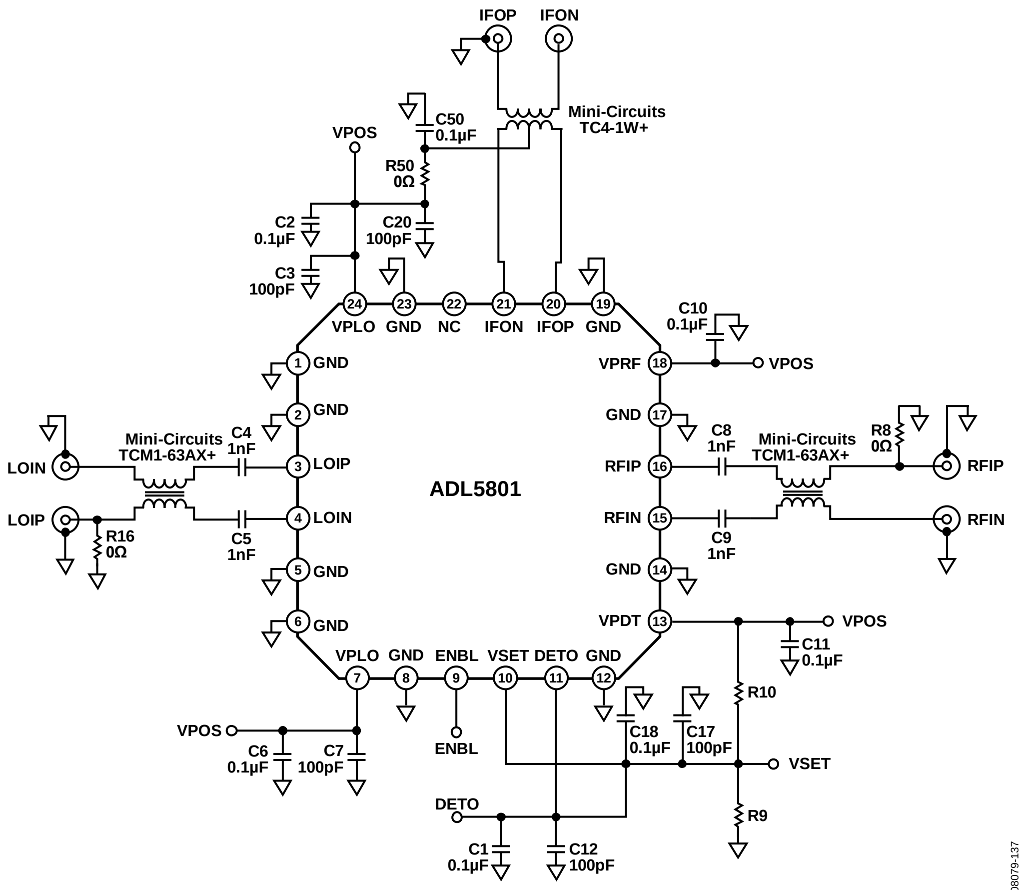

Figure 98. Sample Setup Configuration with the MiniCircuits TCM1-63AX+ Broadband Balun

Figure 99 to Figure 101 demonstrate the performance of the mixer with the MiniCircuits TCM1-63AX+ populated on the RF and LO ports.

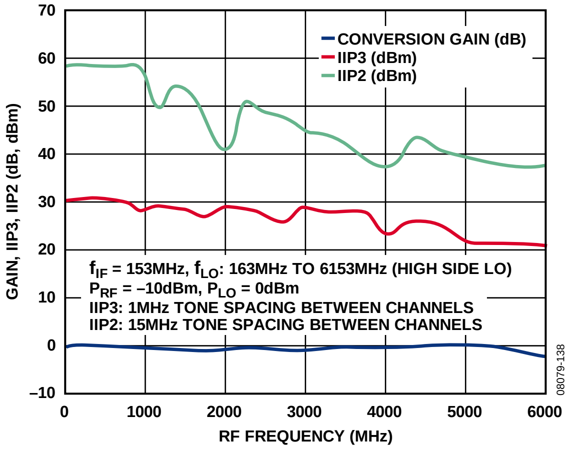

Figure 99. Gain, IIP3, IIP2 vs. RF Frequency

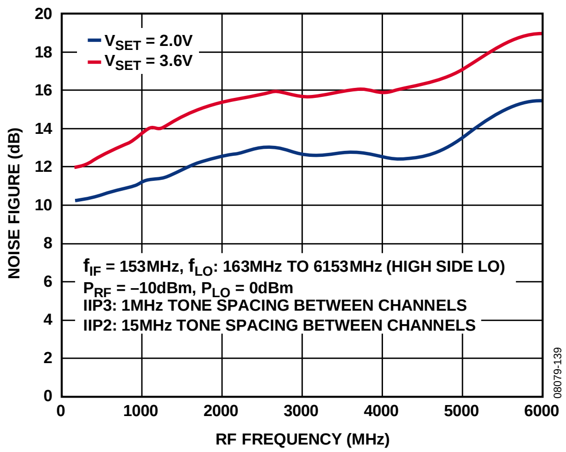

Figure 100. Noise Figure vs. RF Frequency

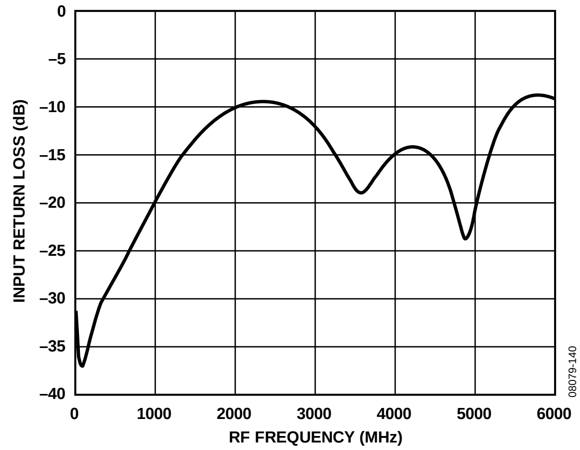

Figure 101. Input Return Loss vs. RF Frequency

The device maintains an Input IP3 of 20 dBm or better and conversion gain of −2 dB or better across the 10 MHz to 6 GHz frequency band.

SINGLE-ENDED DRIVE OF RF AND LO INPUTS

The RF and LO ports of the active mixer can be driven single-ended without baluns for single-ended operation. In this configuration, the unused RF and LO ports should be ac grounded using a 1 nF capacitor. Figure 102 depicts setup configuration suggested to operate the device in the single-ended mode.

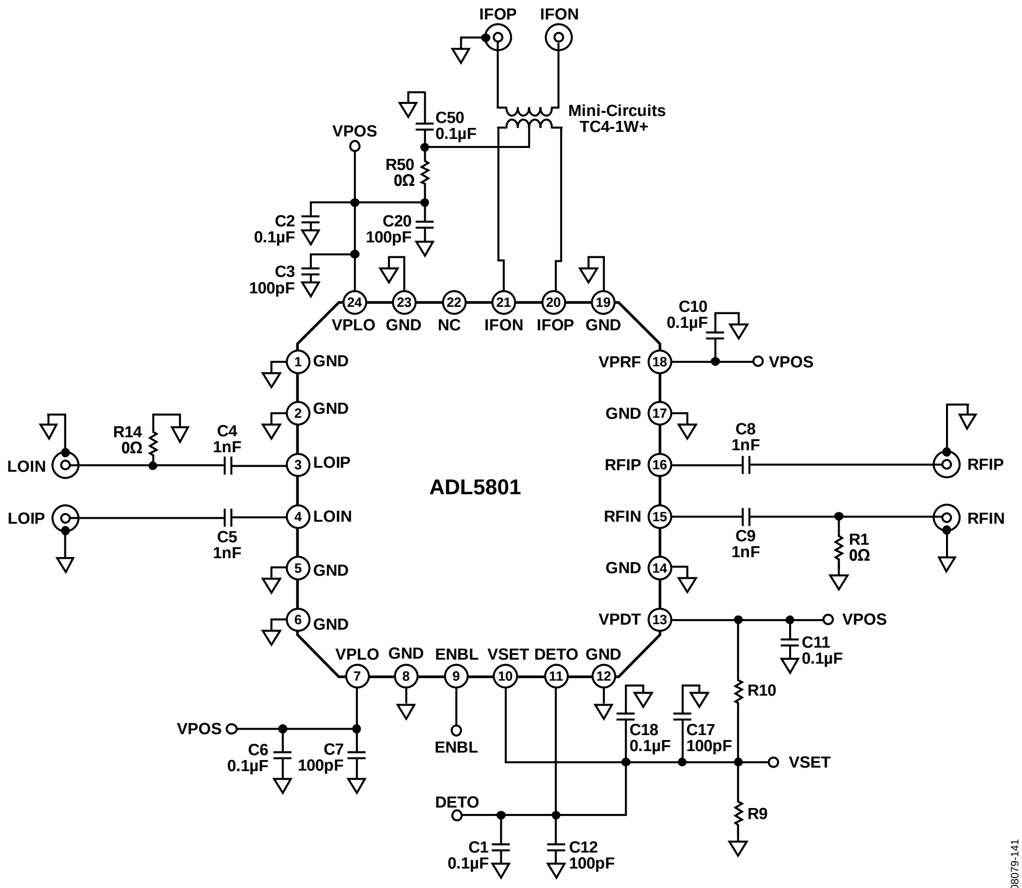

Figure 102. Single-Ended Configuration to Operate the ADL5801

Figure 103 to Figure 105 demonstrate the performance of the mixer in the single ended mode.

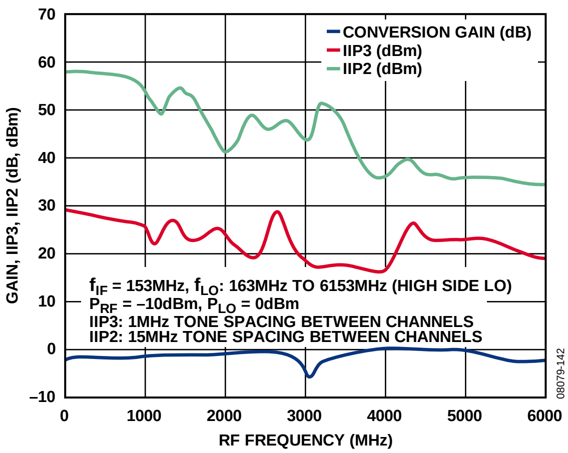

Figure 103. Gain, IIP3, IIP2 vs. RF Frequency

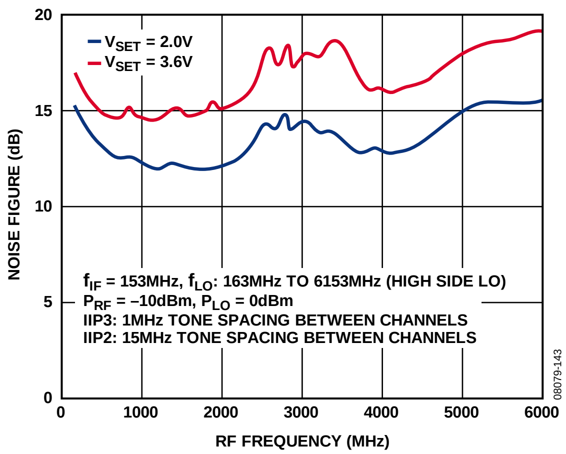

Figure 104. Noise Figure vs. RF Frequency

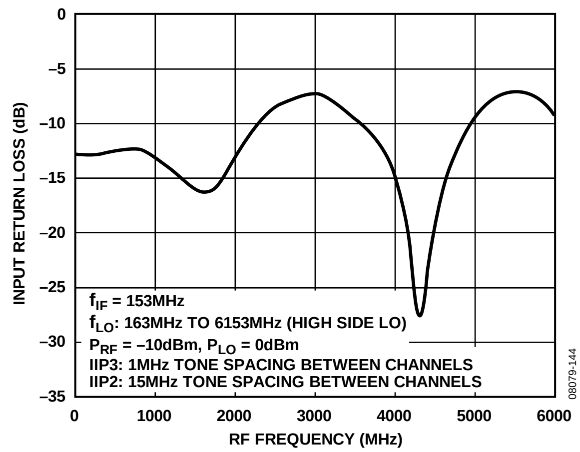

Figure 105. Input Return Loss vs. RF Frequency

EVALUATION BOARD

An evaluation board is available for the ADL5801. The standard evaluation board is fabricated using Rogers® RO3003 material. Each RF, LO, and IF port is configured for single-ended signaling via a balun transformer. The schematic for the evaluation board is shown in Figure 106. Table 8 describes the various configuration options for the evaluation board. Layout for the board is shown in Figure 107 and Figure 108.

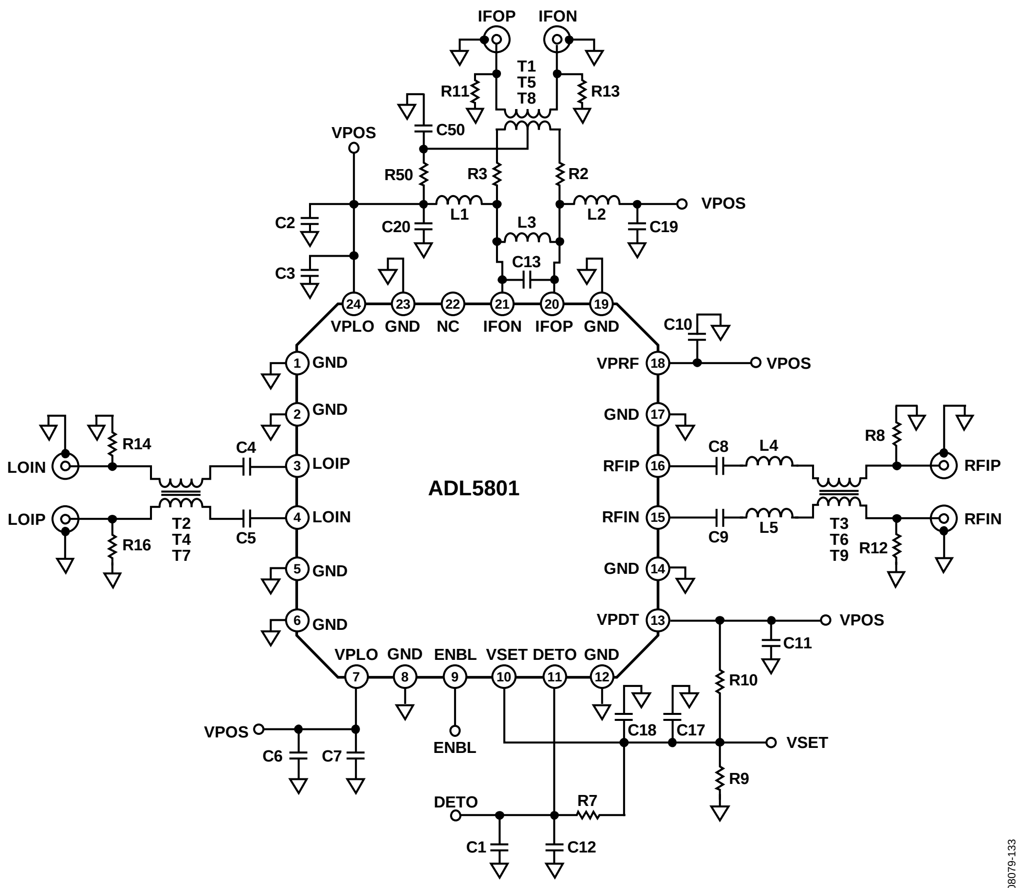

Figure 106. Evaluation Board Schematic

Table 8. Evaluation Board Configuration

Components	Function	Default Conditions
C2, C3, C6, C7, C10, C11	Power supply decoupling. Nominal supply decoupling consists of a 0.1 µF capacitor to ground in parallel with 100 pF capacitors to ground, positioned as close to the device as possible. Series resistors are provided for enhanced supply decoupling using optional ferrite chip inductors.	C2, C6, C10, C11 = 0.1 µF (size 0402) C3, C7 = 100 pF (size 0402)
C8, C9, L4, L5, R4, R8, R12, T3, T6, T9, RFIN, RFIP	RF input interfaces. (Use RFIN for operation). Input channels are ac-coupled through C8 and C9. R8 and R12 provide options when additional matching is needed. T3 is a 1:1 balun used to interface to the 50 Ω differential inputs. T6 and T9 provide options when high frequency baluns are used and require smaller balun footprints.	C8, C9 = 1 nF (size 0402) L4, L5 = 0 Ω (size 0402) R12 = open (size 0402) R4, R8 = 0 Ω (size 0402) T3 = TCM1-63AX+ (Mini-Circuits)
C13, C19, C20, C50, L1, L2, L3, R2, R3, R11, R13, R50, T1, T5, T8, IFON, IFOP	IF output interfaces. The 200 Ω open collector IF output interfaces are biased through the center tap of a 4:1 impedance transformer at T1. C50 provides local bypassing with R50 available for additional supply bypassing. L1 and L2 provide options when pull-up choke inductors are used to bias the open-collector outputs. C13, L3, R2, and R3 are provided for IF filtering and matching options. T5 and T8 provide options when high frequency baluns are used and require smaller balun footprints.	C13 = open (size 0402) C19, C20 = 100 pF (size 0402) C50 = 0.1 µF (size 0402) L1, L2 = open (size 0805) L3 = open (size 0402) R2, R3, R13, R50 = 0 Ω (size 0402) R11 = open (size 0402) T1 = TC4-1W+ (Mini-Circuits)
C4, C5, R14, R16, T2, T4, T7, LOIN, LOIP	LO interface. (Use LOIN for operation). C4 and C5 provide ac coupling for the local oscillator input. T2 is a 1:1 balun that allows single-ended interfacing to the differential 50 Ω local oscillator input. T4 and T7 provide options when high frequency baluns are used and require smaller balun footprints.	C4, C5 = 1 nF (size 0402) R14 = open (size 0402) R16 = 0 Ω (size 0402) T2 = TCM1-63AX+
C1, C12, R7, DETO	DETO interface. C1 and C12 provide decoupling for the DETO pin. R7 provides access to the VSET pin when automatic input IP3 control is needed.	C1 = 0.1 µF (size 0603) C12 = 100 pF (size 0402) R7 = open (size 0402)
C17, C18, R9, R10, VSET	VSET bias control. C17 and C18 provide decoupling for the VSET pin. R9 and R10 form an optional resistor divider network between VPOS and GND, allowing for a fixed bias setting. Supply 3.8 V at the VSET pin when the DETO pin is not connected for automatic input IP3 control.	C17 = 100 pF (size 0402) C18 = 0.1 µF (size 0603) R9, R10 = open (size 0402)

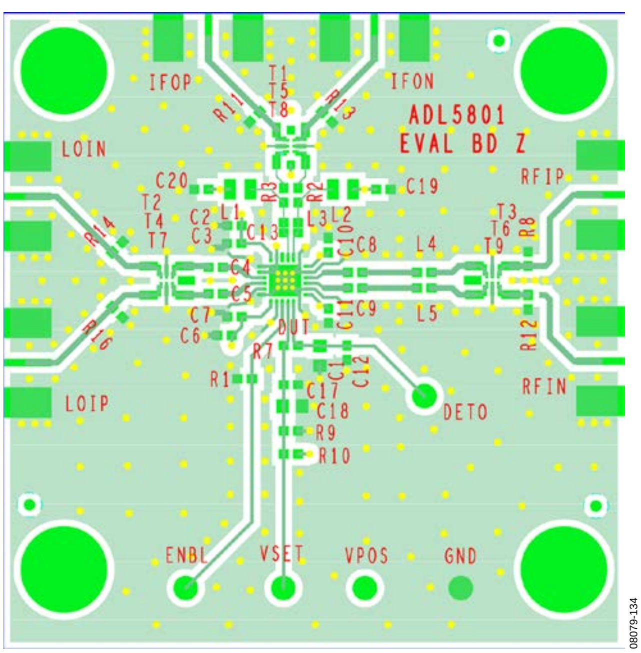

Figure 107. Evaluation Board Top Layer

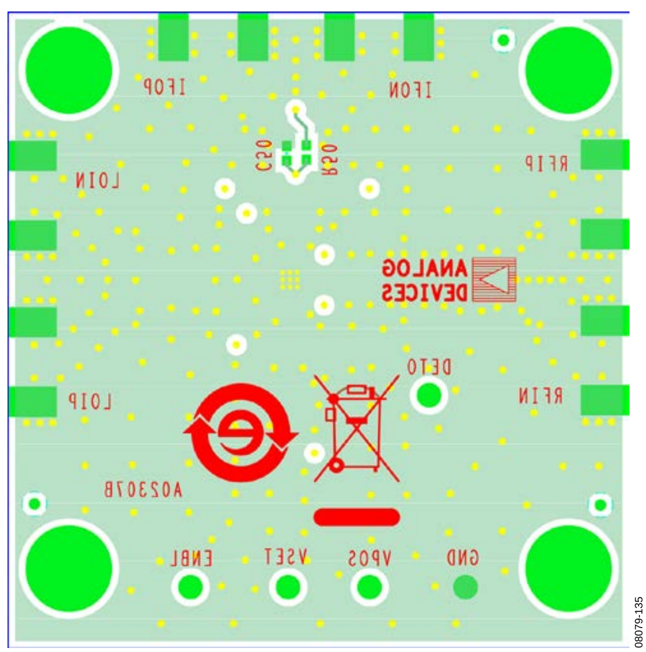

Figure 108. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

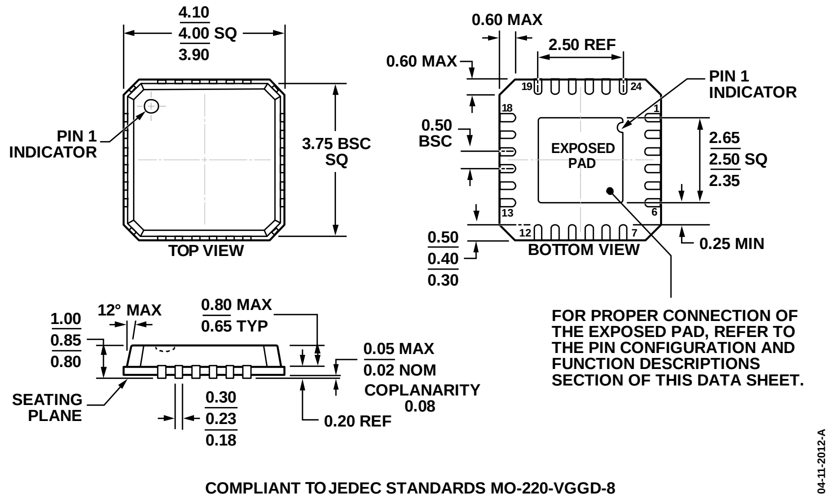

Figure 109. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad (CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5801ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-3	1,500 per Reel
ADL5801-EVALZ		Evaluation Board		1

[1] Z = RoHS Compliant Part.

NOTES