Isolated Precision Half-Bridge Driver, 4.0 A Output

Data Sheet

ADuM7223

FEATURES

- 4.0 A peak output current
- Working voltage
  - High-side or low-side relative to input: 565 V peak
  - High-side to low-side differential: 700 V peak
- High frequency operation: 1 MHz maximum
- Precise timing characteristics
  - 64 ns maximum propagation delay
  - 8.5 ns maximum channel-to-channel matching
- 3.0 V to 5.5 V input voltage
- 4.5 V to 18 V output drive
- UVLO supply at 2.8 V V_{DD1}
  - A Version UVLO, V_{DDA} and V_{DDB} (V_{DD2}) at 4.1 V
- CMOS input logic levels
- High common-mode transient immunity: >25 kV/µs
- High junction temperature operation: 125°C
- Default low output
- 5 mm × 5 mm, 13-terminal LGA

APPLICATIONS

- Switching power supplies
- Isolated IGBT/MOSFET gate drives
- Industrial inverters

GENERAL DESCRIPTION

The ADuM7223 is a 4.0 A isolated, half-bridge gate driver that employ Analog Devices, Inc., *i*Coupler® technology to provide independent and isolated high-side and low-side outputs. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as the combination of pulse transformers and non-isolated gate drivers. By integrating the isolator and driver in a single package, propagation delay is a maximum of only 64 ns, and the propagation skew from channel to channel is a maximum of only 12 ns at 12 V.

The ADuM7223 provides two independent isolation channels. The ADuM7223 operates with an input supply ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems. The outputs operate in a wide range from 4.5 V to 18 V with three output voltage versions available. The 5 mm × 5 mm, LGA package provides 565 V operating voltage from input to output and 700 V from output to output.

In comparison to gate drivers employing high voltage level translation methodologies, this gate driver offers the benefit of true, galvanic isolation between the input and each output. As a result, this gate driver provides reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

FUNCTIONAL BLOCK DIAGRAM

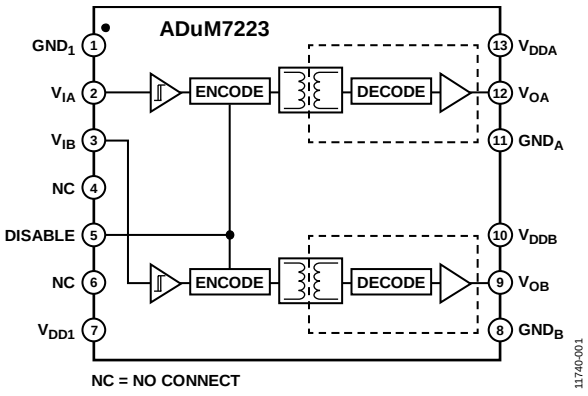

Figure 1.

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REVISION HISTORY

10/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to +125°C. All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 12 V. Switching specifications are tested with CMOS signal levels.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI(Q)}$		1.4	2.4	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$		2.3	3.5	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.6	2.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{DDB} Supply Current	$I_{DDA(Q)}$, $I_{DDB(Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	−1	+0.01	+1	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD2} − 0.1	V_{DD2}		V	I_{Ox} = −20 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox} = 20 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout, V_{DD1} Supply						
Positive Going Threshold	V_{DD1UV+}		2.8		V	
Negative Going Threshold	V_{DD1UV-}		2.6		V	
Hysteresis	V_{DD1UVH}		0.2		V	
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A-Grade
Negative Going Threshold	V_{DD2UV-}	3.2	3.6		V	A-Grade
Hysteresis	V_{DD2UVH}		0.5		V	A-Grade
Output Short-Circuit Pulsed Current[1]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DD2} = 12 V
Output Source Resistance	R_{OA}, R_{OB}	0.25	0.95	1.5	Ω	V_{DD2} = 12 V, I_{Ox} = −250 mA
Output Sink Resistance	R_{OA}, R_{OB}	0.55	0.6	1.35	Ω	V_{DD2} = 12 V, I_{Ox} = 250 mA
THERMAL SHUTDOWN TEMPERATURES						
Junction Temperature Shutdown Rising Edge	T_{JR}		150		°C	
Junction Temperature Shutdown Falling Edge	T_{JF}		140		°C	
SWITCHING SPECIFICATIONS						See Figure 16
Pulse Width[2]	PW	50			ns	C_L = 2 nF, V_{DD2} = 12 V
Maximum Data Rate[3]		1			MHz	C_L = 2 nF, V_{DD2} = 12 V
Propagation Delay[4]	t_{DHL}, t_{DLH}	19	40	62	ns	C_L = 2 nF, V_{DD2} = 12 V
ADuM7223A		25	46	68	ns	C_L = 2 nF, V_{DD2} = 4.5 V
Propagation Delay Skew[5]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 12 V
Channel-to-Channel Matching[6]	t_{PSKCD}					
V_{DD2} = 12 V			1	8.5	ns	C_L = 2 nF
V_{DD2} = 4.5 V			1	8.5	ns	C_L = 2 nF
Output Rise/Fall Time (10% to 90%)	t_R/t_F	1	12	24	ns	C_L = 2 nF, V_{DD2} = 12 V
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	V_{DD2} = 12 V
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		1.65		mA/Mbps	V_{DD2} = 12 V
Refresh Rate	f_r		1.2		Mbps	V_{DD2} = 12 V

[1] Short-circuit duration less than 1 µs. Average power must conform to the limit shown under the Absolute Maximum Ratings.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[4] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 16 for waveforms of propagation delay parameters.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between ADuM7223 units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 16 for waveforms of propagation delay parameters.
[6] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to 125°C. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 12 V. Switching specifications are tested with CMOS signal levels.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current ,Quiescent	$I_{DDI (Q)}$		0.87	1.4	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		2.3	3.5	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.1	1.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{DDB} Supply Current	$I_{DDA (Q)}$, $I_{DDB (Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	−1	+0.01	+1	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OAH}	V_{DD2} − 0.1	V_{DD2}		V	I_{Ox} = −20 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox} = 20 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout, V_{DD1} Supply						
Positive Going Threshold	V_{DD1UV+}		2.8		V	
Negative Going Threshold	$V_{DD1UV−}$		2.6		V	
Hysteresis	V_{DD1UVH}		0.2		V	
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A-Grade
Negative Going Threshold	$V_{DD2UV−}$	3.2	3.6		V	A-Grade
Hysteresis	V_{DD2UVH}		0.5		V	A-Grade
Output Short-Circuit Pulsed Current[1]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DD2} = 12 V
Output Source Resistance	R_{OA}, R_{OB}	0.25	0.95	1.5	Ω	V_{DD2} = 12 V, I_{Ox} = −250 mA
Output Sink Resistance	R_{OA}, R_{OB}	0.55	0.6	1.35	Ω	V_{DD2} = 12 V, I_{Ox} = 250 mA
THERMAL SHUTDOWN TEMPERATURES						
Junction Temperature Shutdown Rising Edge	T_{JR}		150		°C	
Junction Temperature Shutdown Falling Edge	T_{JF}		140		°C	
SWITCHING SPECIFICATIONS						See Figure 16
Pulse Width[2]	PW	50			ns	C_L = 2 nF, V_{DD2} = 12 V
Maximum Data Rate[3]		1			MHz	C_L = 2 nF, V_{DD2} = 12 V
Propagation Delay[4]	t_{DHL}, t_{DLH}	25	44	64	ns	C_L = 2 nF, V_{DD2} = 12 V
ADuM7223A		28	49	71	ns	C_L = 2 nF, V_{DD2} = 4.5 V
Propagation Delay Skew[5]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 12 V
Channel-to-Channel Matching[6]						
V_{DD2} = 12 V	t_{PSKCD}		1	8.5	ns	C_L = 2 nF
V_{DD2} = 4.5 V	t_{PSKCD}		1	8.5	ns	C_L = 2 nF
Output Rise/Fall Time (10% to 90%)	t_R/t_F	1	12	24	ns	C_L = 2 nF, V_{DD2} = 12 V
Dynamic Input Supply Current per Channel	$I_{DDI (D)}$		0.05		mA/Mbps	V_{DD2} = 12 V
Dynamic Output Supply Current per Channel	$I_{DDO (D)}$		1.65		mA/Mbps	V_{DD2} = 12 V
Refresh Rate	f_r		1.1		Mbps	V_{DD2} = 12 V

[1] Short-circuit duration less than 1 µs. Average power must conform to the limit shown under the Absolute Maximum Ratings.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
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[4] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 16 for waveforms of propagation delay parameters.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 16 for waveforms of propagation delay parameters.
[6] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		96.3		°C/W	
IC Junction-to-Case Thermal Resistance	θ_{JC}		43.2		°C/W	

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Functional Dielectric Insulation Voltage[1]		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	3.5 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	3.5 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

[1] Insulation voltage guaranteed by design, not tested in production. Insulation is similar in structure to devices that are tested to 5 kV rms in production.

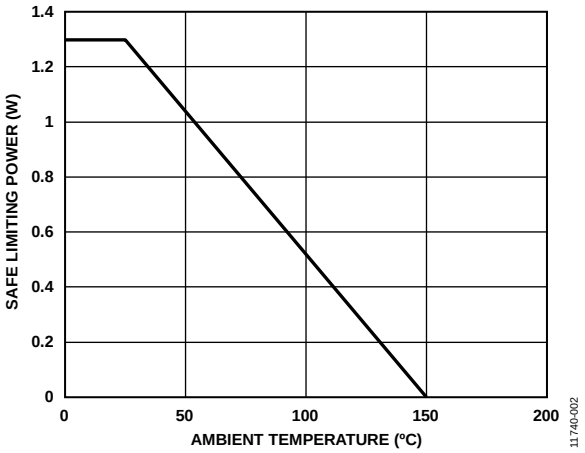

Figure 2. Thermal Derating Curve

RECOMMENDED OPERATING CONDITIONS

Table 5.

Parameter	Symbol	Min	Max	Unit
Operating Junction Temperature	T_J	−40	+125	°C
Supply Voltages[1]	V_{DD1}	3.0	5.5	V
	V_{DDA}, V_{DDB}	4.5	18	V
Maximum Input Signal Rise and Fall Times	T_{VIA}, T_{VIB}		1	ms
Common-Mode Transient Static[2]		−50	+50	kV/µs
Common-Mode Transient Immunity Dynamic[3]		−25	+25	kV/µs

[1] All voltages are relative to their respective ground. See the Applications Information section for information on immunity to external magnetic fields.
[2] Static common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_A/GND_B with inputs held either high or low such that the output voltage remains either above $0.8 \times V_{DD2}$ for V_{IA}/V_{IB} = high, or 0.8 V for V_{IA}/V_{IB} = low. Operation with transients above recommended levels can cause momentary data upsets.
[3] Dynamic common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_A/GND_B with switching edge coincident with the transient test pulse. Operation with transients above recommended levels can cause momentary data upsets.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 6.

Parameter	Symbol	Rating
Storage Temperature	T_{ST}	−55°C to +150°C
Operating Junction Temperature	T_J	−40°C to +150°C
Supply Voltages[1]	V_{DD1}	−0.3 V to +6.0 V
	V_{DD2}	−0.3 V to +20 V
Input Voltage[1, 2]	V_{IA}, V_{IB}	−0.3 V to V_{DDI} + 0.3 V
Output Voltage[1, 2]	V_{OA}, V_{OB}	−0.3 to V_{DDO} + 0.3 V
Average Output Current, per Pin[3]	I_O	−35 mA to +35 mA
Common-Mode Transients[4]	CM_H, CM_L	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 2 for information on maximum allowable current for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 7. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	50-year minimum lifetime
DC Voltage			
Functional Insulation	1131	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 8. Truth Table (Positive Logic)[1]

DISABLE	V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DDA}/V_{DDB} State	V_{OA} Output	V_{OB} Output	Notes
L	L	L	Powered	Powered	L	L	Outputs return to the input state within 1 µs of DISABLE = set to low.
L	L	H	Powered	Powered	L	H	Outputs return to the input state within 1 µs of DISABLE = set to low.
L	H	L	Powered	Powered	H	L	Outputs return to the input state within 1 µs of DISABLE = set to low.
L	H	H	Powered	Powered	H	H	Outputs return to the input state within 1 µs of DISABLE = set to low.
H	X	X	Powered	Powered	L	L	Outputs take on default low state within 3 µs of DISABLE = set to high.
L	L	L	Unpowered	Powered	L	L	Outputs return to the input state within 1 µs of V_{DD1} power restoration.
X	X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 50 µs of V_{DDA}/V_{DDB} power restoration.

[1] X = don't care.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

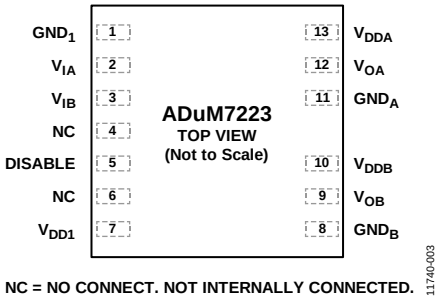

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND_1	Ground Reference for Input Logic Signals.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4, 6	NC	No Connect. Not internally connected.
5	DISABLE	Input Disable. Disables the isolator inputs and refresh circuits. Outputs take on default low state.
7	V_{DD1}	Input Supply Voltage.
8	GND_B	Ground Reference for Output B.
9	V_{OB}	Output B.
10	V_{DDB}	Output B Supply Voltage.
11	GND_A	Ground Reference for Output A.
12	V_{OA}	Output A.
13	V_{DDA}	Output A Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

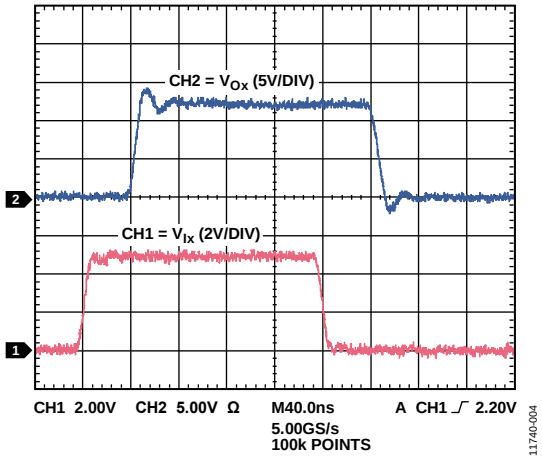

Figure 4. Output Waveform for 2 nF Load with 12 V Output Supply

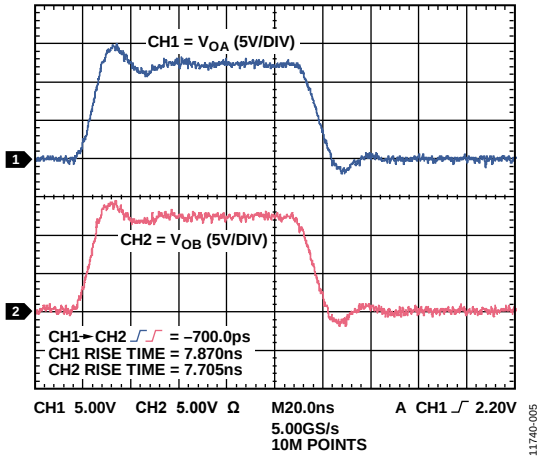

Figure 5. Output Matching and Rise Time Waveforms for 2 nF Load with 12 V Output Supply

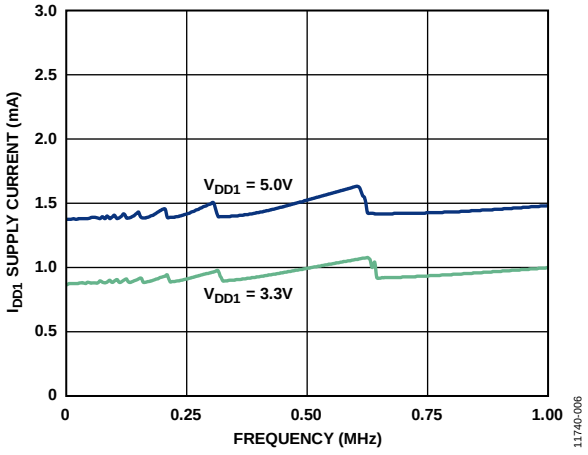

Figure 6. Typical I_{DD1} Supply Current vs. Frequency

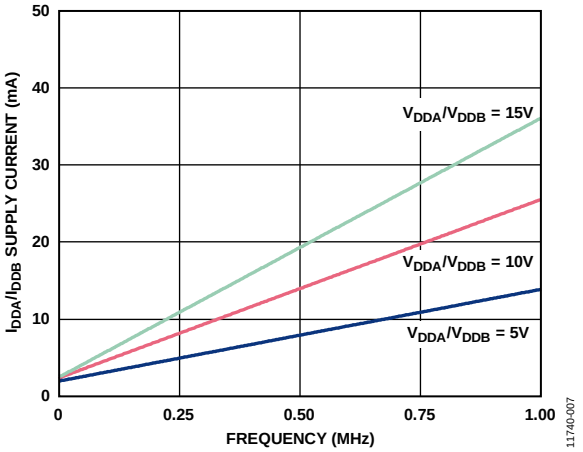

Figure 7. Typical I_{DDA}/I_{DDB} Supply Current vs. Frequency with 2 nF Load

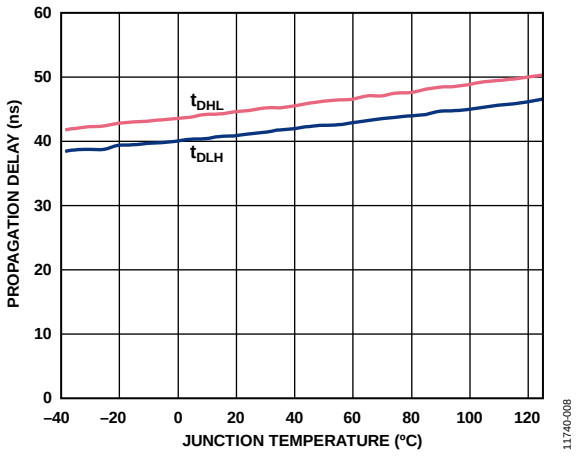

Figure 8. Typical Propagation Delay vs. Junction Temperature

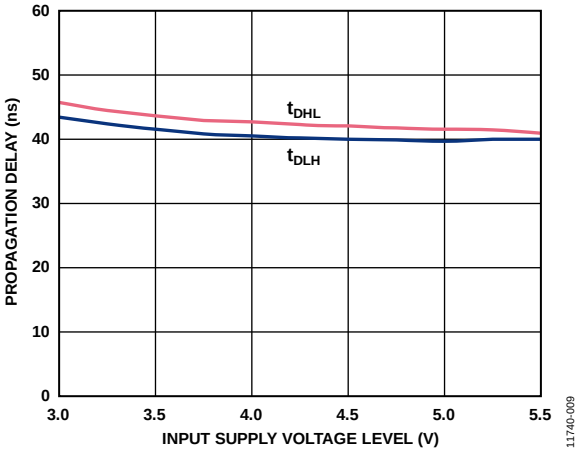

Figure 9. Typical Propagation Delay vs. Input Supply Voltage, V_{DDA}/V_{DDB} = 12 V

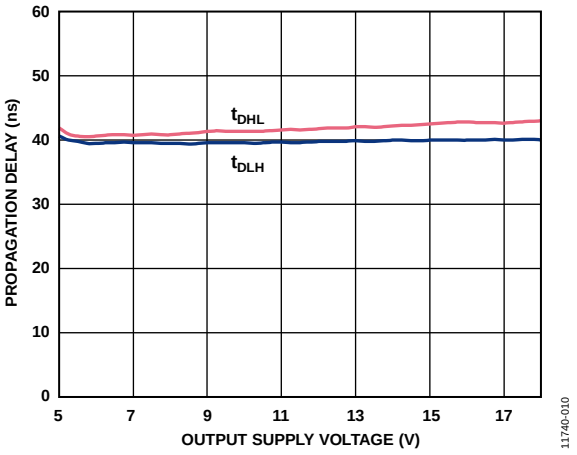

Figure 10. Typical Propagation Delay vs. Output Supply Voltage, V_{DD1} = 5 V

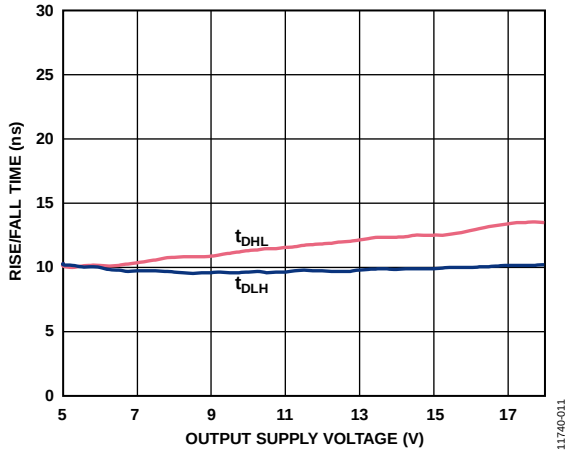

Figure 11. Typical Rise/Fall Time vs. Output Supply Voltage

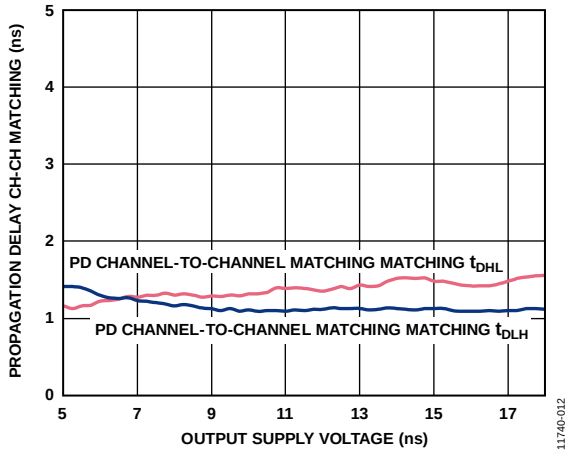

Figure 12. Typical Propagation Delay, Channel-to-Channel Matching vs. Output Supply Voltage

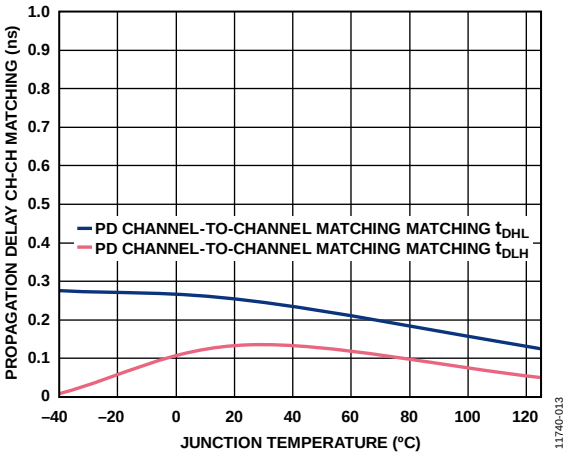

Figure 13. Typical Propagation Delay (PD) Channel-to-Channel Matching vs. Temperature, V_{DDA}/V_{DDB} = 12 V

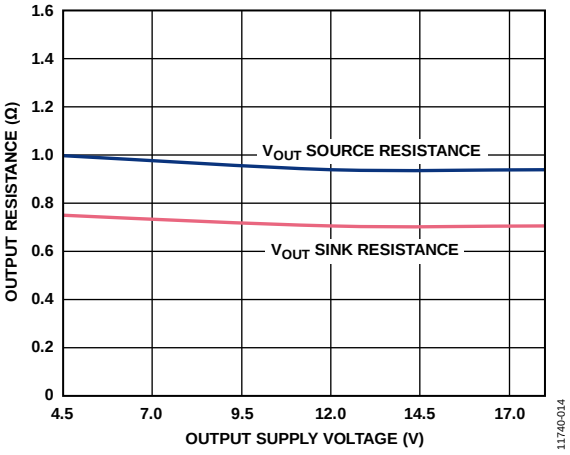

Figure 14. Typical Output Resistance vs. Output Supply Voltage

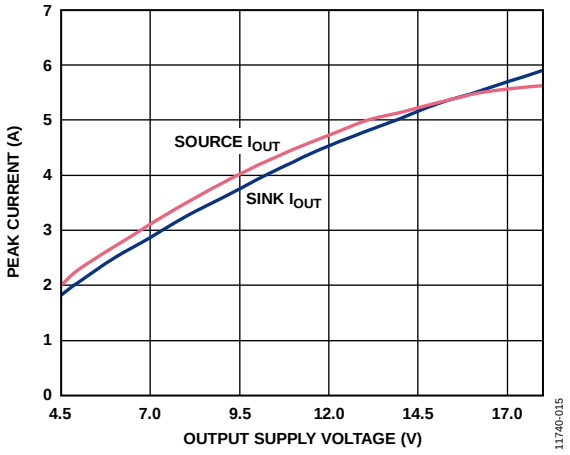

Figure 15. Typical Peak Output Current vs. Output Supply Voltage, 1.2 Ω Series Resistance

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM7223 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a good high frequency bypass. On the output power supply pins, V_{DDA} or V_{DDB}, it is recommended to add a 10 µF capacitor in parallel to provide the charge required to drive the gate capacitance at the ADuM7223 outputs. On the output supply pins, avoid bypass capacitor use of vias, or employ multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed 20 mm for best performance. For best performance, place bypass capacitors as near to the device as possible.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM7223 specifies t_{DLH} as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold (see Figure 16). Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, as is the industry standard for gate drivers.

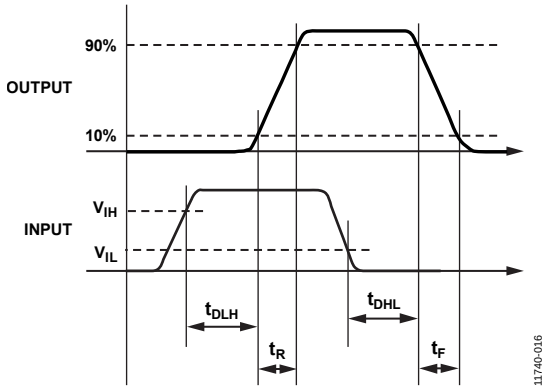

Figure 16. Propagation Delay Parameters

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM7223 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM7223 devices operating under the same conditions.

THERMAL LIMITATIONS AND SWITCH LOAD CHARACTERISTICS

For isolated gate drivers, the necessary separation between the input and output circuits prevents the use of a single thermal pad beneath the device, and heat is, therefore, dissipated mainly through the package pins.

Power dissipation within the device is primarily driven by the effective load capacitance being driven, switching frequency, operating voltage, and external series resistance. Power dissipation within each channel can be calculated by

$$P_{DISSs} = C_{EFF} \times (V_{DDA} / V_{DDB})^2 \times f_{SW} \frac{R_{DSON}}{R_{DSON} + R_{GATE}}$$

where:
C_{EFF} is the effective capacitance of the load.
$V_{DDA/B}$ is the secondary side voltage.
f_{SW} is the switching frequency.
R_{DSON} is the internal resistance of the ADuM7223 (R_{OA}, R_{OB}).
R_{GATE} is the external gate resistor.

To find temperature rise above ambient temperature, multiply total power dissipation by the θ_{JA}, which is then added to the ambient temperature to find the approximate internal junction temperature of the ADuM7223.

Each of the ADuM7223 isolator outputs have a thermal shutdown protection function. This function sets an output to a logic low level when the rising junction temperature typically reaches 150°C and turns back on after the junction temperature has fallen from the shutdown value by about 10°C.

OUTPUT LOAD CHARACTERISTICS

The ADuM7223 output signals depend on the characteristics of the output load, which is typically an N-channel MOSFET. The driver output response to an N-channel MOSFET load can be modeled with a switch output resistance (R_{SW}), an inductance due to the PCB trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate to source capacitance (C_{GS}), as shown in Figure 17.

R_{SW} is the switch resistance of the internal ADuM7223 driver output (1.1 Ω typical for turn-on and 0.6 Ω for turn-off). R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4 A gate driver has a typical intrinsic gate resistance of about 1 Ω and a gate-to-source capacitance (C_{GS}) of between 2 nF and 10 nF. L_{TRACE} is the inductance of the PCB trace, typically a value of 5 nH or less for a well-designed layout with a very short and wide connection from the ADuM7223 output to the gate of the MOSFET.

The following equation defines the Q factor of the RLC circuit, which indicates how the ADuM7223 output responds to a step change. For a well-damped output, Q is less than one. Adding a series gate resistance dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

To reduce output ringing, add a series gate resistance to dampen the response. For applications using a load of 1 nF or less, add a series gate resistor of about 5 Ω. It is recommended that the Q factor be below 1 which results in a damped system, with a value of 0.7 as the recommended target.

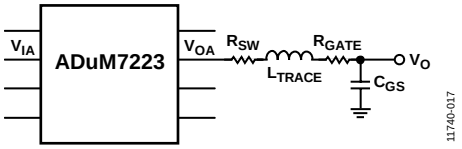

Figure 17. RLC Model of the Gate of an N-Channel MOSFET

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 1 µs (typical) at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no internal pulses for more than about 3 µs (typical), the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit. In addition, the outputs are in a low default state while the power is coming up before the UVLO threshold is crossed.

The limitation on the ADuM7223 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM7223 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM7223 and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 18.

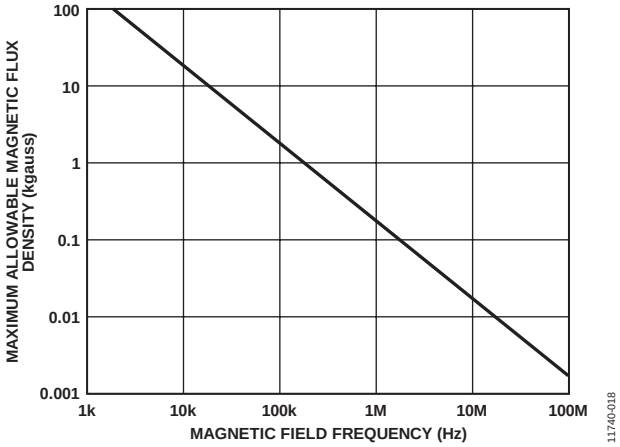

Figure 18. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM7223 transformers. Figure 19 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM7223 is immune and only affected by extremely large currents operated at a high frequency and near the component. For the 1 MHz example, place a 0.5 kA current 5 mm away from the ADuM7223 to affect the operation of the component.

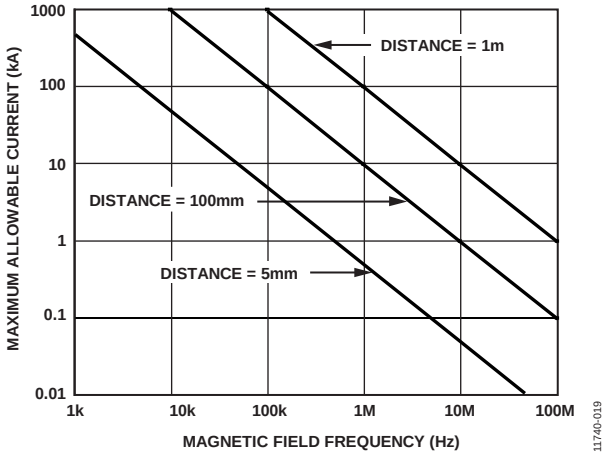

Figure 19. Maximum Allowable Current for Various Current to ADuM7223 Spacings

POWER CONSUMPTION

The supply current at a given channel of the ADuM7223 isolator is a function of the supply voltage, channel data rate, and channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI(\,Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

C_L is the output load capacitance (nF).

V_{DDO} is the output supply voltage (V).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 6 provides total input I_{DD1} supply current as a function of data rate for both input channels. Figure 7 provides total I_{DD2} supply current as a function of data rate for both outputs loaded with 2 nF capacitance.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM7223.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 7 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than a 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM7223 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 20, Figure 21, and Figure 22 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products and is the 50-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. Treat any cross-insulation voltage waveform that does not conform to Figure 21 or Figure 22 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 7.

Note that the voltage presented in Figure 21 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

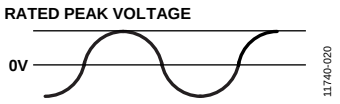

Figure 20. Bipolar AC Waveform

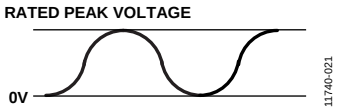

Figure 21. Unipolar AC Waveform

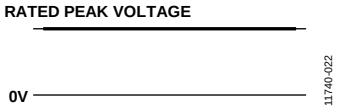

Figure 22. DC Waveform

OUTLINE DIMENSIONS

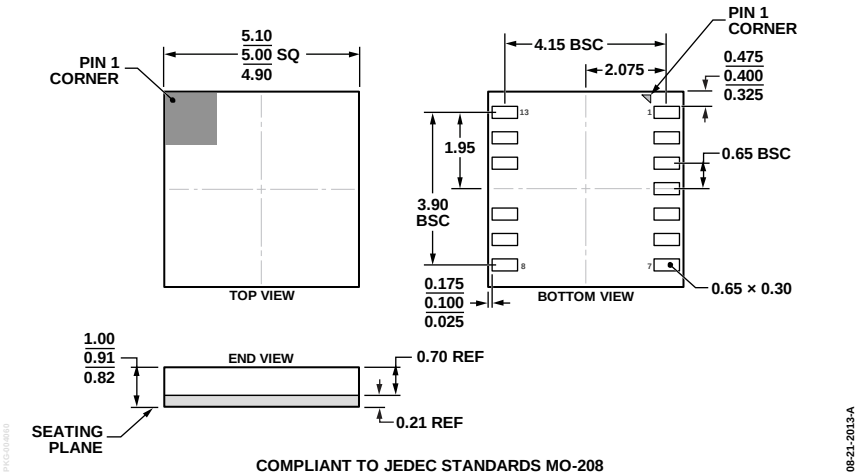

Figure 23. 13-Terminal Land Grid Array [LGA]
(CC-13-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	No. of Channels	Output Peak Current (A)	Minimum Output Voltage (V)	Junction Temperature Range	Package Description	Package Option	Ordering Quantity
ADuM7223ACCZ	2	4	4.5	−40°C to +125°C	13-Terminal LGA	CC-13-1	
ADuM7223ACCZ-RL7	2	4	4.5	−40°C to +125°C	13-Terminal LGA, 7″ Tape and Reel	CC-13-1	1,000

[1] Z = RoHS Compliant Part.

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