AN291

OUTPUT BUFFER OPTIONS FOR Si53x/55x/57x/59x XO/VCXO DEVICES

1. Introduction

The Si53x/55x/57x/59x XO/VCXO devices can be ordered with one of four different output buffer types: CMOS, LVPECL, LVDS, or CML. Each output type has its own particular benefits and disadvantages. This document describes each buffer type, proper biasing and termination schemes, and related technical trade-offs.

2. CMOS

Complementary metal-oxide semiconductor (CMOS) outputs are typically chosen for the lowest output frequencies (below 160 MHz) because they do not offer constant, controlled output impedance. Without controlled output impedance, the length of the connected transmission line must be limited. The general rule is that if the line length approaches 1/4th the wavelength of the highest harmonic frequency, that line should be treated as a transmission line. CMOS can be ordered for all three of the supported supply levels (1.8, 2.5, and 3.3 V). Silicon Laboratories XOs and VCXOs support a nominal CMOS output voltage swing from ground to V_{DD}. CMOS is compatible with LVTTL I/O.

3. LVPECL

Low-voltage positive emitter-coupled logic (LVPECL) differential outputs are typically chosen for their compatibility with other high-speed ICs. This output type requires external biasing and proper termination of 50 Ω to V_{DD} minus 2 V for each side of the differential output. Many well-known LVPECL biasing and termination schemes are supported by the Si53x/55x/57x/59x devices. The most common are shown in Figures 1, 2, and 3. The primary disadvantages of this output format are increased power consumption (due to the 28 mA required for dc biasing) and incompatibility with 1.8 V supplies. The primary advantage of the LVPECL signal format is jitter performance. LVPECL provides the best jitter performance because of its large swing.

The Si53x/55x/57x/59x LVPECL driver is a CMOS instantiation that does not present a low output impedance similar to a traditional bipolar LVPECL driver. Therefore, we do not recommend termination approaches such as STECL (Source Terminated ECL) that do not use load terminations. If such an approach is required, contact the factory.

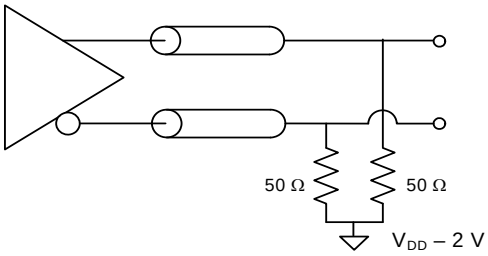

Figure 1. Traditional Biasing and Termination for LVPECL Output Buffers

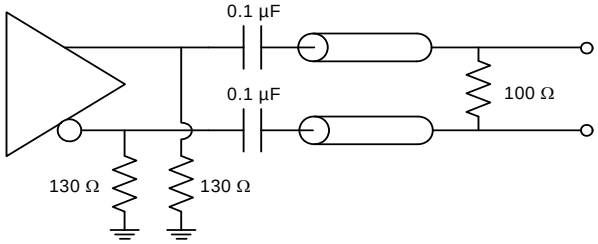

Figure 2. First Alternative Biasing and Termination for LVPECL Output Buffers (100 Ω Line Termination May Be Internal to the Receiving IC)

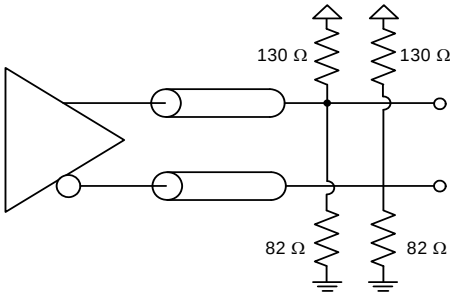

Figure 3. Second Alternative Biasing and Termination for LVPECL Output Buffers

4. LVDS

Low-voltage differential signaling (LVDS) differential outputs are typically chosen for newer designs because of their ease of implementation in CMOS ICs and because of their ease of use at the system level. LVDS outputs require no external biasing or termination when connected to LVDS inputs and are very power-efficient. Also, the LVDS specification allows for significant dc biasing drift from transmitter to receiver, further simplifying system-level design. The primary disadvantages of this output are reduced jitter performance when compared to LVPECL. The primary advantage is ease of use. LVDS outputs are connected as shown in Figure 4.

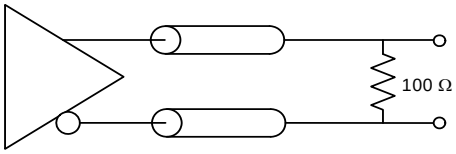

Figure 4. Typical Transmission Line Connection for LVDS
(100 Ω Line Termination May be Internal to the Receiving IC)

5. CML

Typically, current-mode logic (CML) differential outputs are chosen when LVPECL outputs are desired but lower power consumption is required. CML provides similar performance to LVPECL but does not require external biasing. CML outputs must be ac-coupled since they cannot provide sufficient current to bias other devices. CML outputs are connected as shown in Figures 5 and 6.

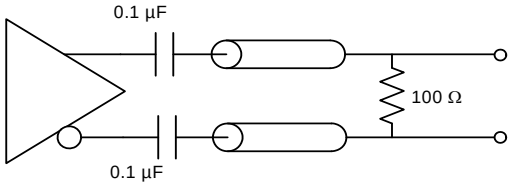

Figure 5. Typical CML Output Buffer Connection
(100 Ω Line Termination may be Internal to the Receiving IC)

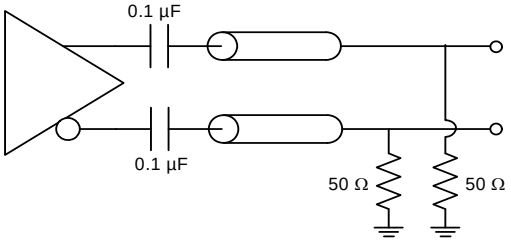

Figure 6. Alternative CML Output Buffer Connection

6. Relative Comparison

Figure 7 shows a relative comparison between jitter performance and power consumed. Generally, better performance requires more power.

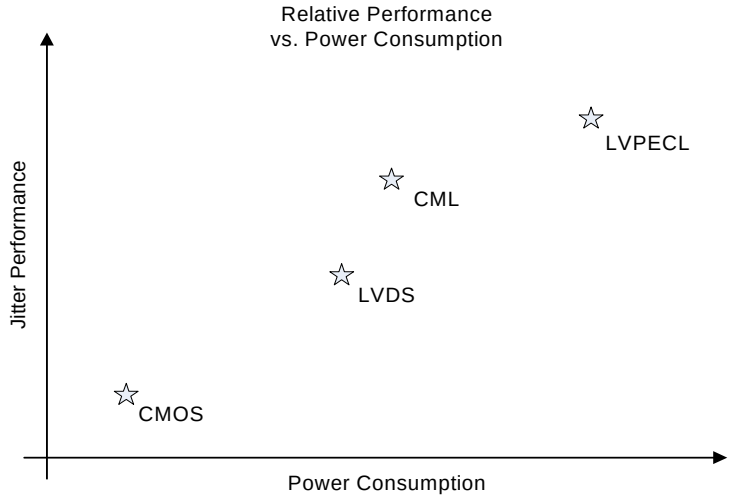

Figure 7. Relationship of Jitter Performance to Power Consumption

7. Conclusion

Because of the flexibility of Silicon Laboratories' XO/VCXO products, it is important that the system designer understand the benefits and trade-offs associated with common output buffer types so that the best output lock signal format can be chosen to optimize each design at the application level. LVPECL offers the best jitter performance followed by CML, LVDS, and finally CMOS. Choose LVPECL for applications where jitter is the primary concern. Power consumption is optimized by choosing CML or LVDS when appropriate. Other trade-offs may exist; so, if you are unsure which output buffer type to choose, please contact Silicon Laboratories directly at VCXOinfo@silabs.com.

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Added Si59x part number.

NOTES:

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