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## CS556x / 7x / 8x: Converting Output Data from Serial to Parallel

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### 1. Introduction

The CS556X, CS557X, and CS558X series of high-throughput Delta-Sigma A/D converters output data in serial format. Some applications may require that data be available in parallel format. This application note will discuss how to use common serial-to-parallel register ICs to provide parallel data output capability for these A/D converters.

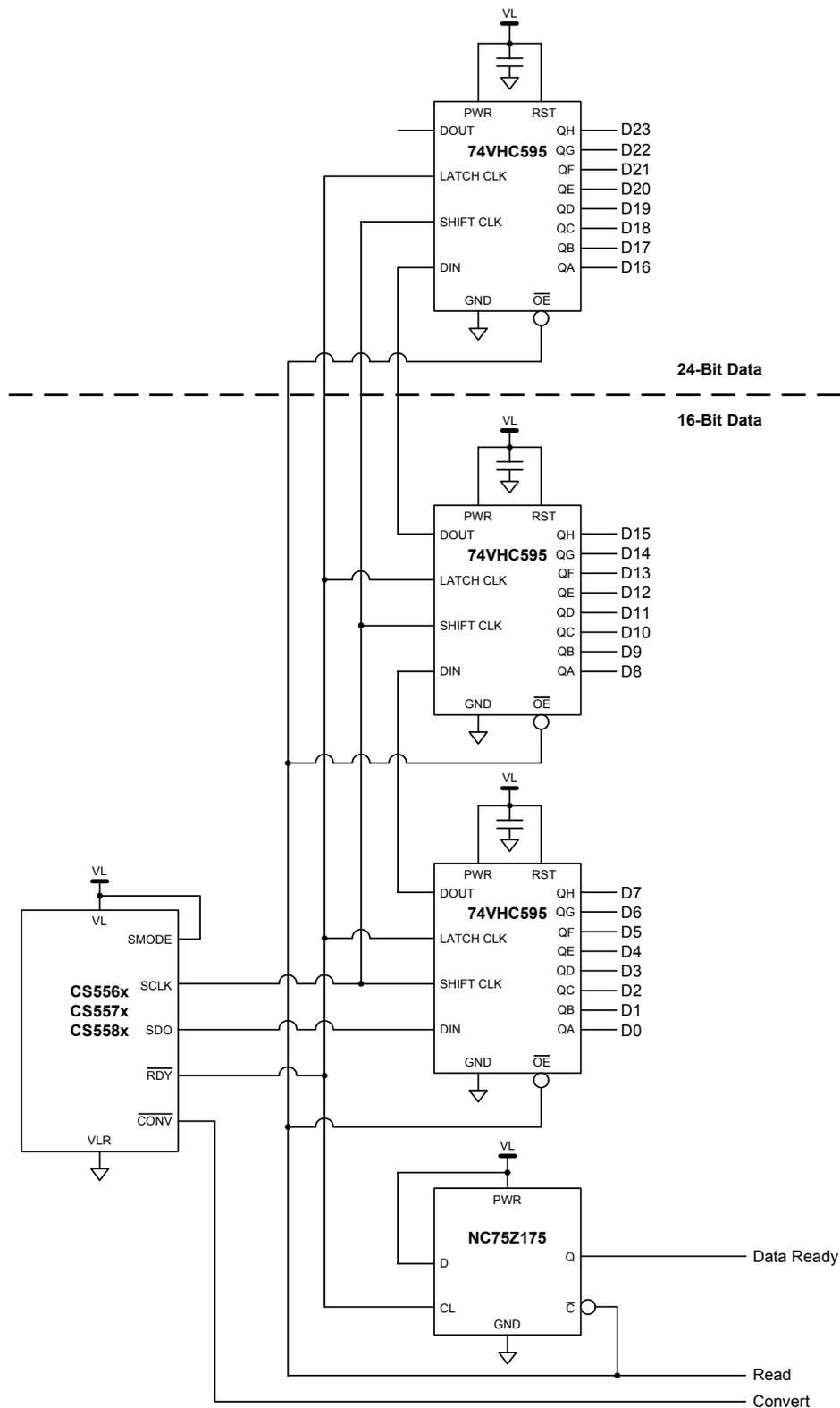
Some A/D converters provide parallel output data as an output option. While this makes for faster data transfer it can introduce some possible compromises in the performance of the A/D converter. A parallel interface requires many more pins on the A/D than a serial interface. This factor can increase the cost, but a larger concern should be how a parallel interface can reduce performance. The data interface has many more connections via bond wires to the semiconductor die. When the digital data on the digital bus is changing each bond wire acts as a radiator of an electromagnetic field. This electromagnetic field can interfere with the performance of the converter. The digital activity on the bus need not be due to the converter itself but may be caused by other peripherals using the same bus. Many A/D converters that have parallel interfaces recommend that bus activity be stopped when a conversion is performed, and that the data from the converter be read when the converter is not performing a conversion. Another option would be to provide a second set of latches outside the A/D to isolate the bus activity from being on the digital output pins of the converter itself.

### 2. The CS556x/7x/8x

Cirrus Logic has chosen to offer the CS556X/7X/8X series of converters with only a serial interface. This reduces the package pin count and also reduces the number of digital interface pins that can radiate noise onto the converter die. The serial interface provides two different modes of operation. The serial port on the converter can operate in either master mode, where the converter itself outputs the data according to its own timing (this mode is called the SSC mode, synchronous self-clock mode). The second mode is where the serial port acts as a slave device to an external controller, where the serial data is output from the port according to the clock provided by the external device (this mode is the SEC mode, synchronous external clock mode).

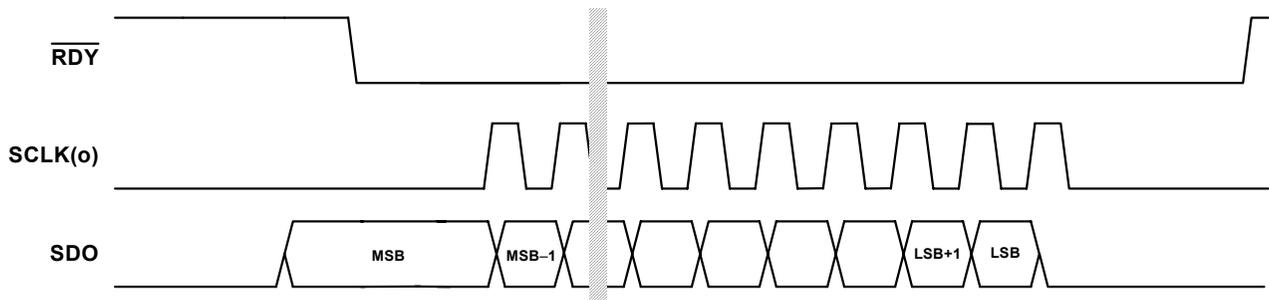
### 3. Serial-to-Parallel Conversion

If an application requires a parallel interface to read the converter data, then the A/D can be configured in the SSC serial port mode and directly interfaced to serial-to-parallel registers. Figure 1 illustrates the CS556x/7x/8x A/D converter interfaced to a set of 74VHC595 serial-to-parallel registers. The SMODE pin of the converter is tied to the VL supply (tied high) to set the serial port mode of the converter into the SSC (master) mode. At the end of each conversion the RDY output from the converter will transition low, and the SCLK and the SDO outputs will become active. The data bits from SDO will be shifted into the first 74VHC595 register by the rising edges of SCLK. The 74VHC595 device holds eight bits of data. Multiple 74VHC595 devices are daisy-chained to provide either a 16-bit parallel (two 74VHC595s) or a 24-bit parallel (three 74VHC595s) interface. The 74VHC595 has a tri-state output so the outputs of these devices can be attached to a multi-peripheral bus. The RDY signal will return high when all the bits from the converter have been shifted into the registers. When RDY transitions high it will set the NC75Z175 latch to provide a "data ready" signal at its Q output. When the read signal from the system goes low, the outputs of the 74VHC595 devices will come out of tri-state and place their data on the bus. The falling read signal will also clear the "data ready" signal back to a zero at the Q output of the NC75Z175 latch.



**Figure 1. CS556x/7x/8x Driving Serial-to-Parallel Registers**

Figure 2 shows the timing of the RDY/, SCLK, and SDO signals from the A/D converter.

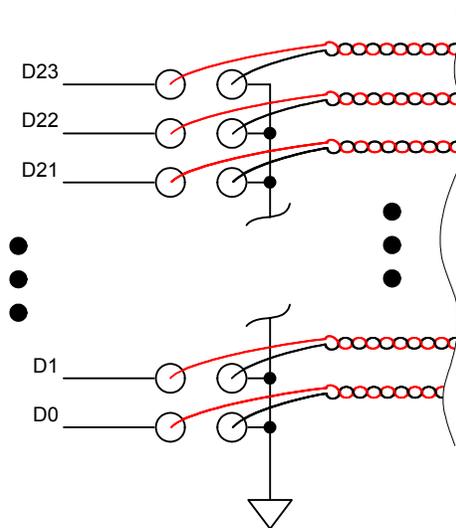


**Figure 2. CS556x/7x/8x Serial Data Output Signals**

## 4. Minimizing EMI

There are applications where output data from a converter must pass via a cable to another circuit board assembly. If this is required, each active signal should have its own ground wire “partner”. On a connector, such as a dual row stake header, each active signal should be paired with a ground signal. Any connecting cable should be constructed from twisted pair ribbon cable where each active signal has its own ground “partner” which is the other wire in the twisted pair. This minimizes radiated noise and reduces the likelihood that radiated noise will interfere with converter performance. It also enhances the likelihood that the system will pass any EMC (electromagnetic compatibility) requirements.

This wiring method is illustrated in Figure 3.



**Figure 3. Recommended Connector & Cable Configuration**

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## Revision History

Release	Date	Changes
REV1	JUN 2007	Initial Release

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## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest to you, go to <http://www.cirrus.com>

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