BUK969R3-100E

N-channel TrenchMOS logic level FET

5 October 2012 — Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with Vgst(th) rating of greater than 0.5V at 175 °C

1.3 Applications

- 12V, 24V and 48V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	100	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; Fig. 1		-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 2		-	-	263	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5$ V; $I_D = 25$ A; $T_j = 25$ °C; Fig. 11		-	7.49	9.3	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5$ V; $I_D = 25$ A; $V_{DS} = 80$ V; Fig. 13; Fig. 14		-	34	-	nC

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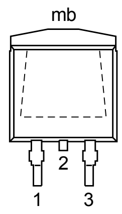
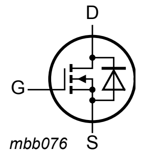
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK969R3-100E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
BUK969R3-100E	BUK969R3-100E

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ		-	100	V
V_{GS}	gate-source voltage	$T_j \leq 175$ °C; DC		-10	10	V
		$T_j \leq 175$ °C; Pulsed	[1][2]	-15	15	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 5$ V; Fig. 1		-	100	A
		$T_{mb} = 100$ °C; $V_{GS} = 5$ V; Fig. 1		-	71	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Fig. 4		-	405	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 2		-	263	W
T_{stg}	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	100	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C		-	405	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[3][4]	-	219	mJ

[1] Accumulated pulse duration up to 50 hours delivers zero defect ppm

[2] Significantly longer life times are achieved by lowering T_j and or V_{GS}

[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[4] Refer to application note AN10273 for further information.

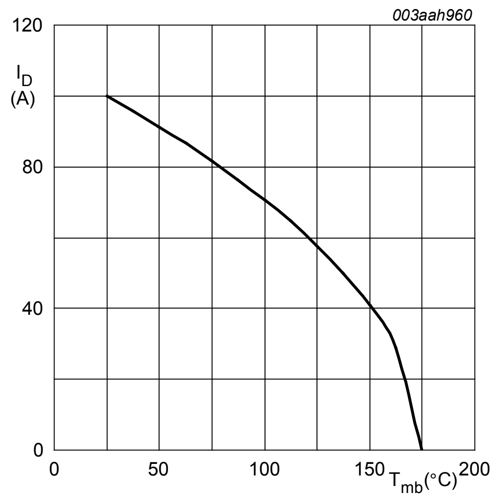


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

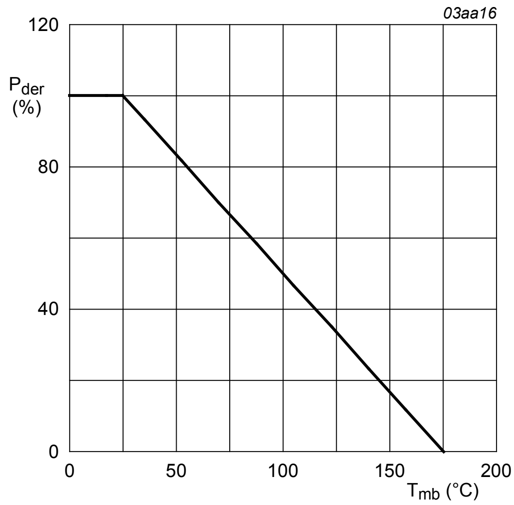


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

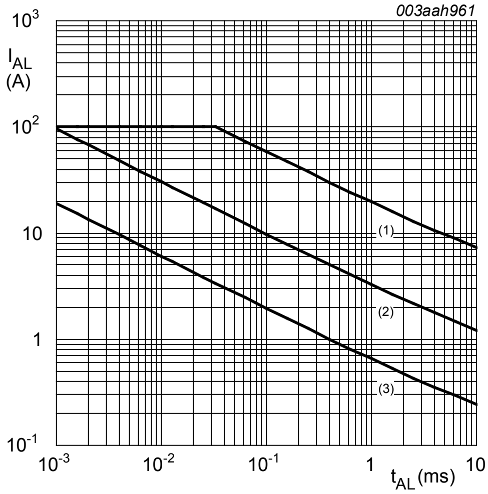


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 150°C$; (3) Repetitive Avalanche

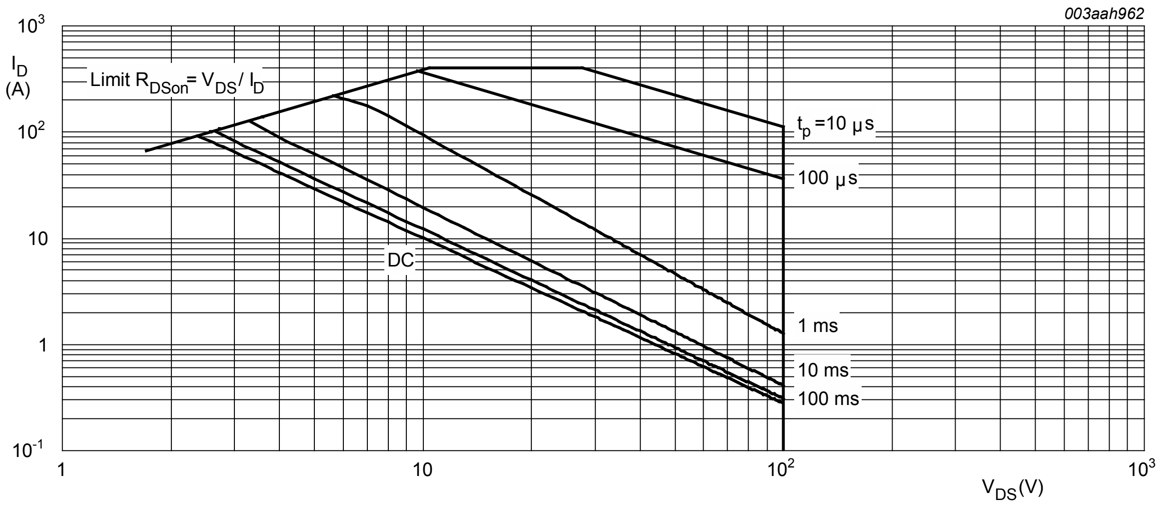


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} *is a single pulse*

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	0.57	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board		-	50	-	K/W

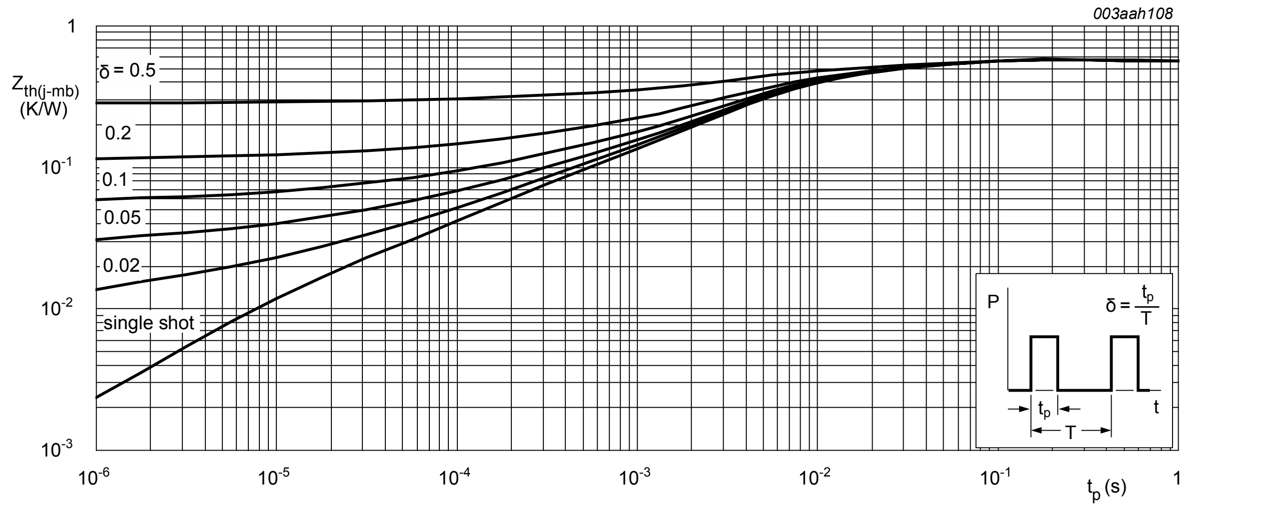


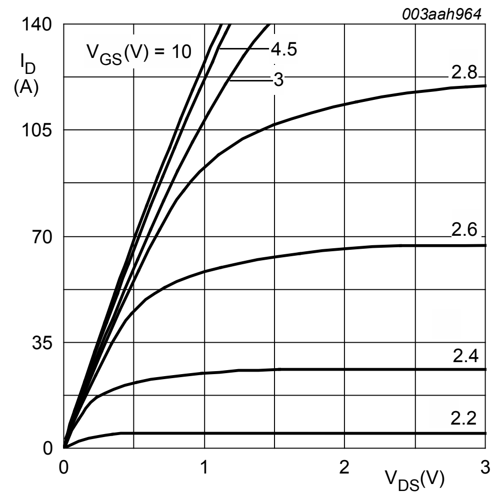
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 9		-	-	2.45	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 9		0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.06	1	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; Fig. 11		-	7.49	9.3	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		-	7.23	8.9	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; Fig. 12; Fig. 11		-	-	25.7	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 80 V; V_{GS} = 5 V; Fig. 13; Fig. 14		-	94.3	-	nC
Q_{GS}	gate-source charge			-	15.2	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GD}	gate-drain charge			-	34	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	8739	11650	pF
C_{oss}	output capacitance			-	499	599	pF
C_{rss}	reverse transfer capacitance			-	312	427	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 80 V; R_L = 3.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω		-	39.5	-	ns
t_r	rise time			-	95.1	-	ns
$t_{d(off)}$	turn-off delay time			-	118	-	ns
t_f	fall time			-	93.4	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V		-	55.5	-	ns
Q_r	recovered charge			-	142	-	nC



T_j = 25 °C; t_p = 300 µs

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

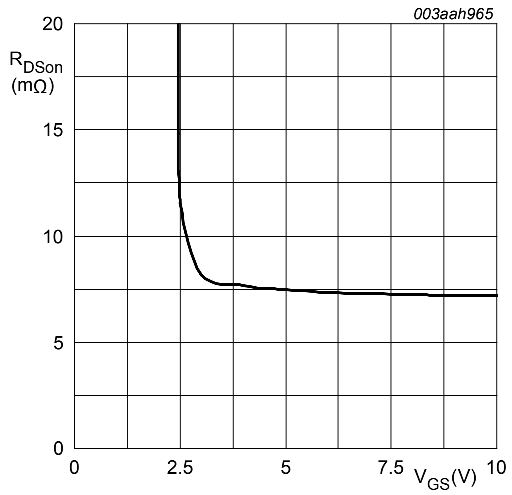


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 25A$

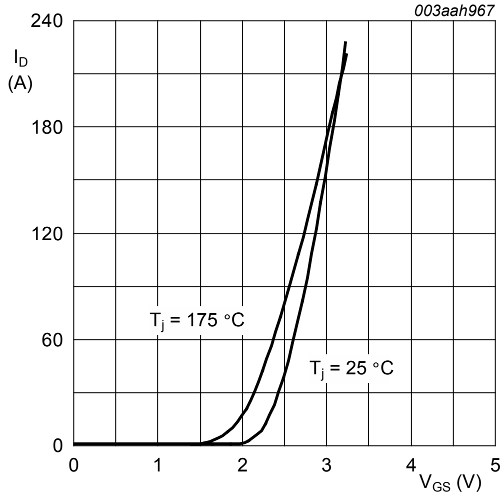


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10 V$

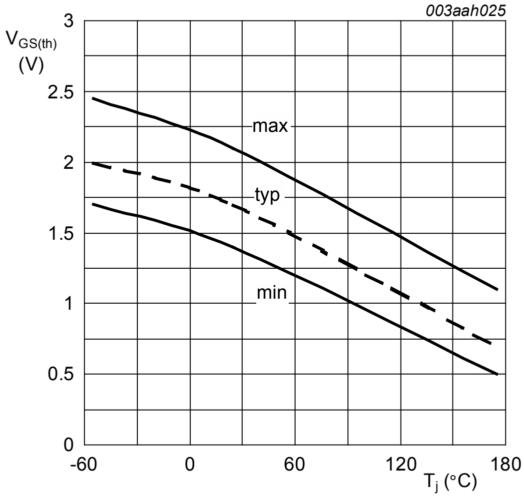


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1$ mA; $V_{DS} = V_{GS}$

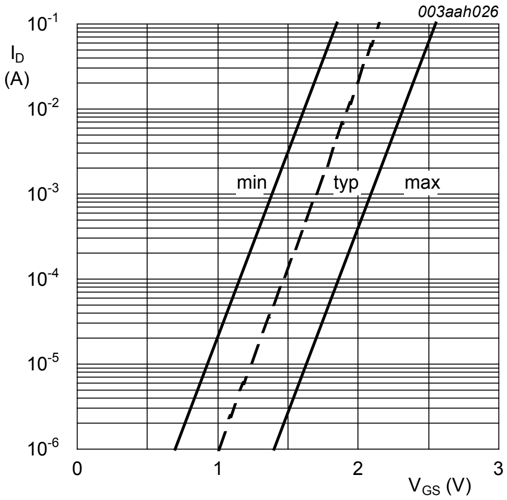
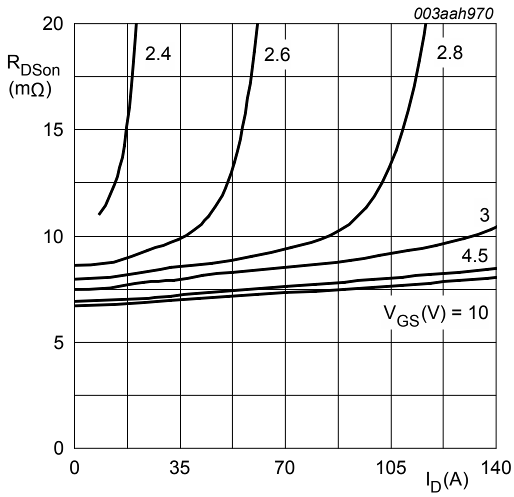


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C$; $V_{DS} = 5V$



T_j = 25 °C; t_p = 300 µs

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

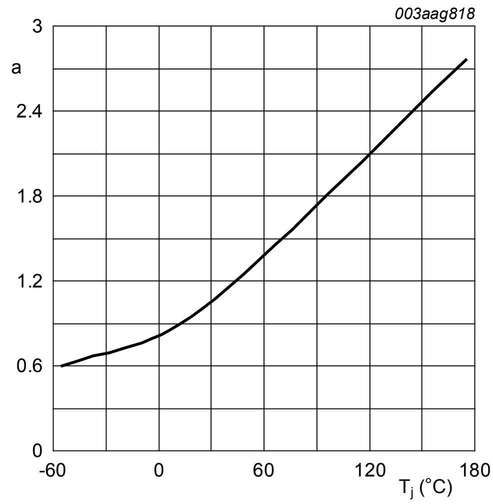


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

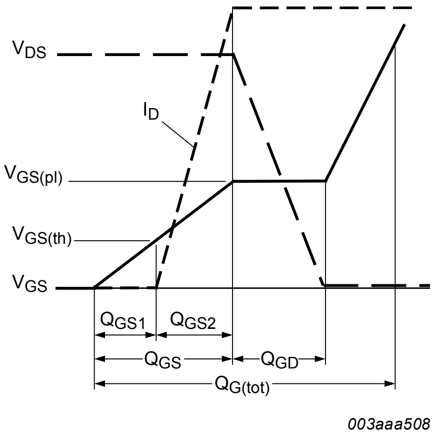


Fig. 13. Gate charge waveform definitions

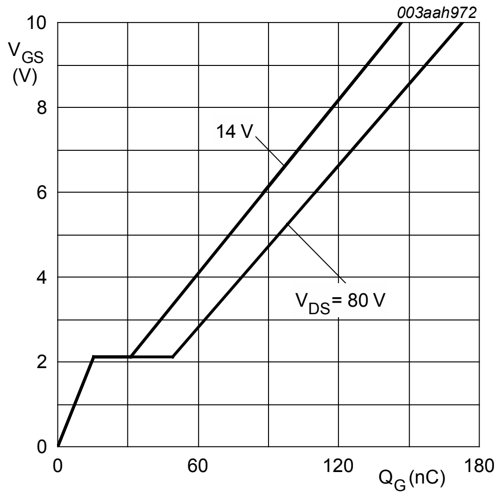


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 25A$

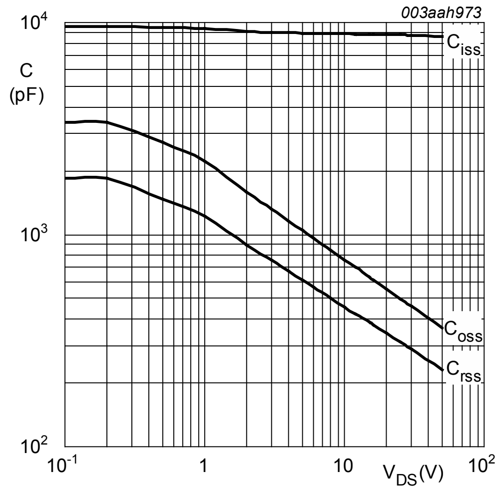


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

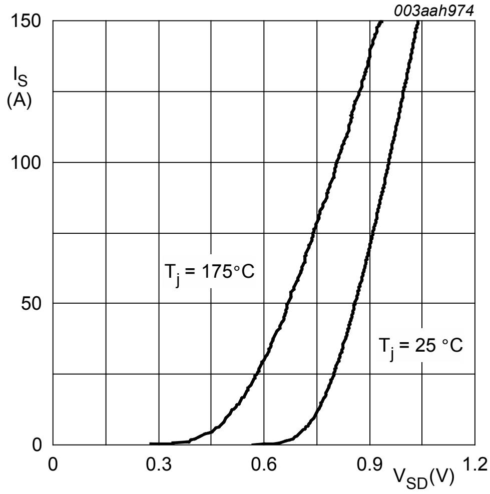
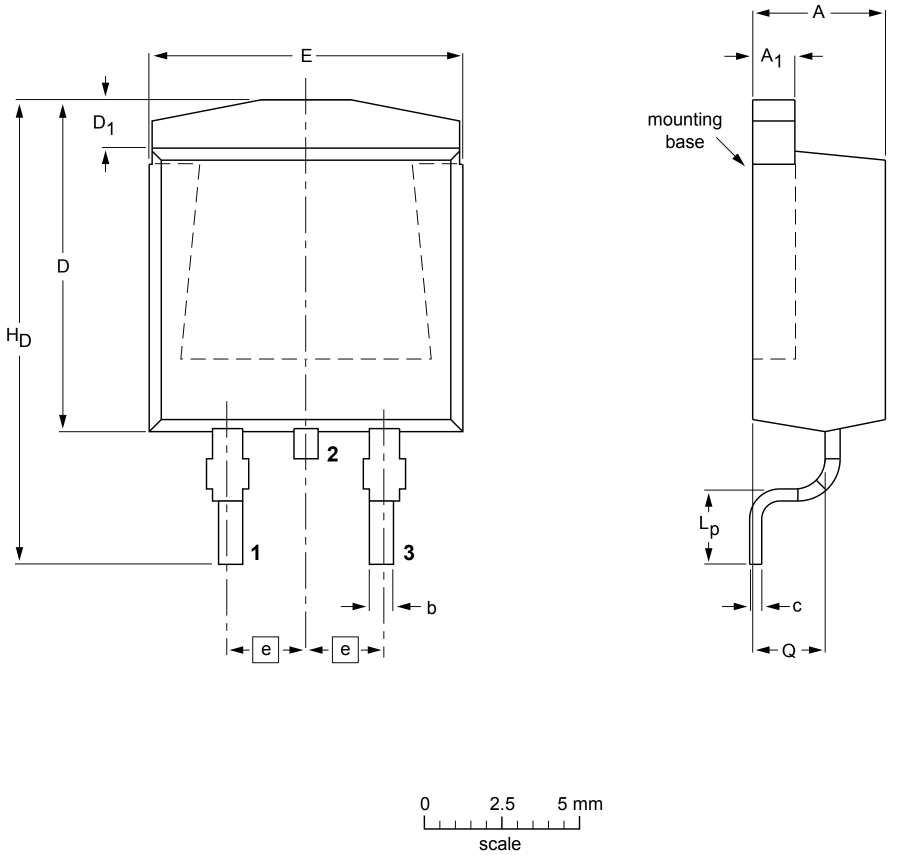


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig. 17. Package outline D2PAK (SOT404)

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9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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