C8051F326-GDI

Full-Speed USB, 16 kB Flash MCU Family

USB Function Controller
- USB specification 2.0 compliant
- Full speed (12 Mbps) or low speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for full speed or low speed
- Supports three fixed-function endpoints
- 256 Byte USB buffer memory
- Integrated transceiver; no external resistors required

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Voltage Supply Input: 2.7 to 5.25 V
- Voltages from 3.6 to 5.25 V supported using On-Chip Voltage Regulator

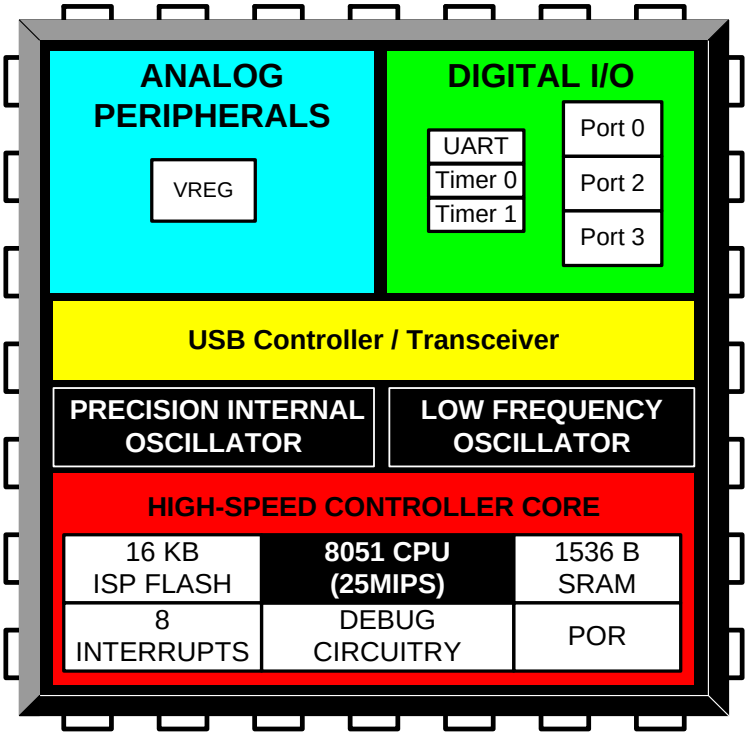
High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory
- 1536 bytes internal RAM (1 k + 256 + 256 USB FIFO)
- 16k bytes Flash; In-system programmable in 512-byte sectors

Digital Peripherals
- 15 Port I/O; All 5 V tolerant with high sink current
- Enhanced UART
- Two general purpose 16-bit timers

Clock Sources
- Internal oscillator: 0.25% accuracy with clock recovery enabled. Supports all USB and UART modes
- External CMOS clock
- Can switch between clock sources on-the-fly; useful in power saving strategies

Full Technical Data Sheet
- C8051F326/7



1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)*	RAM (Bytes)	Calibrated Internal Oscillator	USB	Supply Voltage Regulator	UART	Timers (16-bit)	Digital Port I/Os	Separate I/O Supply	Lead-free (RoHS Compliant)	Package
C8051F326-GDI	25	16	1536	✓	✓	✓	✓	2	15	✓	✓	Tested Die in Wafer Form
***Note:** 512 bytes reserved for factory use.												

2. Pin Definitions

Table 2.1. Pin Definitions for the C8051F326-GDI

Name	Physical Pad Number	Type	Description
VDD	7	Power In Power Out	2.7–3.6 V Core Supply Voltage Input. 3.3 V Voltage Regulator Output.
VIO	6	Power In	V I/O Supply Voltage Input. The voltage at this pin must be less than or equal to the Core Supply Voltage (V_{DD}) for the 'F326.
GND	2, 3		Ground.
$\overline{\text{RST}}$/ C2CK	11	D I/O D I/O	Device Reset. Open-drain output of internal POR or VDD monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. Clock signal for the C2 Debug Interface.
P3.0/ C2D	12	D I/O D I/O	Port 3.0. Bi-directional data signal for the C2 Debug Interface.
REGIN	8, 9	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	10	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
D+	4	D I/O	USB D+.
D–	5	D I/O	USB D–.
P0.0	1	D I/O	Port 0.0.
P0.1	30	D I/O	Port 0.1.
P0.2	29	D I/O	Port 0.2.
P0.3/ XTAL2	28	D I/O D In	Port 0.3. External Clock Input.
P0.4	27	D I/O	Port 0.4.
P0.5	26	D I/O	Port 0.5.
P0.6	25	D I/O	Port 0.6.

Table 2.1. Pin Definitions for the C8051F326-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.7	24	D I/O	Port 0.7.
P2.0	23	D I/O	Port 2.0.
P2.1	22	D I/O	Port 2.1.
P2.2	16	D I/O	Port 2.2.
P2.3	15	D I/O	Port 2.3.
P2.4	20	D I/O	Port 2.4.
P2.5	17	D I/O	Port 2.5.

3. Bonding Instructions

Table 3.1. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (28-QFN)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
1	1	P0.0	–1071.425	892.6
2	2	GND	–1071.425	761.6
3	2	GND	–1071.425	669.6
4	3	D+	–1071.425	461.22
5	4	D–	–1071.425	132.57
6	5	VIO	–1071.425	–66.2
7	6	VDD	–1071.425	–191.28
8	7	REGIN	–1071.425	–836.2
9	7	REGIN	–1071.425	–928.6
10	8	VBUS	–904.425	–1079.6
11	9	/RST/C2CK	–696.825	–1079.6
12	10	P3.0/C2D	–516.825	–1079.6
13	—	Reserved	–385.825	–1079.6
14	—	Reserved	–310.825	–1079.6
15	11	P2.3	–179.825	–1079.6
16	12	P2.2	0.175	–1079.6
17	16	P2.5	1071.425	–877.6
18	—	Reserved	1071.425	–741.6
19	—	Reserved	1071.425	–666.6
20	17	P2.4	1071.425	–530.6
21	—	Reserved	1071.425	–391.8
22	18	P2.1	1071.425	–40.95
23	19	P2.0	1071.425	139.05
24	22	P0.7	884.425	1079.6
25	23	P0.6	714.425	1079.6
26	24	P0.5	534.425	1079.6
27	25	P0.4	–364.425	1079.6
28	26	P0.3	–534.425	1079.6
29	27	P0.2	–714.425	1079.6
30	28	P0.1	–884.425	1079.6

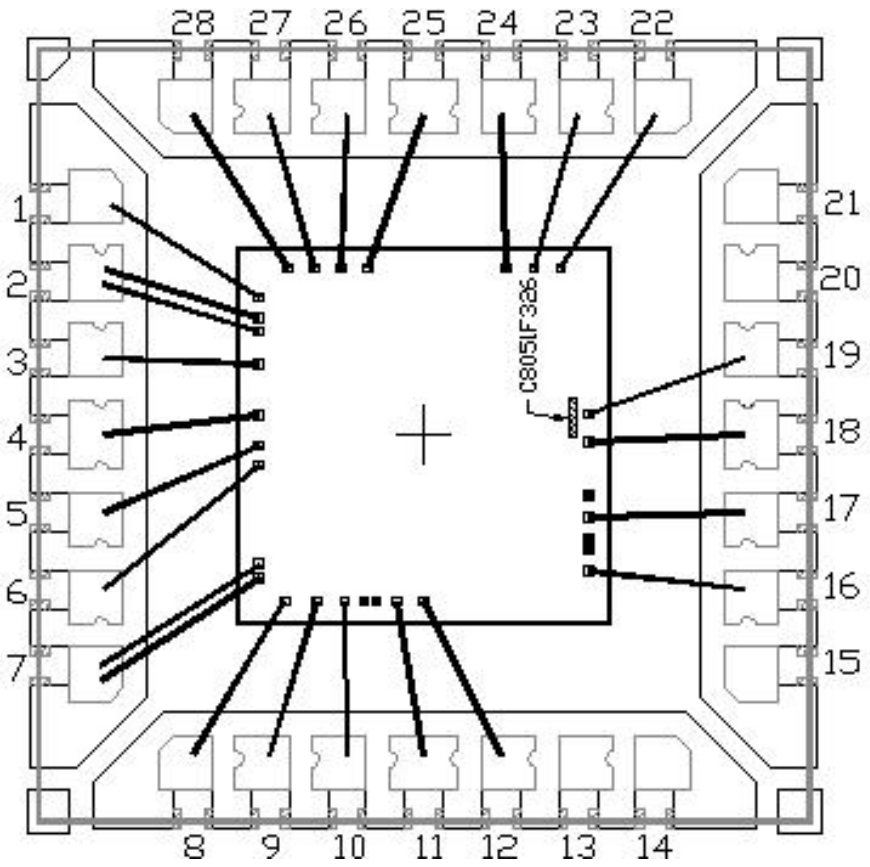


Figure 3.1. Die Bonding (QFP-28)

Table 3.2. Wafer and Die Information

Wafer ID	C8051F326
Wafer Dimensions	8 in
Die Dimensions	2.43 mm x 2.45 mm
Wafer Thickness	12 mil ±1 mil
Wafer Identification	Notch
Scribe Line Width	80 µm
Die Per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 µm
***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

NOTES:

CONTACT INFORMATION

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