C8051F331

25 MIPS, 8 kB Flash, 20-Pin Mixed-Signal MCU

Analog Peripherals

Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4 µA)

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Supply Voltage: 2.7 to 3.6 V

- Typical operating current: 6.4 mA at 25 MHz
  9 µA at 32 kHz
- Typical stop mode current: <0.1 µA

Temperature Range: –40 to +85 °C

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

Clock Sources

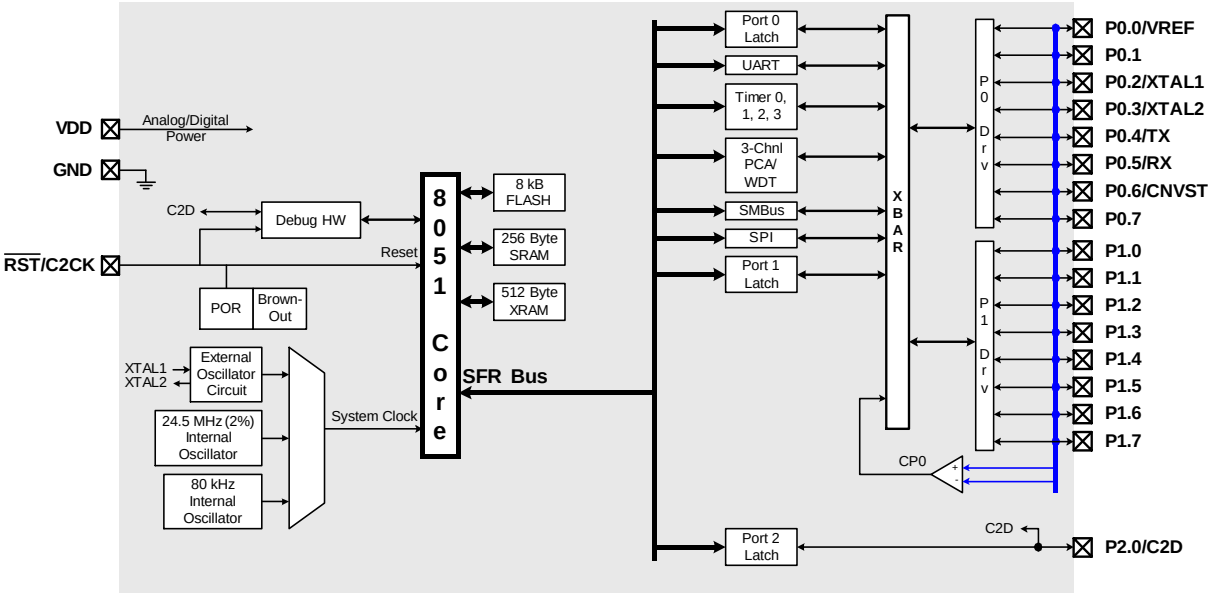
- Two internal oscillators:
  - 25 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

Package

- 20-pin QFN

Ordering Part Numbers

- Lead-free package: C8051F331-GM



Selected Electrical Specifications

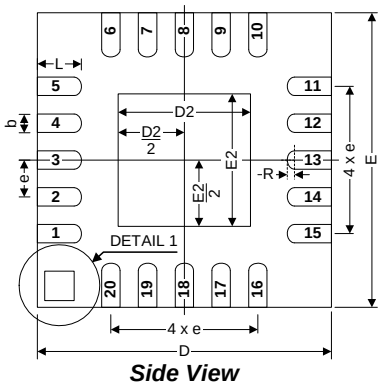
(T_A = –40 to +85 C°, VDD = 2.7 V unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL CHARACTERISTICS					
Supply Voltage		2.7		3.6	V
Supply Current with CPU active	Clock = 25 MHz Clock = 1 MHz Clock = 80 kHz; V_{DD} Monitor Disabled Clock = 32 kHz; V_{DD} Monitor Disabled		6.4 0.36 20 9		mA mA µA µA
Supply Current (shutdown)	Oscillator off; V_{DD} Monitor Disabled		<0.1		µA
Clock Frequency Range		DC		25	MHz
INTERNAL OSCILLATORS					
Frequency (OSC0)		24.0	24.5	25.0	MHz
Frequency (OSC1)	Note 1		80		kHz
COMPARATOR					
Response Time Mode0	(CP+) – (CP-) = 100 mV		0.1		µs
Current Consumption Mode0			7.6		µA
Response Time Mode1	(CP+) – (CP-) = 100 mV		0.18		µs
Current Consumption Mode1			3.2		µA
Response Time Mode2	(CP+) – (CP-) = 100 mV		0.32		µs
Current Consumption Mode2			1.3		µA
Response Time Mode3	(CP+) – (CP-) = 100 mV		1		µs
Current Consumption Mode3			0.4		µA

Note 1: OSC1 can be calibrated in 2.5% steps using an internal calibration register.

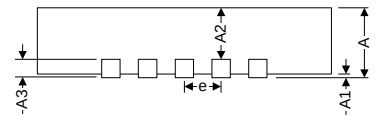
Package Information

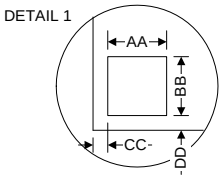
Bottom View



	MM		
	MIN	TYP	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D		4.00	
D2	2.00	2.15	2.35
E		4.00	
E2	2.00	2.15	2.35
e		0.5	
L	0.45	0.55	0.65
N		20	
ND		5	
NE		5	
R	0.09		
AA		0.435	
BB		0.435	
CC		0.18	
DD		0.18	

Side View





C8051F330DK Development Kit