C8051F912-GDI

Tested Single/Dual Battery, 0.9–3.6 V, 16 kB Flash, SmaRTClock, 12/10-Bit ADC MCU Die in Wafer Form

Ultra-Low Power
- 160 µA/MHz in active mode (24.5 MHz clock)
- 2 µs wake-up time (two-cell mode)
- 10 nA sleep mode with memory retention
- 50 nA sleep mode with brownout detector
- 300 nA sleep mode with LFO
- 600 nA sleep mode with external crystal

Supply Voltage 0.9 to 3.6 V
- One-cell mode supports 0.9 to 3.6 V operation
- Two-cell mode supports 1.8 to 3.6 V operation
- Built-in dc-dc converter with 1.8 to 3.3 V output for use in one-cell mode
- Built-in LDO regulator allows a high analog supply voltage and low digital core voltage
- 2 built-in supply monitors (brownout detectors)

12 or 10-Bit Analog-to-Digital Converter
- ±1 LSB INL no missing codes (10-bit mode)
- Programmable throughput up to 300 ksps (10-bit mode)
- 12-bit extended resolution mode provides ±1.5 LSB INL at up to 75 ksps throughput
- 15 external inputs
- On-chip voltage reference
- On-chip PGA allows measuring voltages up to twice the reference voltage
- 16-bit auto-averaging accumulator with burst mode provides increased ADC resolution
- Data dependent windowed interrupt generator
- Built-in temperature sensor

Two Comparators
- Programmable hysteresis and response time
- Configurable as wake-up or reset source

6-Bit Programmable Current Reference
- Up to ± 500 µA. Can be used as a bias or for generating a custom reference voltage
- PWM Enhanced Mode provides additional resolution

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory
- 768 bytes RAM
- 16 kB Flash; In-system programmable

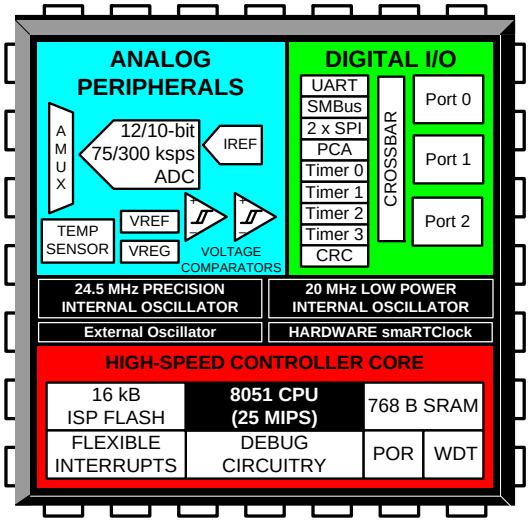
Digital Peripherals
- 16 port I/O; All 5 V tolerant with high sink current and programmable drive strength
- Hardware SMBus™ (I²C™ Compatible), 2 x SPI™, and UART serial ports available concurrently
- Four general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with six capture/compare modules and watchdog timer

Clock Sources
- Internal oscillators: 24.5 MHz, 2% accuracy supports UART operation; 20 MHz low power oscillator requires very little bias current
- External oscillator: Crystal, RC, C, or CMOS Clock
- SmaRTClock oscillator: 32 kHz crystal or internal LFO
- Can switch between clock sources on-the-fly; useful in implementing various power saving modes

On-Chip Debug
- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (no emulator required)
- Provides 4 breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

Temperature range: –40 to +85° C

Full Technical Data Sheet
- C8051F91x-C8051F90x



1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)*	RAM (Bytes)	SmaRTClock Real Time Clock	SMBus/I^2C	UART	Enhanced SPI	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 300ksps ADC	Programmable Current Reference	Internal Voltage Reference	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	C8051F9xx Plus Features	Package
C8051F912-GDI	25	16	768	✓	1	1	2	4	✓	16	✓	✓	✓	✓	2	✓	✓	Tested Die in Wafer Form
***Note:** 1024 bytes reserved for factory use																		

2. Pin Definitions

Table 2.1. Pin Definitions for C8051F912-GDI

Name	Physical Pad Number	Type	Description
VBAT	6	P In	Battery Supply Voltage. C8051F912 devices: Must be 0.9 to 3.6 V in single-cell battery mode and 1.8 to 3.6 V in dual-cell battery mode.
V_{DD} / DC+	4	P In P Out	Power Supply Voltage. Must be 1.8 to 3.6 V. This supply voltage is not required in low power sleep mode. This voltage must always be $\geq$ VBAT. Positive output of the dc-dc converter. In single-cell battery mode, a 1uF ceramic capacitor is required between DC+ and DC–. This pin can supply power to external devices when operating in single-cell battery mode.
DC– / GND	2	P In G	DC-DC converter return current path. In single-cell battery mode, this pin is typically not connected to ground. In dual-cell battery mode, this pin must be connected directly to ground.
GND	3	G	Required Ground.
DCEN	5	P In G	DC-DC Enable Pin. In single-cell battery mode, this pin must be connected to VBAT through a 0.68 µH inductor. In dual-cell battery mode, this pin must be connected directly to ground.
$\overline{RST}$/ C2CK	7	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. A 1 kΩ to 5 kΩ pullup to V_{DD} is recommended. Clock signal for the C2 Debug Interface.
P2.7/ C2D	8	D I/O D I/O	Port 2.7. This pin can only be used as GPIO. The Crossbar cannot route signals to this pin and it cannot be configured as an analog input. See Port I/O Section of C8051F91x-C8051F90x data sheet for a complete description. Bi-directional data signal for the C2 Debug Interface.
XTAL3	10	A In	SmaRTClock Oscillator Crystal Input.
XTAL4	9	A Out	SmaRTClock Oscillator Crystal Output.
P0.0 V_{REF}	32	D I/O or A In A In A Out	Port 0.0. External V_{REF} Input. Internal V_{REF} Output. External V_{REF} decoupling capacitors are recommended.

Table 2.1. Pin Definitions for C8051F912-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.1	31	D I/O or A In	Port 0.1.
AGND		G	Optional Analog Ground.
P0.2	30	D I/O or A In	Port 0.2. See Port I/O Section of the C8051F91x-C8051F90x data sheet for a complete description.
XTAL1		A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator. Buffered SmaRTClock oscillator output.
P0.3	29	D I/O or A In	Port 0.3.
XTAL2		A Out	External Clock Output. This pin is the excitation driver for an external crystal or resonator.
		D In	External Clock Input. This pin is the external clock input in external CMOS clock mode.
		A In	External Clock Input. This pin is the external clock input in capacitor or RC oscillator configurations.
P0.4	28	D I/O or A In	Port 0.4.
TX		D Out	UART TX Pin.
P0.5	26	D I/O or A In	Port 0.5.
RX		D In	UART RX Pin.
P0.6	25	D I/O or A In	Port 0.6.
CNVSTR		D In	External Convert Start Input for ADC0.
P0.7	24	D I/O or A In	Port 0.7.
IREF0		A Out	IREF0 Output. See IREF Section of the C8051F91x-C8051F90x data sheet for complete description.
P1.0	19	D I/O or A In	Port 1.0. May also be used as SCK for SPI1.
P1.1	18	D I/O or A In	Port 1.1. May also be used as MISO for SPI1.
P1.2	17	D I/O or A In	Port 1.2. May also be used as MOSI for SPI1.

Table 2.1. Pin Definitions for C8051F912-GDI (Continued)

Name	Physical Pad Number	Type	Description
P1.3	16	D I/O or A In	Port 1.3. May also be used as NSS for SPI1.
P1.4	13	D I/O or A In	Port 1.4.
P1.5	12	D I/O or A In	Port 1.5.
P1.6	11	D I/O or A In	Port 1.6.

3. Bonding Instructions

Table 3.1. Bond Pad Coordinates

Physical Pad Number	Example Package Pin Number (QFN-24)	Package Pin Name	Pad Coordinates Relative to Center	
			X (µm)	Y (µm)
1	Reserved*	—	–836	600
2	1	DC–/GND	–836	480
3	2	GND	–836	233
4	3	VDD/DC+	–836	78
5	4	DCEN	–836	–105
6	5	VBAT	–836	–329
7	6	$\overline{\text{RST}}$/C2CK	–836	–688
8	7	P2.7/C2D	–633	–891
9	8	XTAL4	–348	–891
10	9	XTAL3	–126	–891
11	10	P1.6	134	–891
12	11	P1.5	290	–891
13	12	P1.4	433	–891
14	Reserved*	—	577	–891
15	Reserved*	—	667	–891
16	13	P1.3	836	–688
17	14	P1.2	836	–545
18	15	P1.1	836	–389
19	16	P1.0	836	–226
20	Reserved*	—	836	–103
21	Reserved*	—	836	–13
22	Reserved*	—	836	77
23	Reserved*	—	836	167
24	17	P0.7/IREF0	836	369

***Note:** Pins marked “Reserved” should not be connected.

Table 3.1. Bond Pad Coordinates (Continued)

Physical Pad Number	Example Package Pin Number (QFN-24)	Package Pin Name	Pad Coordinates Relative to Center	
			X (µm)	Y (µm)
25	18	P0.6/CNVSTR	836	525
26	19	P0.5/RX	836	688
27	Reserved*	—	745	883
28	20	P0.4/TX	641	891
29	21	P0.3/XTAL2	484	891
30	22	P0.2/XTAL1	342	891
31	23	P0.1/AGND	–490	891
32	24	P0.0/VREF	–633	891

***Note:** Pins marked “Reserved” should not be connected.

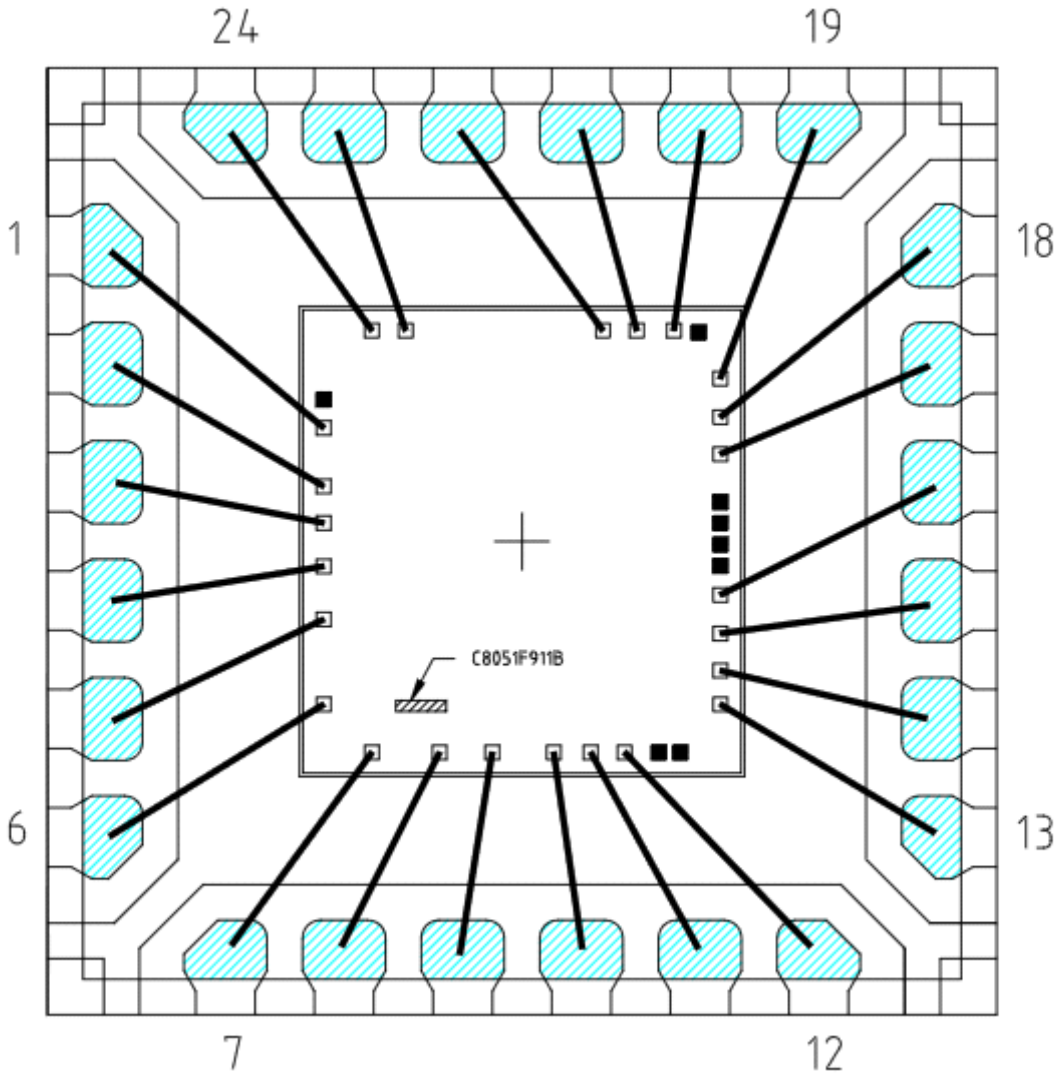


Figure 3.1. Die Bonding (QFN-24)

Table 3.2. Wafer and Die Information

Wafer ID	C8051F911B
Wafer Dimensions	8 in.
Die Dimensions	1.9256 mm x 2.0366 mm
Wafer Thickness	12 mil ±1 mil
Wafer Identification	Notch
Scribe Line Width	80 µm
Die per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	142 µm
***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 9.

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