July 31, 2012

C8051T620/1, C8051T320/1/2/3 Revision D, and C8051T626/7 Revision B Errata

Errata Status Summary

Errata #	Title	Impact	Status		Applicable Part Numbers
			Affected Revisions	Fixed Revision	
1	USB D+/D- Driver Impedance	Minor	Revision D	Not Fixed	C8051T620 C8051T621 C8051T320 C8051T321 C8051T322 C8051T323
2	GPIO Signals Driven Low After Power Cycling	Major	Revision A - D	Not Fixed	C8051T620 C8051T621 C8051T320 C8051T321 C8051T322 C8051T323
3	Clock frequency prior to entering Suspend Mode	Minor	Revision B	Not Fixed	C8051T626 C8051T627

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

1. **Description:** The output impedance of the drivers on the USB D+ and D- data lines is nominally 28 Ω but, in some cases, may be as low as 26 Ω. The minimum USB specification for full-speed devices on the D+ and D- data lines is 28 Ω.

   Impact: This may impact systems that need to be submitted for USB compliance testing. The specification for USB compliance is a system-level parameter, not a chip-level parameter. In most systems, the lower impedance of the device will not be a factor. A typical PCB will add 2-3 Ω to the effective driver impedance and bring the system level impedance within specifications.

   Workaround: For systems that require USB certification, it is recommended to add some series impedance (between 5 and 8 Ohms, ¼ watt or higher) to D+ and D- in the PCB design.

2. **Description:** The GPIO signals will be driven low for approximately 40 microseconds after power cycling the device and then return to the configured reset state.

   Impact: This may impact systems where the T62x/T32x is connected to devices that are powered from a separate supply and turned on before the T62x/T32x receives power through the 5 volt regulator or through VDD and VIO pins. The drop of the T62x/T32x signals may be seen as invalid data to the connected devices.

   Workaround: In systems that are affected by this drop, the T62x/T32x should be powered through the 5 volt regulator or through the VDD and VIO pins from the same supply used by devices that are connected to the GPIO signals of the T62x/T32x.

3. **Description:** The system clock frequency cannot be set to 48 MHz before entering Suspend Mode. Setting the system clock to high frequencies can cause improper code execution after exit from suspend on some devices.

   Impact: Devices exhibiting the issue can fail to enumerate properly over USB after exit from Suspend Mode.

   Workaround: The internal high-frequency oscillator should be set to output 1.5 MHz (OSCICN register, IFCN[1:0] = 00b) and the system clock should be set to be derived from this oscillator (CLKSEL register, CLKSL[2:0] = 000b) before entering Suspend Mode by setting the SUSPEND bit in the OSCICN register.