



74LCXH162244

LOW VOLTAGE CMOS 16-BIT BUS BUFFER (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
 $t_{PD} = 4.4 \text{ ns (MAX.) at } V_{CC} = 3V$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 12\text{mA (MIN) at } V_{CC} = 3V$
- PCI BUS LEVELS GUARANTEED AT 12 mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- 26Ω SERIE RESISTORS IN OUTPUTS
- BUS HOLD PROVIDED ON DATA INPUT
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2.0V \text{ to } 3.6V \text{ (1.5V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES H162244
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
 HBM > 2000V (MIL STD 883 method 3015);
 MM > 200V

DESCRIPTION

The 74LCXH162244 is a low voltage CMOS 16 BIT BUS BUFFER (NON-INVERTED) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

Any nG output control governs four BUS BUFFERS. Output Enable input (nG) tied together gives full 16-bit operation.

When nG is LOW, the outputs are on. When nG is HIGH, the output are in high impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

This device is designed to be used with 3 state memory address drivers, etc.

The device circuits is including 26Ω series resistance in the outputs. These resistors permit to reduce line noise in high speed applications.

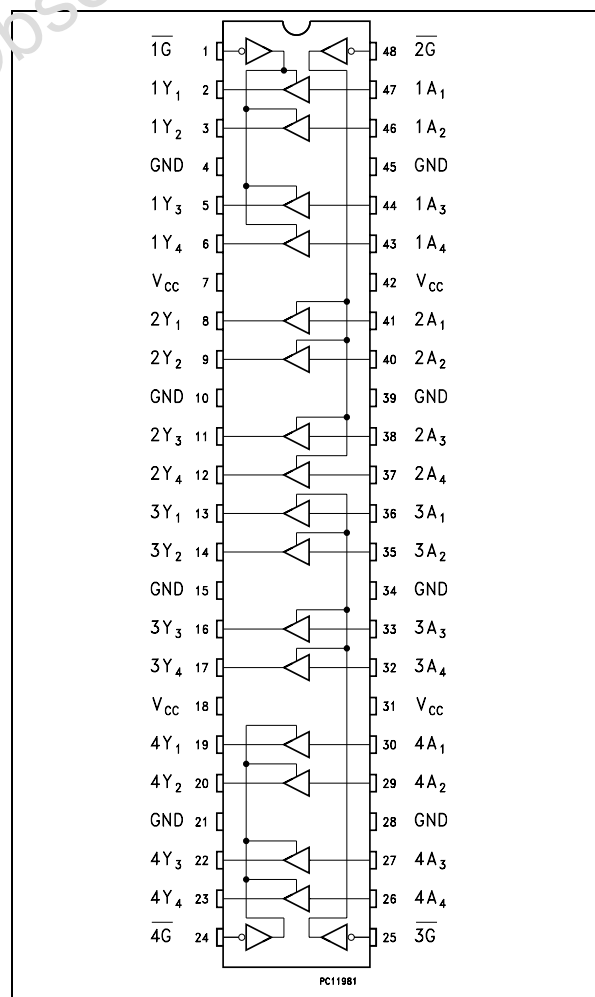
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



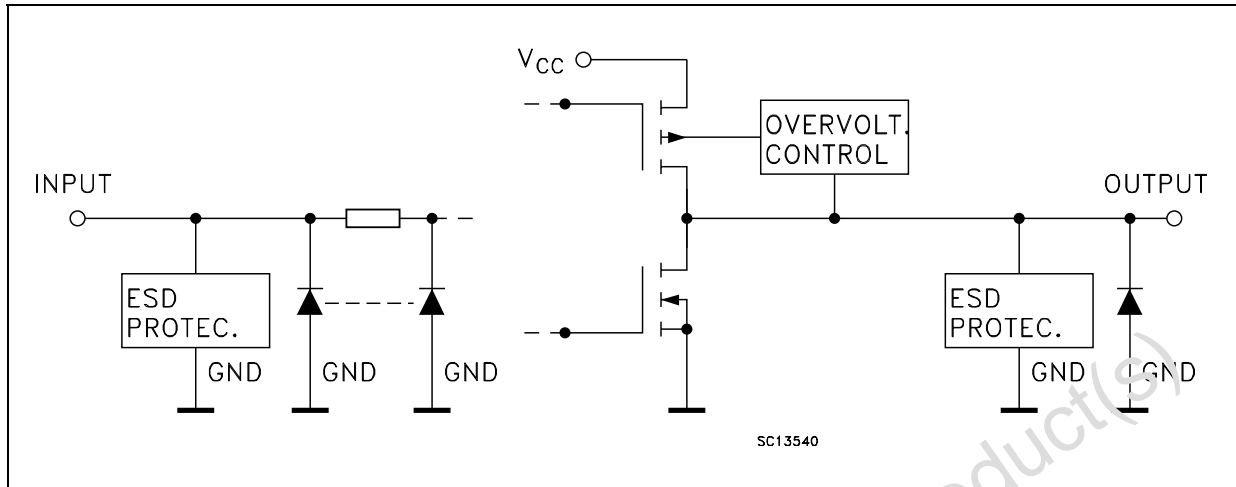
ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74LCXH162244TTR

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

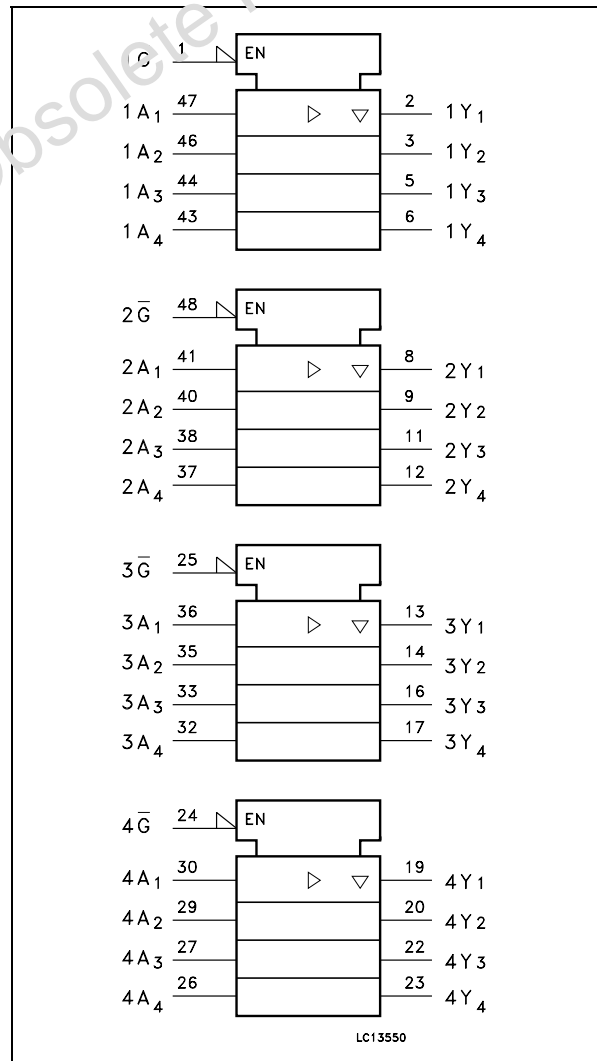
PIN No	SYMBOL	NAME AND FUNCTION
1	1G	Output Enable Input
2, 3, 5, 6	1Y1 to 1Y4	Data Outputs
8, 9, 11, 12	2Y1 to 2Y4	Data Outputs
13, 14, 16, 17	3Y1 to 3Y4	Data Outputs
19, 20, 22, 23	4Y1 to 4Y4	Data Outputs
24	4G	Output Enable Input
25	3G	Output Enable Input
30, 29, 27, 26	4A1 to 4A4	Data Outputs
36, 35, 33, 32	3A1 to 3A4	Data Outputs
41, 40, 38, 37	2A1 to 2A4	Data Outputs
47, 46, 44, 43	1A1 to 1A4	Data Outputs
48	2G	Output Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive Supply Voltage

TRUTH TABLE

INPUTS		OUTPUT
\bar{G}	A _n	Y _n
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (OFF State)	-0.5 to +7.0	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (10 sec)	300	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

- 1) I_O absolute maximum rating must be observed
 2) $V_O < \text{GND}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (OFF State)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 3.0$ to 3.6V)	± 12	mA
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 2.7\text{V}$)	± 8	mA
T_{op}	Operating Temperature	-55 to 125	$^{\circ}\text{C}$
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

- 1) Truth Table guaranteed: 1.5V to 3.6V
 2) V_{IN} from 0.8V to 2V at $V_{CC} = 3.0\text{V}$

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value				Unit
		V _{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
V _{IL}	Low Level Input Voltage					0.8		0.8
V _{OH}	High Level Output Voltage	2.7 to 3.6	I _O =-100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		2.7	I _O =-8 mA	2.0		2.0		
		3.0	I _O =-6 mA	2.4		2.4		
V _{OL}	Low Level Output Voltage	2.7 to 3.6	I _O =100 μA		0.2		0.2	V
		2.7	I _O =8 mA		0.6		0.6	
		3.0	I _O =6 mA		0.55		0.55	
			I _O =12 mA		0.5		0.8	
I _I	Input Leakage Current	2.7 to 3.6	V _I = 0 to 5.5V		± 5		± 5	μA
I _{I(HOLD)}	Input Hold Current	3.0	V _I = 0.8V	75		75		μA
			V _I = 2.0V	-75		-75		
		3.6	V _I = 0 to 3.6V		± 500		± 500	
I _{off}	Power Off Leakage Current	0	V _I or V _O = 5.5V		10		10	μA
I _{oz}	High Impedance Output Leakage Current	2.7 to 3.6	V _I = V _{IH} or V _{IL} V _O = 0 to V _{CC}		± 5		± 5	μA
I _{CC}	Quiescent Supply Current	2.7 to 3.6	V _I = V _{CC} or GND		20		20	μA
			V _I or V _O = 3.6 to 5.5V		± 20		± 20	
ΔI _{CC}	I _{CC} incr. per input	2.7 to 3.6	V _{IH} = V _{CC} - 0.6V		500		500	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
V _{OLP}	Dynamic Low Level Quiet Output (note 1)	3.3	C _L = 50pF V _{IL} = 0V, V _{IH} = 3.3V		0.8		V
V _{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition				Value				Unit
		V _{CC} (V)	C _L (pF)	R _L (Ω)	t _s = t _r (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	2.7	50	500	2.5	1.5	5.6	1.5	6.5	ns
		3.0 to 3.6				1.5	4.4	1.5	5.1	
t _{PZL} t _{PZH}	Output Enable Time	2.7	50	500	2.5	1.5	6.3	1.5	7.2	ns
		3.0 to 3.6				1.5	5.9	1.5	6.8	
t _{PLZ} t _{PHZ}	Output Disable Time	2.7	50	500	2.5	1.5	6.3	1.5	7.2	ns
		3.0 to 3.6				1.5	5.9	1.5	6.8	
t _{OSLH} t _{OSHL}	Output To Output Skew Time (note1, 2)	3.0 to 3.6	50	500	2.5		1.0		1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|)

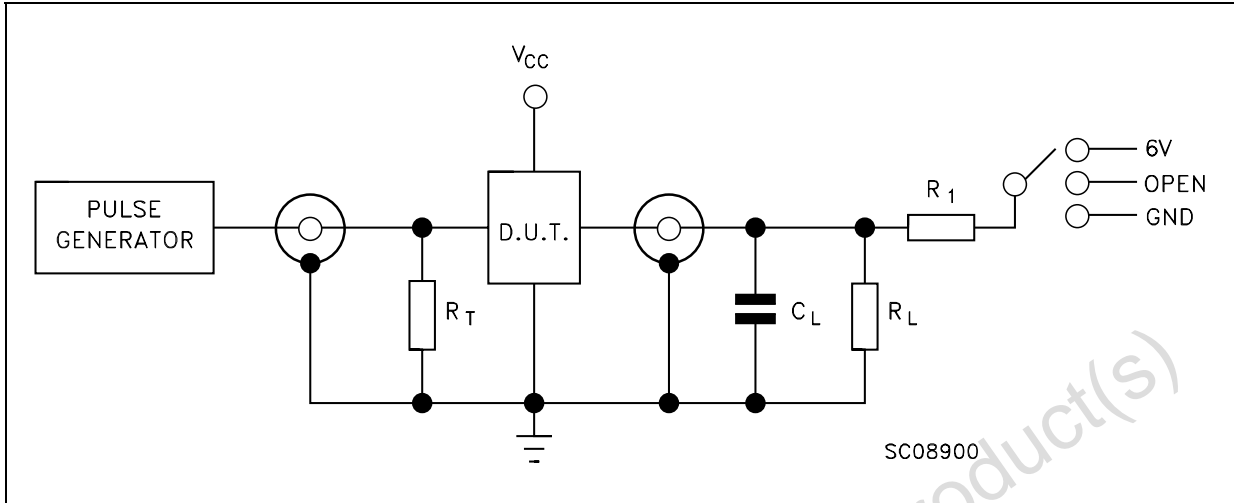
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance				4		pF
C _{OUT}	Output Capacitance				10		pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10MHz V _{IN} = 0 or V _{CC}		50		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(oper)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/16 (per circuit)

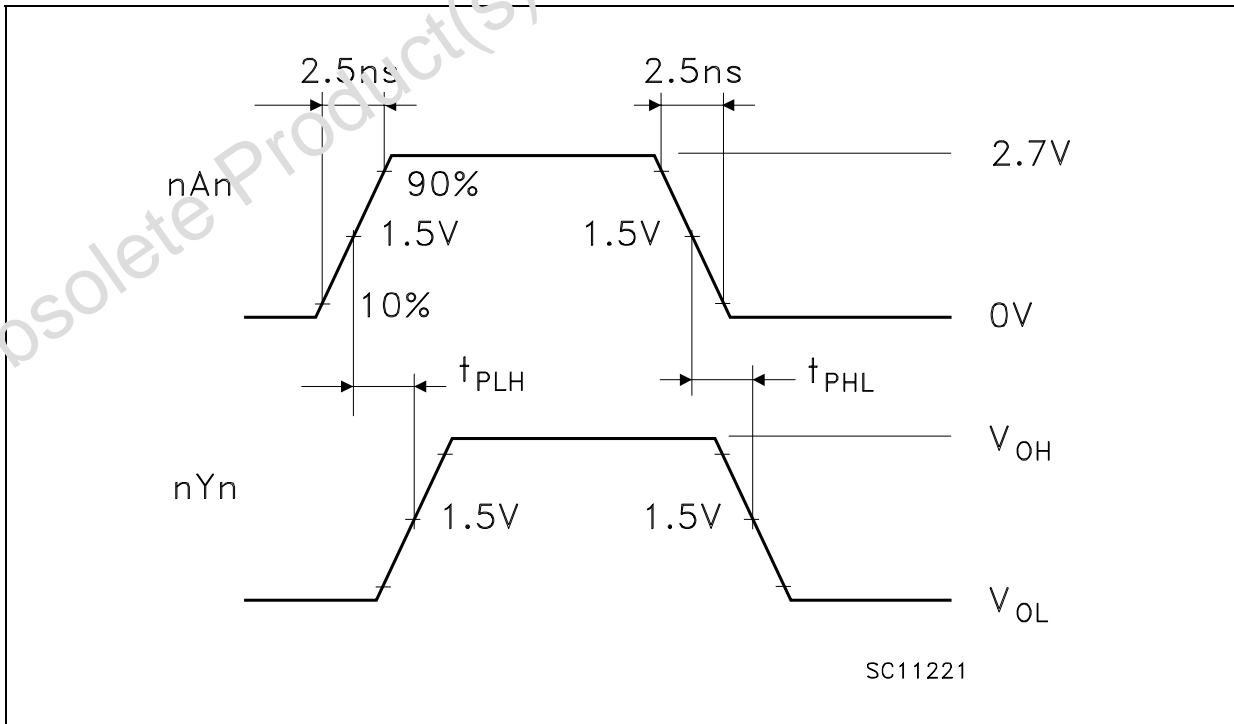
TEST CIRCUIT



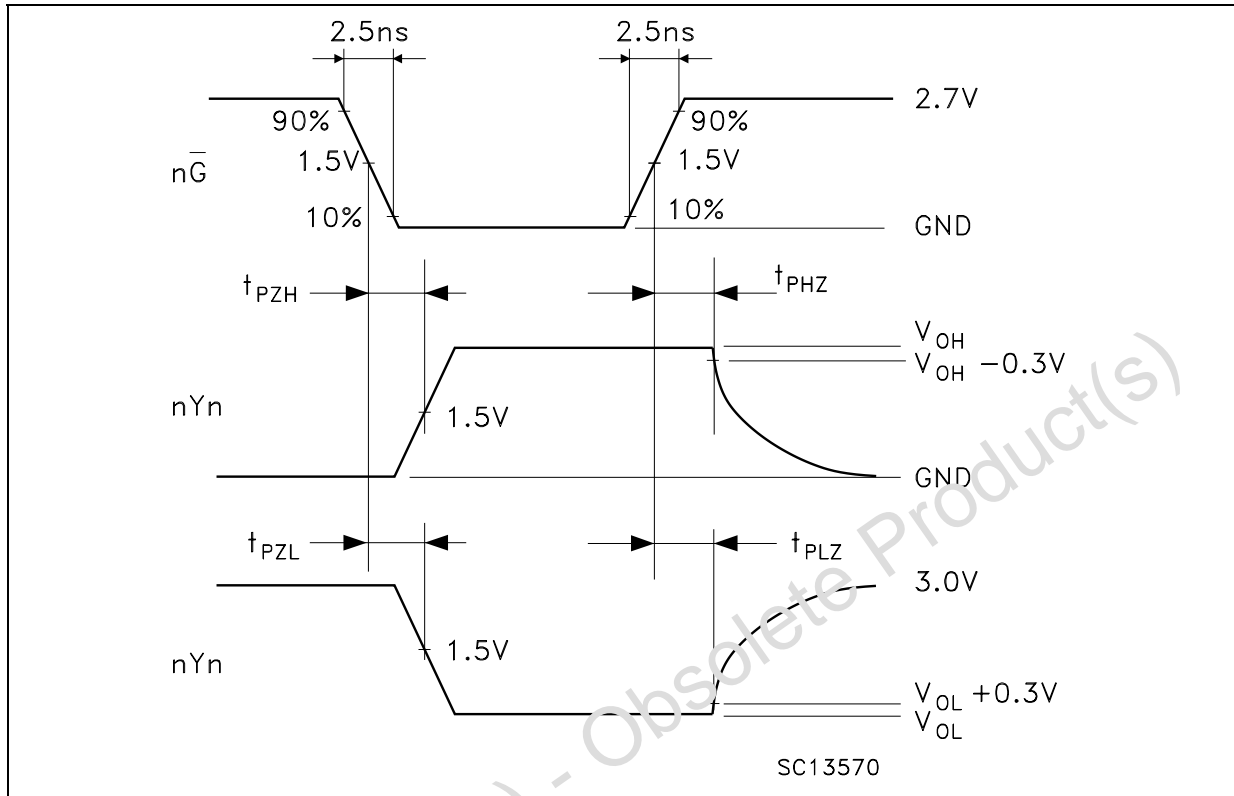
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
t_{PZH} , t_{PHZ}	GND

C_L = 50 pF or equivalent (includes jig and probe capacitance)
 R_L = R_1 = 500 Ω or equivalent
 R_T = Z_{OUT} of pulse generator (typically 50 Ω)

WAVEFORM 1 : PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

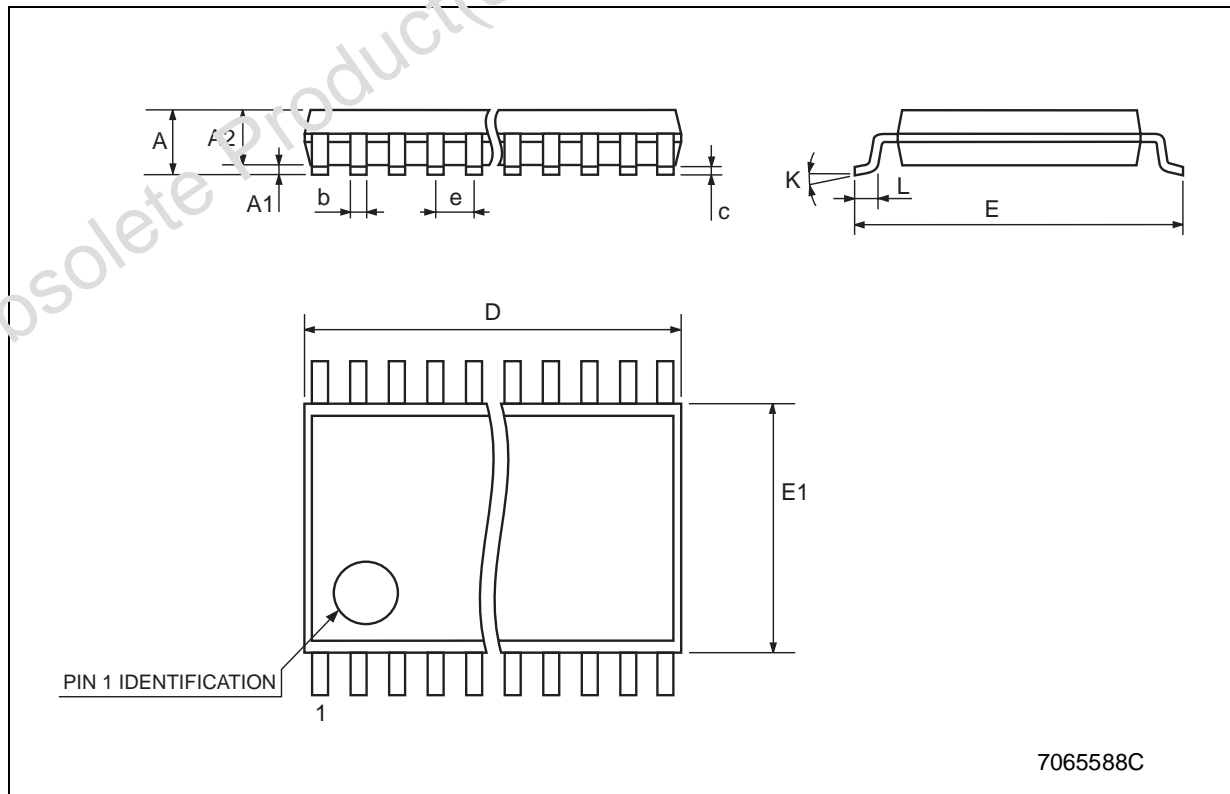


WAVEFORM 2 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



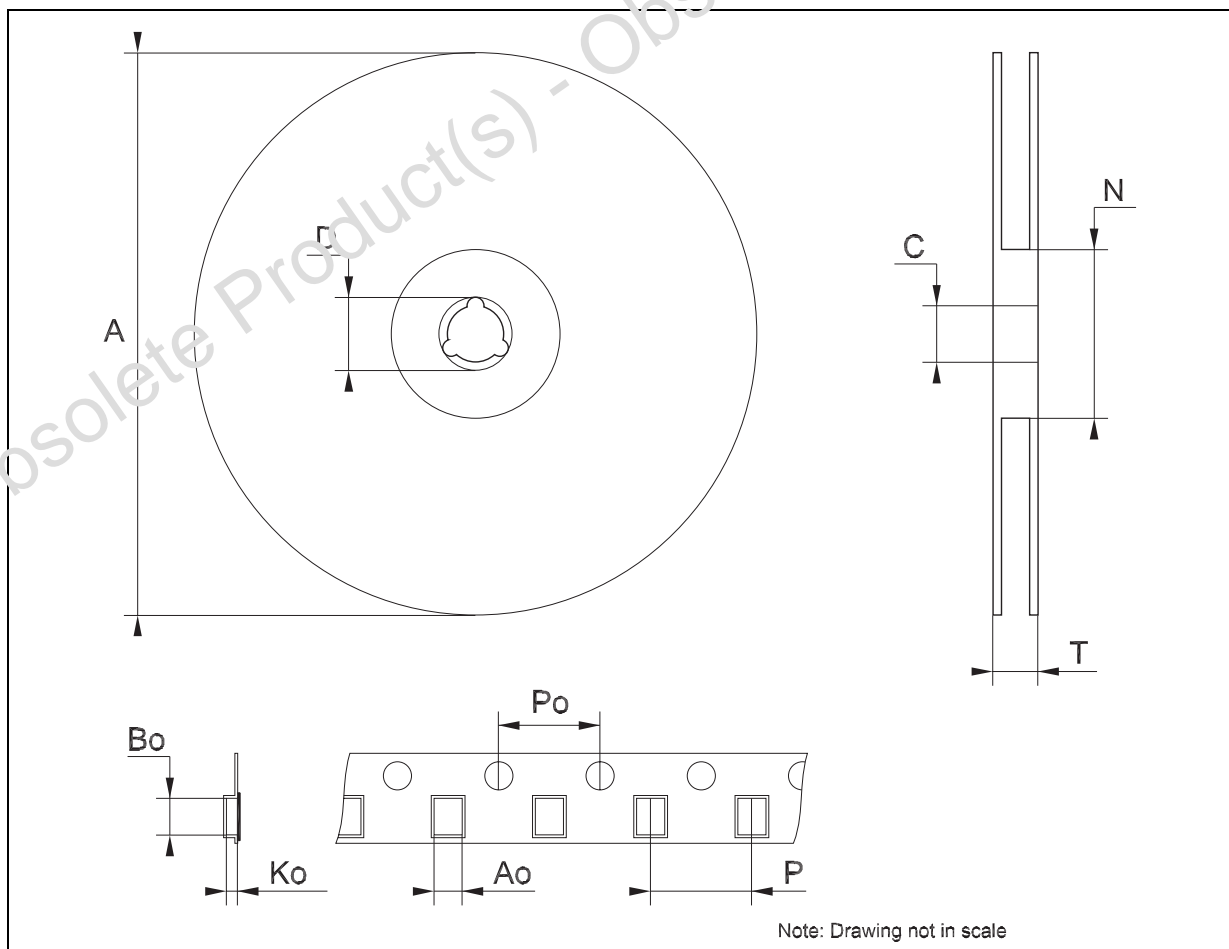
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>