

Low power voltage regulator

Features

- Operating DC supply voltage range 5.6V to 31V
- Very low quiescent current with watchdog disabled
- Precision output voltage (3%)
- Low drop voltage (180mV typ at $I_o=150\text{mA}$)
- Reset circuit sensing the output voltage down to 1V
- Programmable reset delay with external capacitor
- Watchdog disable input
- Programmable watchdog timer with external capacitor
- Thermal shutdown and short circuit protection
- Wide temperature range ($T_j = -40^\circ\text{C}$ to 150°C)

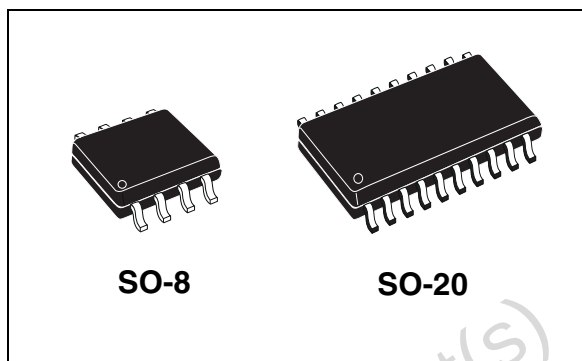


Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
SO-8	L4989D	L4989D013TR
SO-20	L4989MD	L4989MD013TR

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1 Block diagram and pin configuration

Figure 1. Block diagram

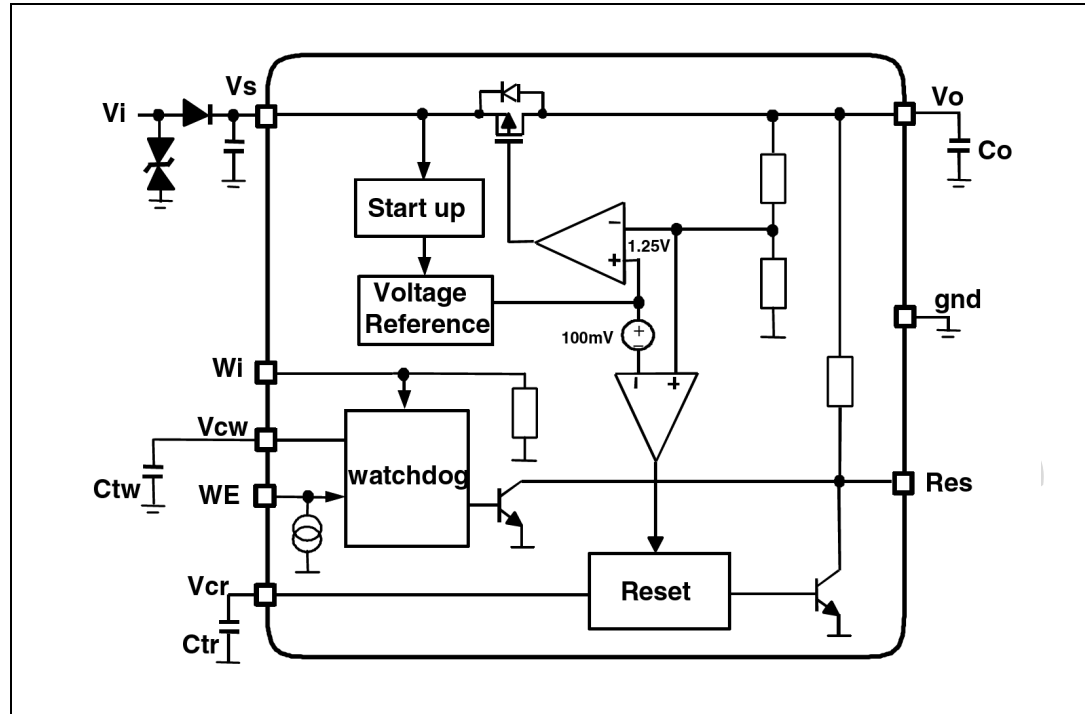
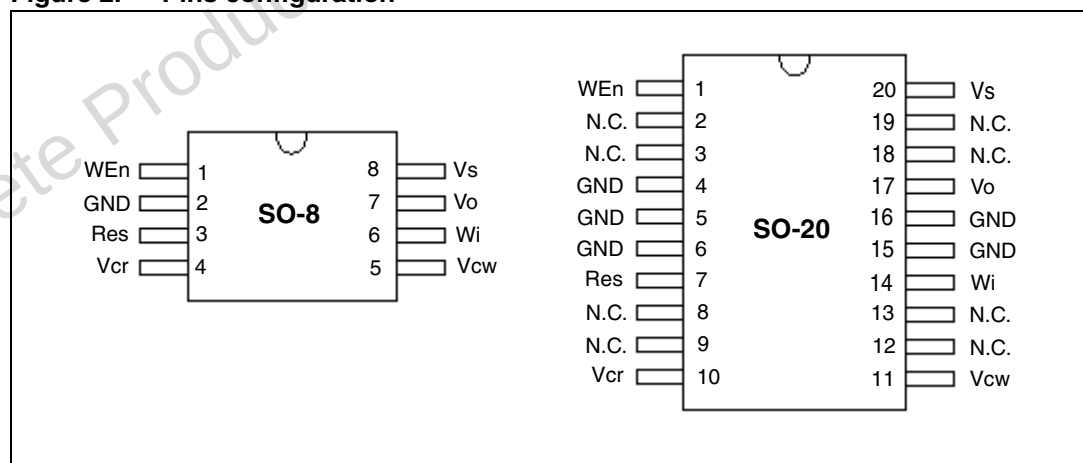


Table 2. Pins description

Pin name	SO-8(D)	SO-20(MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground. Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
Vo	7	17	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
Vs	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2. Pins configuration

2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{VSDC}	DC supply voltage	-0.3 to 40	V
I_{VSDC}	Input current	Internally limited	
V_{Vo}	DC output voltage	-0.3 to 6	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{od}	Open Drain output voltage	-0.3 to $V_{Vo} + 0.3$	V
I_{od}	Open Drain output current	Internally limited	
V_{cr}	Reset delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{cw}	Watchdog delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{WE_n}	Watchdog Enable input voltage	-0.3 to 40	V
T_j	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	S0-8	S0-12+4+4	Unit
$R_{th-jamb}$	Thermal resistance junction to ambient	130 to 180	50 ⁽¹⁾	°C/W

1. With 6 sq. cm on board heat sink.

2.3 Electrical characteristics

$V_s = 5.6V$ to $31V$, $T_j = -40^\circ C$ to $+150^\circ C$ unless otherwise specified.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vo	V_{o_ref}	Output voltage	$V_s = 5.6$ to $31V$ $I_o = 1$ to 150 mA	4.85	5.0	5.15	V
Vo	I_{short_13}	Short circuit current	$V_s = 13.5V^{(1)}$	160	210	250	mA
Vo	I_{lim}	Output current limitation	$V_s = 13.5V^{(1)}$	170	250	290	mA
V_s, V_o	V_{line}	Line regulation voltage	$V_s = 5.6$ to $31V$ $I_o = 1$ to $150mA$			25	mV
Vo	V_{load}	Load regulation voltage	$I_o = 1$ to $150mA$			25	mV
V_s, V_o	V_{dp}	Drop voltage	$I_o = 150mA$		180	400	mV
V_s, V_o	SVR	Ripple rejection	$f_r = 100$ Hz	55			dB
V_s, V_o	I_{qs_1}	Current consumption with watchdog not active $I_{qs_1} = I_{VS} - I_O$	$V_s = 13.5V, I_o < 1mA,$ $WEn = low$		69	115	μA
V_s, V_o	I_{qs_10}	Current consumption with watchdog not active $I_{qs_10} = I_{VS} - I_O$	$V_s = 13.5V,$ $I_o = 10mA,$ $WEn = low$		127	300	μA
V_s, V_o	I_{qs_50}	Current consumption with watchdog not active $I_{qs_50} = I_{VS} - I_O$	$V_s = 13.5V,$ $I_o = 50mA,$ $WEn = low$		498	900	μA
V_s, V_o	I_{qs_150}	Current consumption with watchdog not active $I_{qs_150} = I_{VS} - I_O$	$V_s = 13.5V,$ $I_o = 150mA,$ $WEn = low$		1.40	2	mA
V_s, V_o	I_{qn_1}	Current consumption with watchdog active $I_{qn_1} = I_{VS} - I_O$	$V_s = 13.5V, I_o < 1mA,$ $WEn = high$		110	170	μA
V_s, V_o	I_{qn_10}	Current consumption with watchdog active $I_{qn_10} = I_{VS} - I_O$	$V_s = 13.5V,$ $I_o = 10mA,$ $WEn = high$		168	350	μA
V_s, V_o	I_{qn_50}	Current consumption with watchdog active $I_{qn_50} = I_{VS} - I_O$	$V_s = 13.5V,$ $I_o = 50mA,$ $WEn = high$		538	1000	μA
V_s, V_o	I_{qn_150}	Current consumption with watchdog active $I_{qn_150} = I_{VS} - I_O$	$V_s = 13.5V,$ $I_o = 150mA,$ $WEn = high$		1.45	2	mA
	T_w	Thermal protection temperature		150		190	$^\circ C$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^\circ C$

1. See [Figure 3](#).

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	$R_{ext} = 5k\Omega$ to V_o , $V_o > 1V$			0.4	V
Res	I_{Res_lkg}	Reset output high leakage current	$V_{Res} = 5V$			1	μA
Res	R_{Res}	Pull up internal resistance	Versus V_o	10	20	40	$k\Omega$
Res	V_{o_th}	Reset threshold voltage	$V_s = 5.6$ to $31V$, $I_o = 1$ to $150mA$	6%	8%	10%	Below V_{o_ref}
Vcr	Vrlth	Reset timing low threshold	$V_s = 13.5V$	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset timing high threshold	$V_s = 13.5V$	44%	47%	50%	V_{o_ref}
Vcr	Icr	Charge current	$V_s = 13.5V$	8	15	30	μA
Vcr	Idr	Discharge current	$V_s = 13.5V$	8	15	30	μA
Res	Trr_2	Reset reaction time ⁽¹⁾	$V_o = V_{o_th} - 100mV$	100	250	700	μs
Res	Trd	Reset delay time	$V_s = 13.5V$, $C_{tr} = 1nF$	65	115	165	ms

1. When V_o becomes lower than 4V, the reset reaction time decreases down to 2 μs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	Vih	Input high voltage	$V_s = 13.5V$	3.5			V
Wi	Vil	Input low voltage	$V_s = 13.5V$			1.5	V
Wi	Vih	Input hysteresis	$V_s = 13.5V$		500		mV
Wi	Rwi	Pull down resistor	$V_s = 13.5V$	30	100	250	$K\Omega$
Vcw	Vwhth	High threshold	$V_s = 13.5V$	44%	47%	50%	V_{o_ref}
Vcw	Vwlth	Low threshold	$V_s = 13.5V$	10%	13%	16%	V_{o_ref}
Vcw	Icwc	Charge current	$V_s = 13.5V$, $V_{cw} = 0.1V$	5	10	20	μA
Vcw	Icwd	Discharge current	$V_s = 13.5V$, $V_{cw} = 2.5V$	1.25	2.5	5	μA
Vcw	Twop	Watchdog period	$V_s = 13.5V$, $C_{tw} = 47nF$	20	40	80	ms
Res	twol	Watchdog output low time	$V_s = 13.5V$, $C_{tw} = 47nF$	4	8	16	ms

Table 8. Watchdog Enable

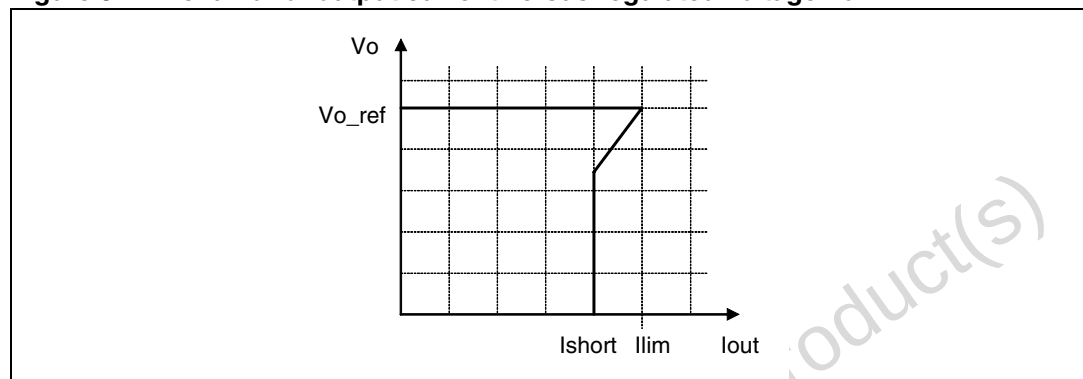
Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WEn	V _{WEn_l}	Enable input low voltage				1	V
WEn	V _{WEn_h}	Enable input high voltage		3			V
WEn	V _{WEn_hy}	Enable input hysteresis		600	920	1300	mV
WEn	I _{leak}	Pull down current	V _s = 13.5V	1	2.5	5	μA

3 Application information

3.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a very low dropout voltage at current up to 150mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. The voltage Regulator is always active and not depending on the state of WEn input pin. A short circuit protection to GND is provided.

Figure 3. Behavior of output current versus regulated voltage Vo



3.2 Reset

The reset circuit supervises the output voltage V_o . The V_{o_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{o_th} then Res goes low with a reaction time t_{rr} . The reset low signal is guaranteed for an output voltage V_o greater than 1V.

When the output voltage becomes higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$T_{osc} = [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{dr}$$

where:

I_{cr} : is an internally generated charge current

I_{dr} : is an internally generated discharge current

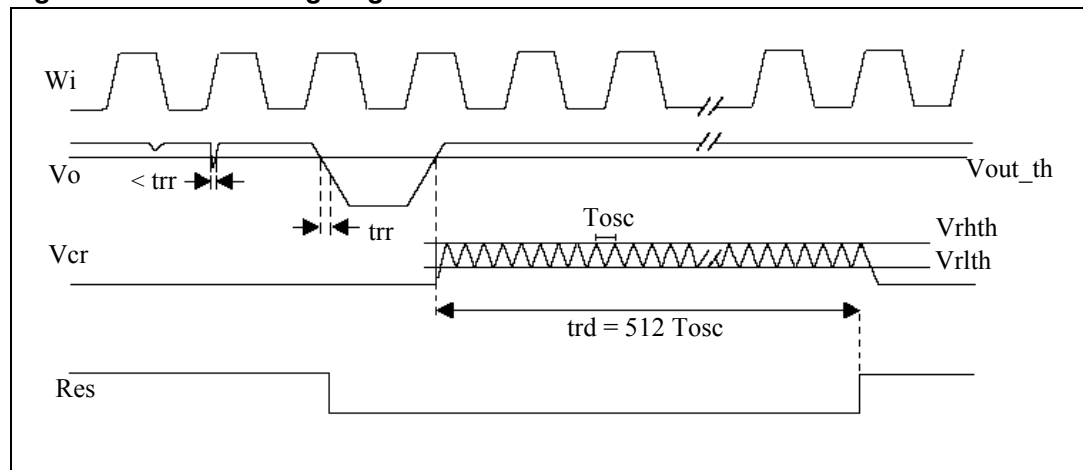
V_{rhth} , V_{rlth} : are two voltages defined with the output voltage and a resistor output divider

C_{tr} : is an external capacitance.

t_{rd} is given by:

$$t_{rd} = 512 \times T_{osc}$$

The Reset is always active and not depending on the state of WEn input pin.

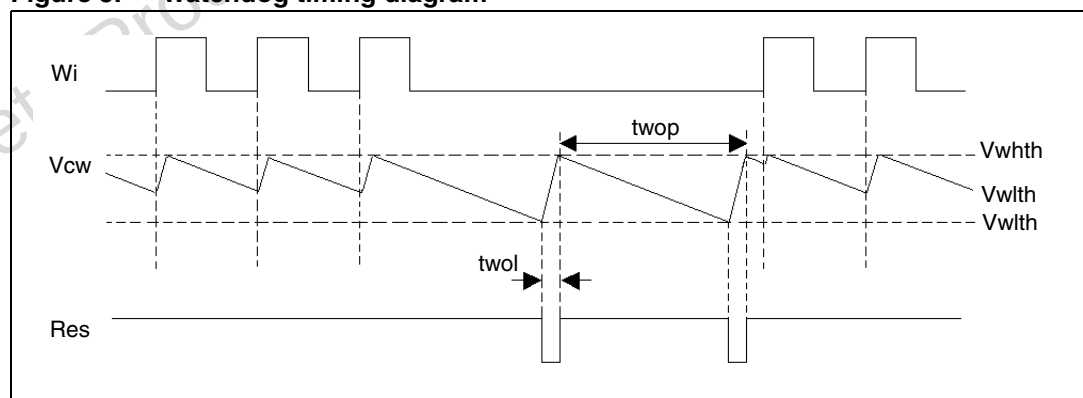
Figure 4. Reset timing diagram

3.3 Watchdog

A connected microcontroller is monitored by the watchdog input W_i . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, C_{tw} . The watchdog circuit discharges the capacitor C_{tw} , with the constant current I_{cld} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t , during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cld} \times t$$

Every W_i positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth} , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw} .

Figure 5. Watchdog timing diagram

4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4.2 SO-8 package information

Figure 6. SO-8 package dimensions

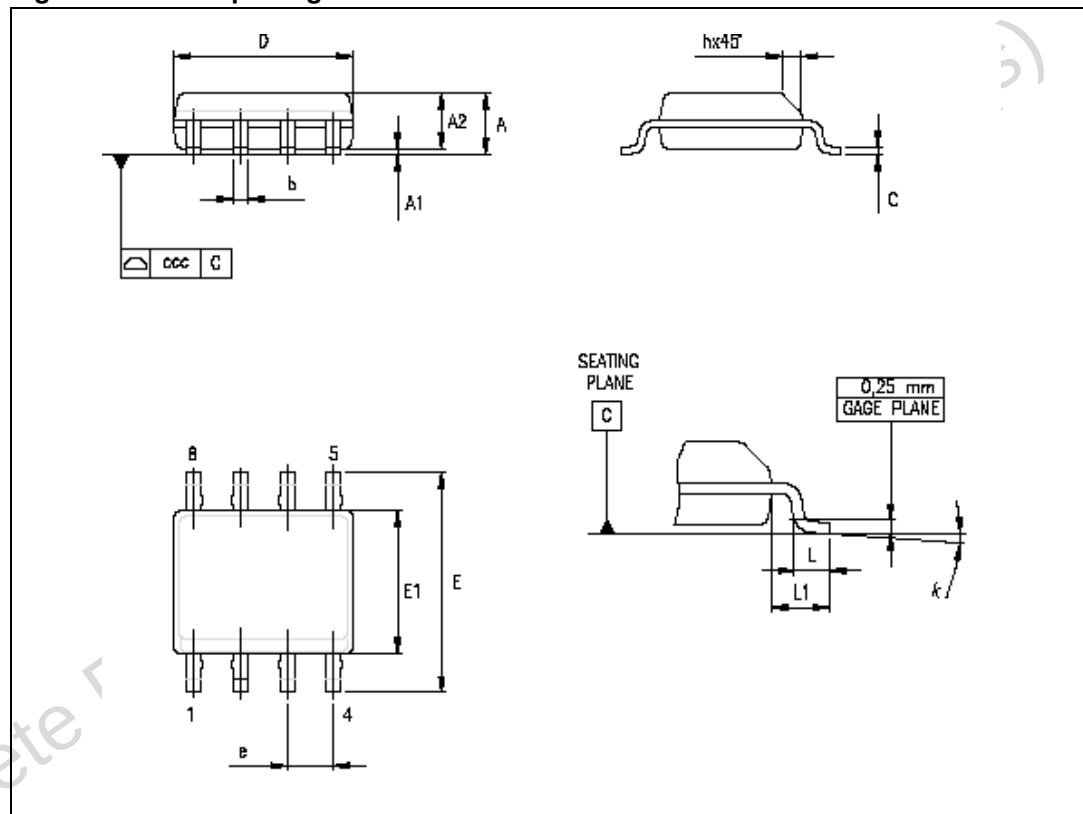


Table 9. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

4.3 SO-20 package information

Figure 7. SO-20 package dimensions

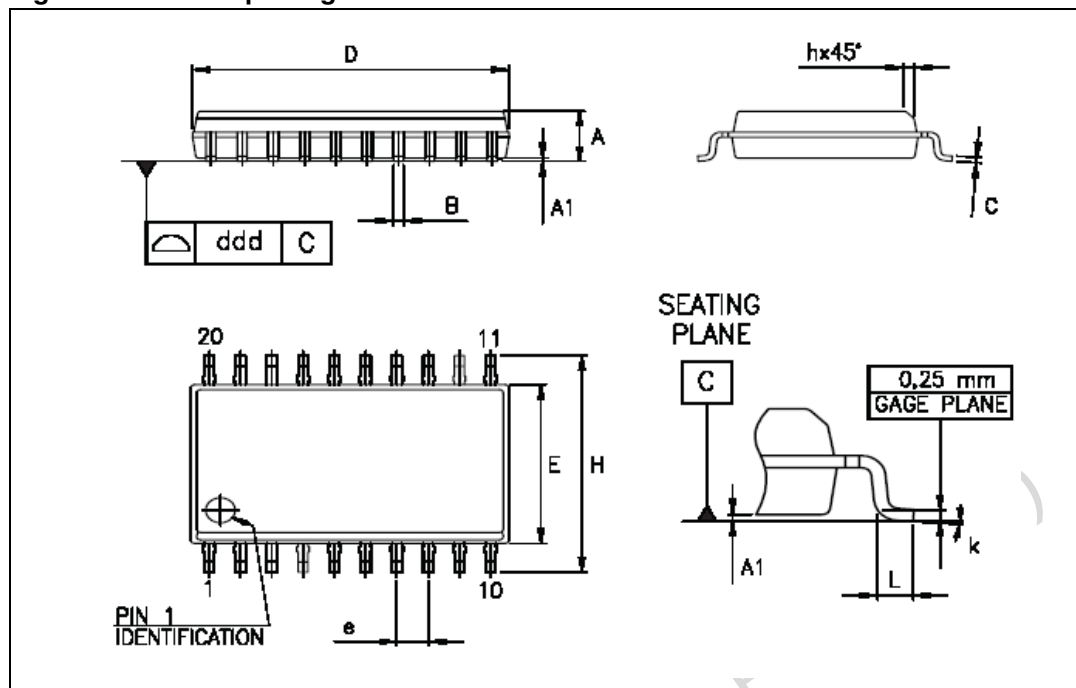


Table 10. SO-20 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D ⁽¹⁾	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

4.4 SO-8 packing information

Figure 8. SO-8 tube shipment (no suffix)

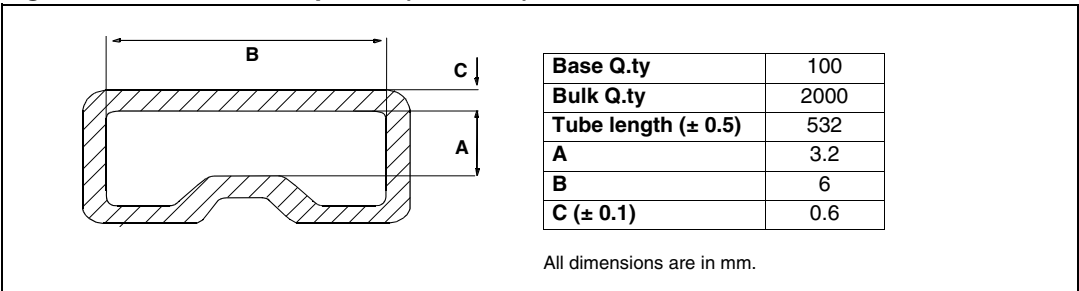
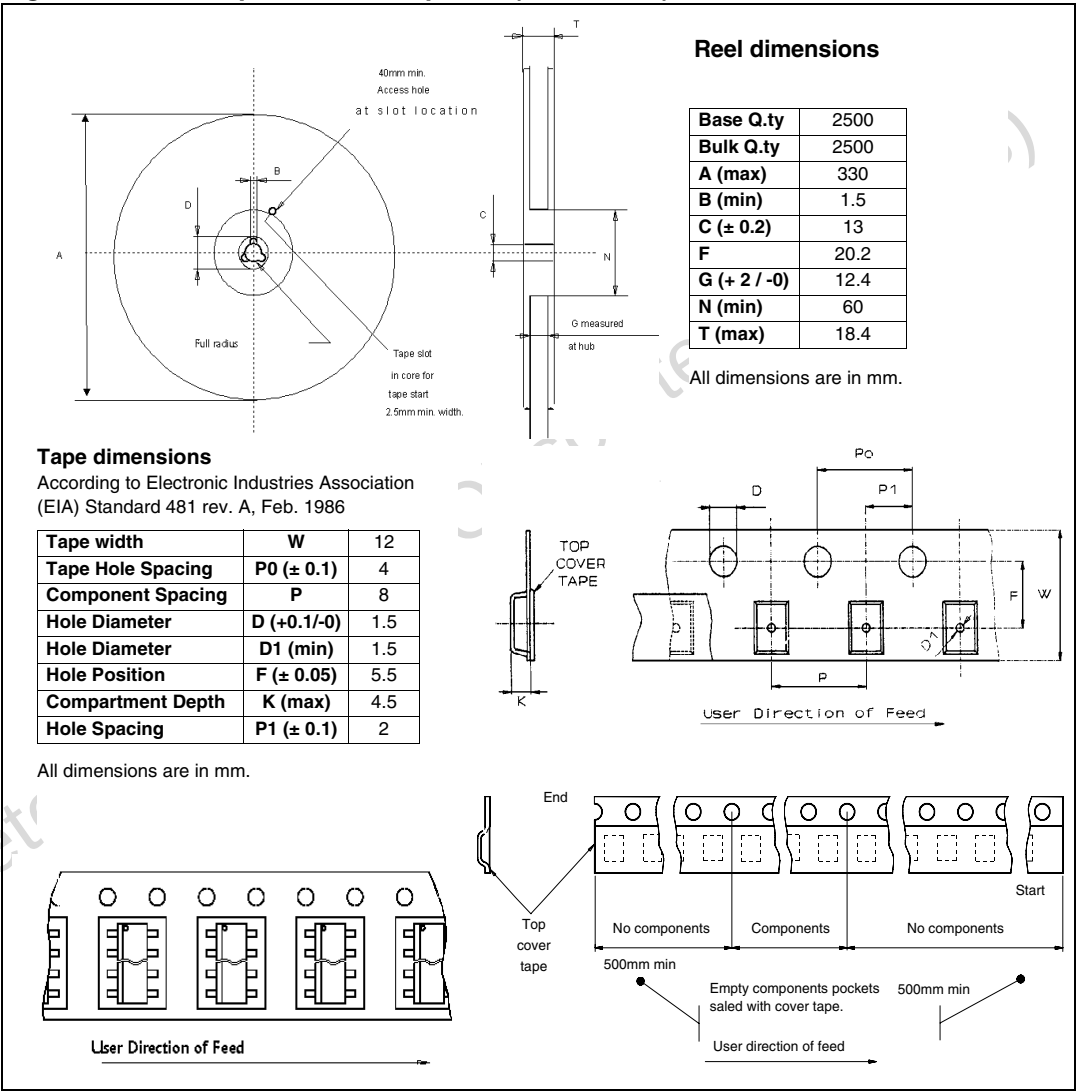


Figure 9. SO-8 tape and reel shipment (suffix "TR")



4.5 SO-20 packing information

Figure 10. SO-20 tube shipment (no suffix)

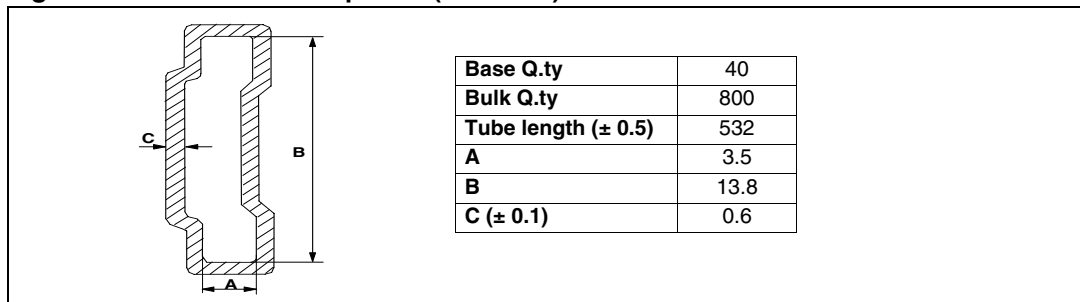
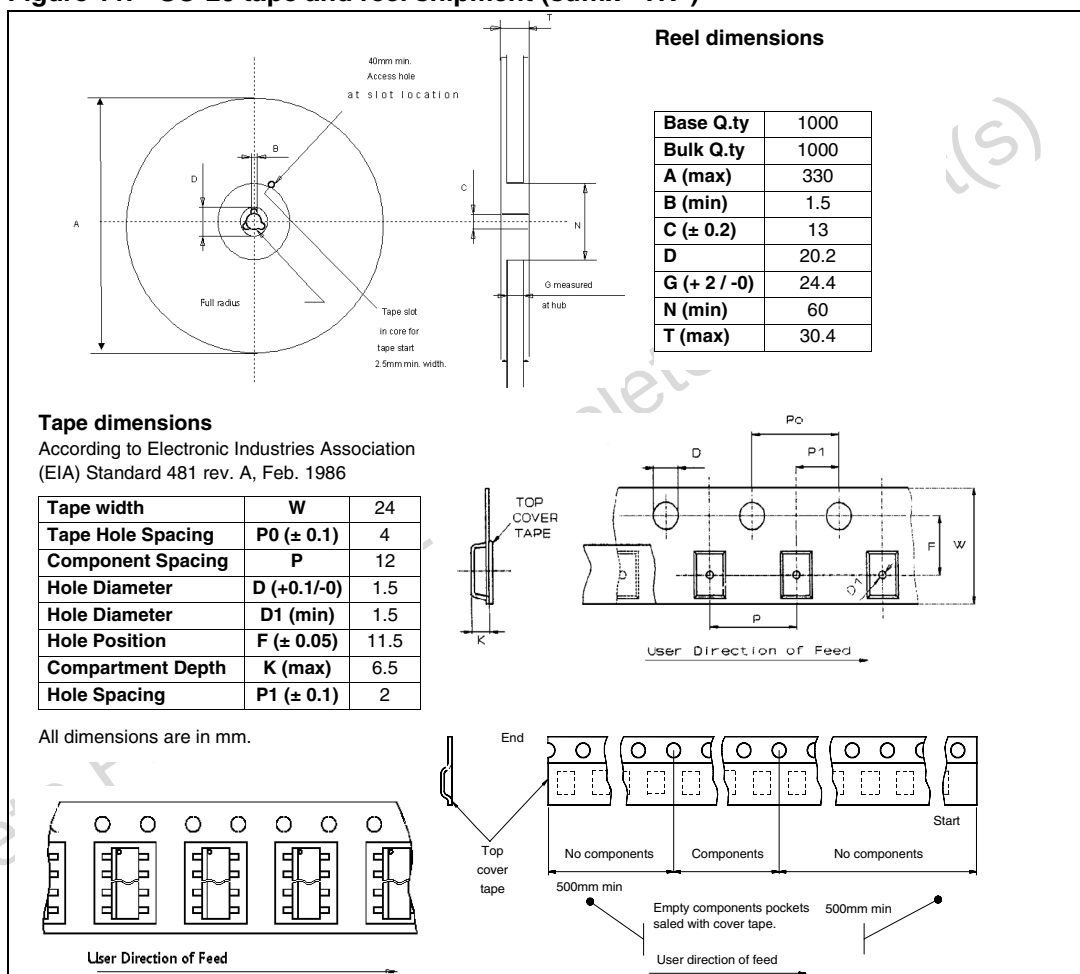


Figure 11. SO-20 tape and reel shipment (suffix "TR")



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
Mar-2004	1	Initial release
13-Feb-2007	2	Changed document maturity status. Added SO-8 packing information and SO-20 packing information .
18-Nov-2008	3	Document reformatted and restructured. Added Table 1: Device summary . Added list of contents, tables and figures. Added ECOPACK® packages information.

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