L6995S

STEP DOWN CONTROLLER FOR HIGH DIFFERENTIAL INPUT-OUTPUT CONVERSION

1 FEATURES

- CONSTANT ON TIME TOPOLOGY ALLOWS OPERATION WITH LOWER DUTY THAN PWM TOPOLOGY
- VERY FAST LOAD TRANSIENTS
- 5V V_{CC} SUPPLY
- 1.5V TO 35V INPUT VOLTAGE RANGE
- 0.9V ±1% V_{REF}
- MINIMUM OUTPUT VOLTAGE AS LOW AS 0.9V
- SELECTABLE SINKING MODE
- LOSSLESS CURRENT LIMIT
- REMOTE SENSING
- OVP,UVP LATCHED PROTECTIONS
- 600µA TYP QUIESCENT CURRENT
- POWER GOOD AND OVP SIGNALS
- PULSE SKIPPING AT LIGHT LOADS

2 APPLICATIONS

- I/O BUS FOR CPU CORE SUPPLY
- NOTEBOOK COMPUTERS
- NETWORKING DC-DC
- DISTRIBUTED POWER

Figure 1. Package

TSSOP20

Table 1. Order Codes

Part Number	Package
L6995S	TSSOP20
L6995STR	Tape & Reel

3 DESCRIPTION

The device is a step-down controller specifically designed to provide extremely high efficiency conversion, with losses current sensing tecnique.

The "constant on-time" topology assures fast load transient response. The embedded "voltage feed-forward" provides nearly constant switching frequency operation.

An integrator can be introduced in the control loop to reduce the static output voltage error.

The available remote sensing improve the static and dynamic regulation recovering the wires voltage drop. Pulse skipping technique reduces power consumption at light load. Drivers current capability allows output current in excess of 20A.

Figure 2. Minimum Component Count Application

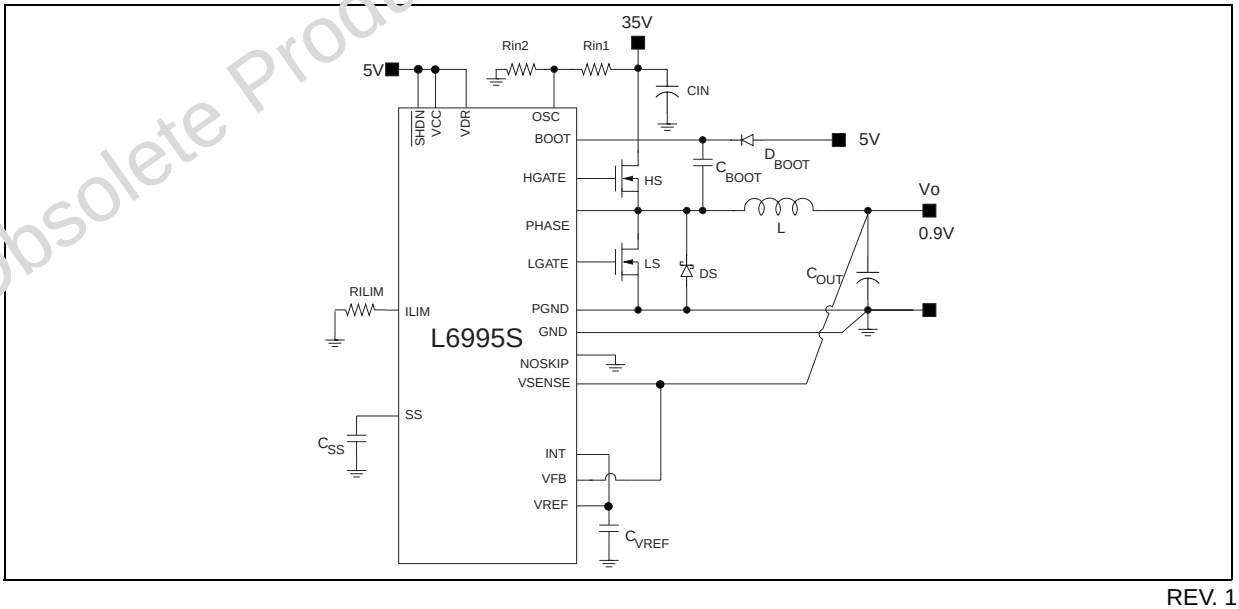


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	-0.3 to 6	V
V_{DR}	V_{DR} to GND	-0.3 to 6	V
	HGATE and BOOT, to PHASE	-0.3 to 6	V
	HGATE and BOOT, to PGND	-0.3 to 42	V
V_{PHASE}	PHASE	-0.3-to 36	V
	LGATE to PGND	-0.3 to V_{DR}+0.3	V
	ILIM, VFB, VSENSE, NOSKIP, SHDN, PGOOD, OVP, VREF, INT, GND_{SENSE} to GND	-0.3 to V_{CC}+0.3	V
BOOT, HGATE and PHASE PINS	Maximum Withstanding Voltage Range Test Condition:CDF-AEC-Q100-002 “Human Body Model” Accepatance Criteria: “Normal Performance”	±750	V
OTHER PINS		±2000	V
P_{tot}	Power dissipation at T_{amb} = 25°C	1	W
T_{stg}	Storage temperature range	-40 to 150	°C

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	125	°C/W
T_j	Junction operating temperature range	0 to 125	°C

Figure 3. Pin Connection (Top View)

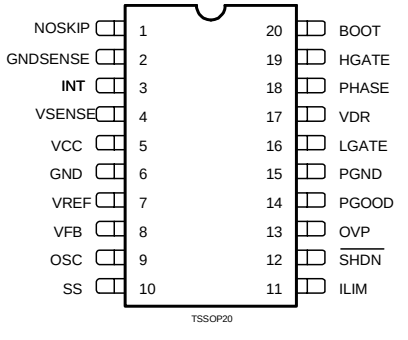


Table 4. Pin Function

N°	Name	Description
1	NOSKIP	Connect to V_{CC} to force continuous conduction mode and sink mode.
2	GNDSENSE	Remote ground sensing pin
3	INT	Integrator output. Short this pin to VFB pin and connect it via a capacitor to V_{OUT} to insert the integrator in the control loop. If the integrator is not used, short this pin to VREF.
4	VSENSE	This pin must be connected to the remote output voltage to detect overvoltage and undervoltage conditions and to provide integrator feedback input.

Table 4. Pin Function (continued)

N°	Name	Description
5	V_{CC}	IC Supply Voltage.
6	GND	Signal ground
7	VREF	0.9 V voltage reference. Connect max. a 10nF ceramic capacitor between this pin and ground. This pin is capable to source or sink up to 250uA
8	VFB	PWM comparator feedback input. Short this pin to INT pin when using the integrator function, or to VSENSE pin without integrator.
9	OSC	Connect this pin to the input voltage through a voltage divider in order to provide the feed-forward function. It cannot be left floating.
10	SS	Soft start pin. A 5µA constant current charges an external capacitor which value sets the soft-start time.
11	ILIM	An external resistor connected between this pin and GND sets the current limit threshold.
12	SHDN	Shutdown. When connected to GND the device and the drivers are OFF. It cannot be left floating.
13	OVP	Open drain output. During the over voltage condition it is pulled up by an external resistor.
14	PGOOD	Open drain output. During the soft start and in case of output voltage fault it is low. It is pulled up by external resistor.
15	PGND	Low Side driver ground.
16	LGATE	Low Side driver output.
17	V_{DR}	Low Side driver supply.
18	PHASE	Return path of the High Side driver.
19	HGATE	High side MOSFETS driver output.
20	BOOT	Bootstrap capacitor pin. High Side driver is supplied through this pin.

Table 5. Electrical Characteristics

(V_{CC} = V_{DR} = 5V; T_{amb} = 0°C to 85°C unless otherwise specified)

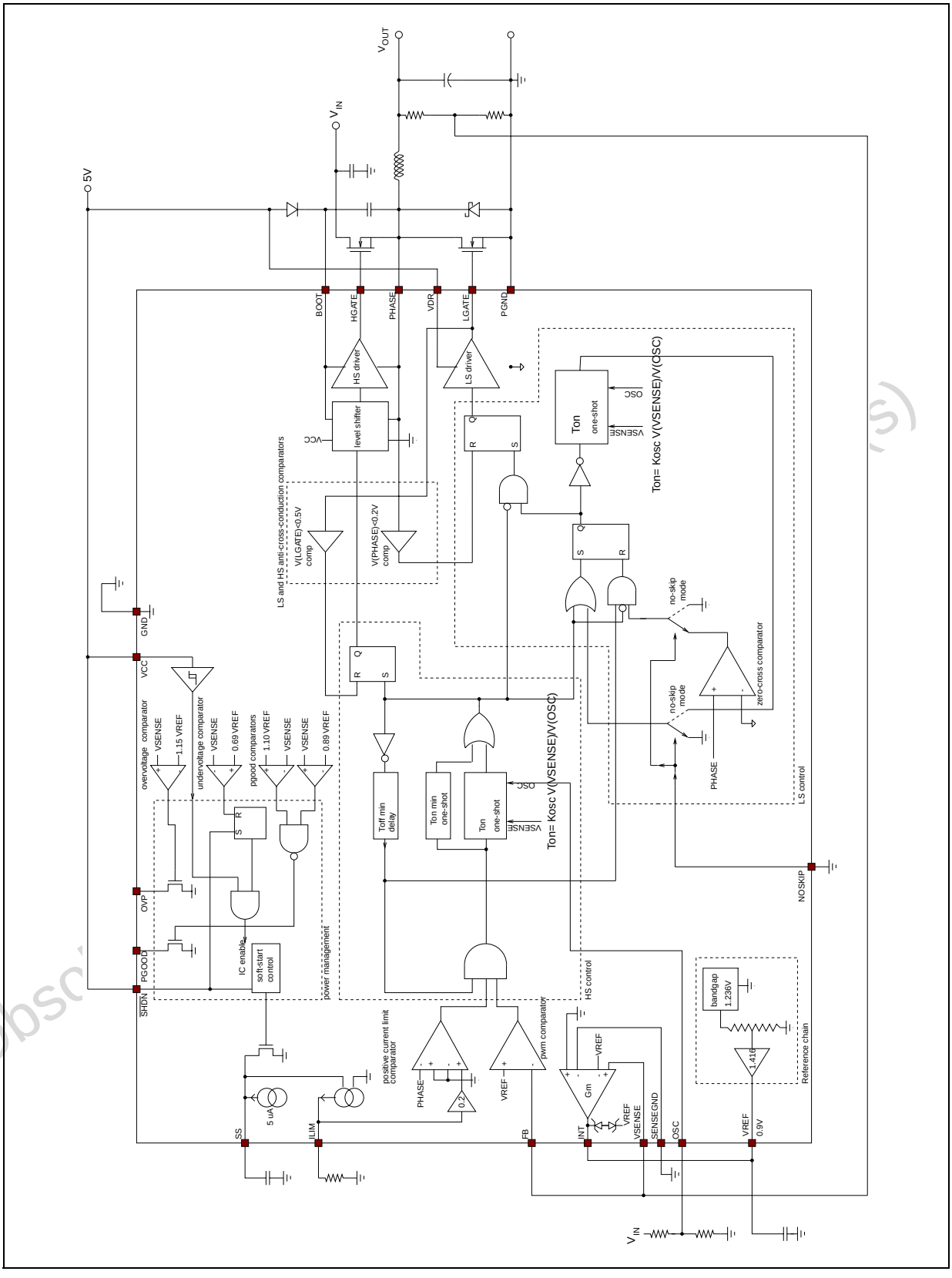
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
Vin	Input voltage range	Vout=Vref Fsw=110Khz Iout=1A	1.5		35	V
V_{CC}, V_{DR}			4.5		5.5	V
V_{CC}	Turn-onvoltage		4.2		4.4	V
	Turn-off voltage		4.1		4.3	V
	Hysteresis			100		mV
IqV_{DR}	Quiescent Current Drivers	VFB > VREF			20	µA
IqVcc	Device Quiescent current	VFB > VREF		400	600	µA
SHUTDOWN SECTION						
SHDN	Device On		1.2			V
	Device Off				0.6	V
$I_{SH}V_{DR}$	Drivers shutdown current	SHDN to GND			5	µA
$I_{SH}V_{CC}$	Devices shutdown current	SHDN to GND		10	15	µA
SOFT START SECTION						
I_{SS}	Soft Start current	V_{SS} = 0.8V	4		6	µA
	SS Clamp Voltage			4		V
	Soft start active range		400	450	500	mV

Table 5. Electrical Characteristics (continued)

(V_{CC} = V_{DR} = 5V; T_{amb} = 0°C to 85°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CURRENT LIMIT AND ZERO CURRENT COMPARATOR						
	ILIM input bias current	R_{ILIM} = 2KΩ to 400KΩ	4.9	5	5.1	µA
	Zero Crossing Comparator Offset Phase-gnd		-2		2	mV
ON TIME						
Ton	On time duration	VREF=VSENSE OSC=250mV	850	950	1050	ns
		VREF=VSENSE OSC=500mV	470	520	570	ns
		VREF=VSENSE OSC=1V	250	285	320	ns
		VREF=VSENSE OSC=2V	130	160	190	ns
OFF TIME						
T_{OFFMIN}	Minimum off time				580	ns
	K_{OSC}/T_{OFFMIN}	OSC=250mV	0.30		0.60	
VOLTAGE REFERENCE						
VREF	Voltage Accuracy	0µA < I_{REF} < 100µA	0.891	0.9	0.909	V
PWM COMPARATOR						
	Input voltage offset		-2		+2	mV
I_{FB}	Input Bias Current			0.1		µA
INTEGRATOR						
INT	Over Voltage Clamp	V_{SENSE} = V_{CC}	1.04	1.07	1.1	V
INT	Under Voltage Clamp	V_{SENSE} = GND	0.82	0.84	0.86	V
	Integrator Input Offset Voltage V_{SENSE}-V_{REF}		-5		5	mV
I_{VSENSE}	Input Bias Current			0.1		µA
GATE DRIVERS						
	High side rise time	V_{DR}=3.3V; C=7nF HGATE - PHASE from 1 to 3V		50	70	ns
	High side fall time			50	70	ns
	Low side rise time	V_{DR}=3.3V; C=14nF LGATE from 1 to 3V		50	70	ns
	Low side fall time			50	70	ns
P_{GOOD} UVP/OVP PROTECTIONS						
OVP	Over voltage threshold	with respect to V_{REF}	112	115	118	%
UVP	Under voltage threshold		66	69	72	%
PGOOD	Upper threshold (V_{SENSE}-V_{REF})	V_{SENSE} rising	107	110	113	%
PGOOD	Lower threshold (V_{SENSE}-V_{REF})	V_{SENSE} falling	86	89	92	%
V_{PGOOD}		I_{Sink}=2mA		0.14	0.2	V

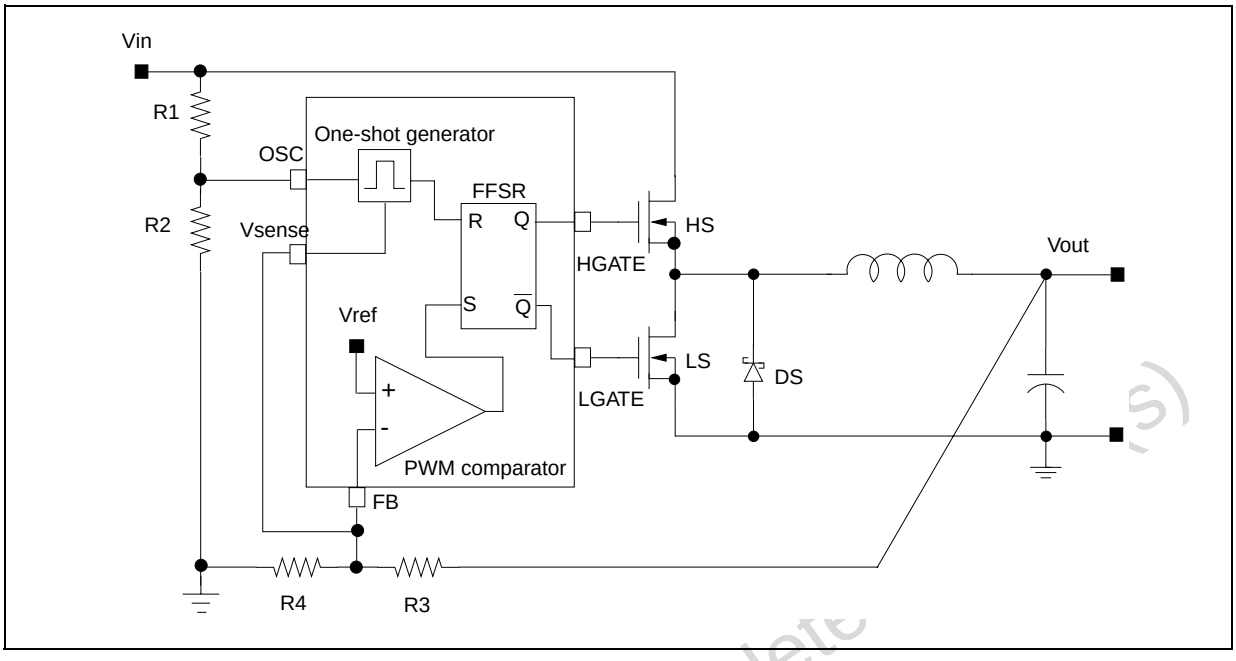
Figure 4. Functional & Block Diagram



4 DEVICE DESCRIPTION

4.1 Constant On Time PWM topology

Figure 5. Loop block schematic diagram



The device implements a Constant On Time control scheme, where the Ton is the high side MOSFET on time duration forced by the one-shot generator. The on time is directly proportional to VSENSE pin voltage and inverse to OSC pin voltage as in Eq1:

Eq 1 $$T_{ON} = K_{OSC}\frac{V_{SENSE}}{V_{OSC}} + \tau$$

where K_{OSC} = 250ns and τ is the internal propagation delay time (typ. 70ns). The system imposes in steady state a minimum on time corresponding to V_{OSC} = 2V. In fact if the V_{OSC} voltage increases above 2V the corresponding Ton will not decrease. Connecting the OSC pin to a voltage partition from V_{IN} to GND, it allows a steady-state switching frequency F_{SW} independent of V_{IN}. It results:

Eq 2 $$f_{SW} = \frac{V_{OUT}}{V_{IN}}\frac{1}{T_{ON}} = \frac{\alpha_{OSC}}{\alpha_{OUT}}\frac{1}{K_{OSC}} \rightarrow \alpha_{OSC} = f_{SW}K_{OSC}\alpha_{OUT}$$

where

Eq 3 $$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}} = \frac{R_2}{R_2 + R_1}$$

Eq 4 $$\alpha_{OUT} = \frac{V_{FB}}{V_{OUT}} = \frac{R_4}{R_3 + R_4}$$

The above equations allow setting the frequency divider ratio α_{OSC} once output voltage has been set; note that such equations hold only if V_{OSC}<2V. Further the Eq2 shows how the system has a switching frequency ideally independent from the input voltage. The delay introduces a light dependence from V_{IN}. A minimum off-time constrain of about 580ns is introduced in order to assure the boot capacitor charge and to limit the switching fre-

quency after a load transient as well as to mask PWM comparator output against noise and spikes.

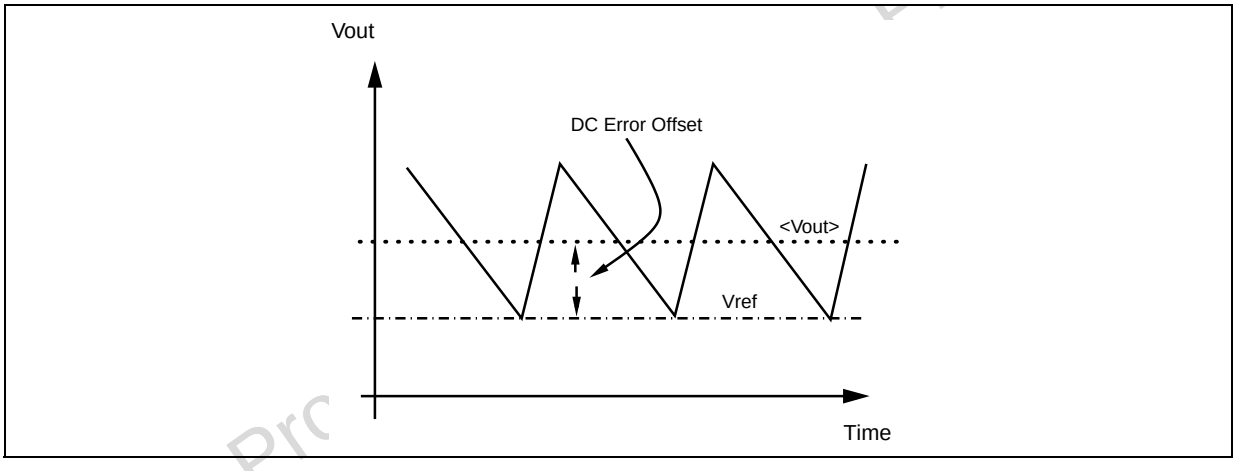
The system has not an internal clock, because this is a hysteretic controller, so the turn on pulse will start if three conditions are met contemporarily: the FB pin voltage is lower than the reference voltage, the minimum off time is passed and the current limit comparator is not triggered (i.e. the inductor current is below the current limit value). The voltage on the OSC pin must range between 50mV and 2V to ensure the system linearity.

4.2 Closing the loop

The loop is closed connecting the output voltage (or the output divider middle point) to the FB pin. The FB pin is linked internally to the comparator negative pin and the positive pin is connected to the reference voltage (0.9V Typ.) as in Figure 2. When the FB goes lower than the reference voltage, the PWM comparator output goes high and sets the flip-flop output, turning on the high side MOSFET. This condition is latched to avoid noise spike. After the on-time (calculated as described in the previous section) the system resets the flip-flop and then turns off the high side MOSFET and turns on the low side MOSFET. Internally the device has more complex logic than a flip-flop to manage the transition in correct way. For more details refers to the Figure 3.

The voltage drop along ground and supply metals connecting output capacitor to the load is a source of DC error. Further the system regulates the output voltage valley value not the average, as in the Figure 5 is shown. So the voltage ripple on the output capacitor is a source of DC static error (as the PCB traces). To compensate the DC errors, an integrator network must be introduced in the control loop, by connecting the output voltage to the INT pin through a capacitor and the FB pin to the INT pin directly as in Figure 6. The internal integrator amplifier with the external capacitor C_{INT1} introduces a DC pole in the control loop. C_{INT1} also provides an AC path for output ripple.

Figure 6. Valley regulation



The integrator amplifier generates a current, proportional to the DC errors, that increases the output capacitance voltage in order to compensate the total static errors. A voltage clamper within the device forces INT pin voltage ranges from V_{REF}-50mV, V_{REF}+150mV. This is useful to avoid or smooth output voltage overshoot during a load transient. Also, this means that the integrator is capable of recovering output error due to ripple when its peak-to-peak amplitude is less than 150mV in steady state.

In case of the ripple amplitude is larger than 150mV, a capacitor C_{INT2} can be connected between INT pin and ground to reduce ripple amplitude at INT pin, otherwise the integrator can operate out of its linear range. Choose C_{INT1} according to the following equation:

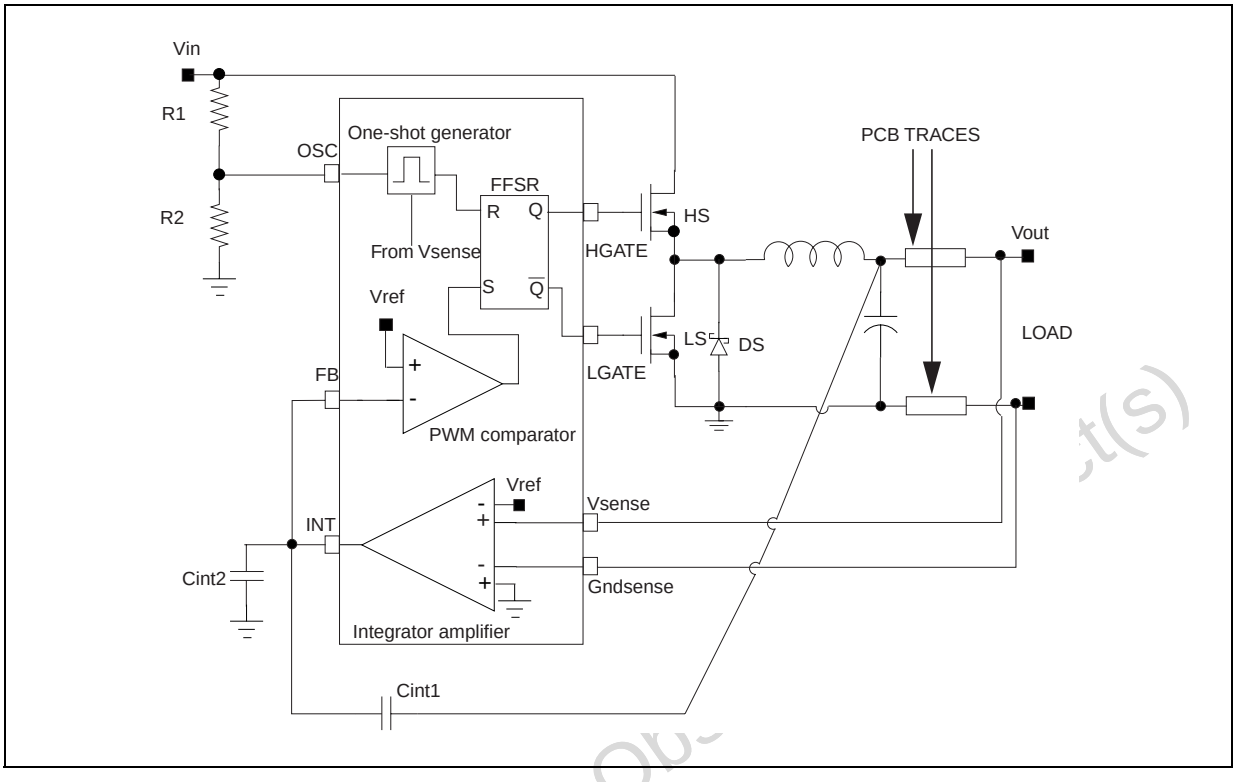
Eq 5 $$C_{INT1} = \frac{g_{INT} \cdot \alpha_{OUT}}{2 \cdot \pi \cdot F_u}$$

where GINT=50 µs is the integrator transconductance, α_{OUT} is the output divider ratio given from Eq4 and F_U is the close loop bandwidth. This equation also holds if C_{INT2} is connected between INT pin and ground. C_{INT2} is given by:

Eq 6 $$\frac{C_{INT2}}{C_{INT1}} = \frac{\Delta V_{OUT}}{V_{INT}}$$

Where ΔV_{OUT} is the output ripple and ΔV_{INT} is the ripple wanted at the INT pin (100mV typ).

Figure 7. Integrator loop block diagram



Respect to a traditional PWM controller, that has an internal oscillator setting the switching frequency, in a hysteretic system the frequency can change with some parameters (input voltage, output current). In L6995S is implemented the voltage feed-forward circuit that allows constant switching frequency during steady-sate operation with the input voltage variation. There are many factors affecting switching frequency accuracy in steady-state operation. Some of these are internal as dead times, which depend on high side MOSFET driver. Others related to the external components as high side MOSFET gate charge and gate resistance, voltage drops on supply and ground rails, low side and high side RDSON and inductor parasitic resistance.

During a positive load transient, (the output current increases), the converter switches at its maximum frequency (the period is TON+TOFFmin) to recover the output voltage drop. During a negative load transient, (the output current decreases), the device stops to switch (high side MOSFET remains off).

4.3 Transition from PWM to PFM/PSK

To achieve high efficiency at light load conditions, PFM mode is provided. The PFM mode differs from the PWM mode essentially for the off section; the on section is the same. In PFM after a turn-on cycle the system turns-on the low side MOSFET, until the inductor current reaches the zero A value, when the zero-crossing comparator turns off the low side MOSFET. In this way the energy stored in the output capacitor will not flow to ground, through the low side MOSFET, but it will flow to the load. In PWM mode, after a turn on cycle, the system keeps the low side MOSFET on until the next turn-on cycle, so the energy stored in the output capacitor will flow through the low side MOSFET to ground. The PFM mode is naturally implemented in hysteretic controller, in fact in PFM mode the system reads the output voltage with a comparator and then turns on the high side MOSFET when the output voltage goes down a reference value. The device works in discontinuous mode at light load and in continuous mode at high load. The transition from PFM to PWM occurs when load current is around half the inductor current ripple. This threshold value depends on V_{IN}, L, and V_{OUT}. Note that the higher the in-

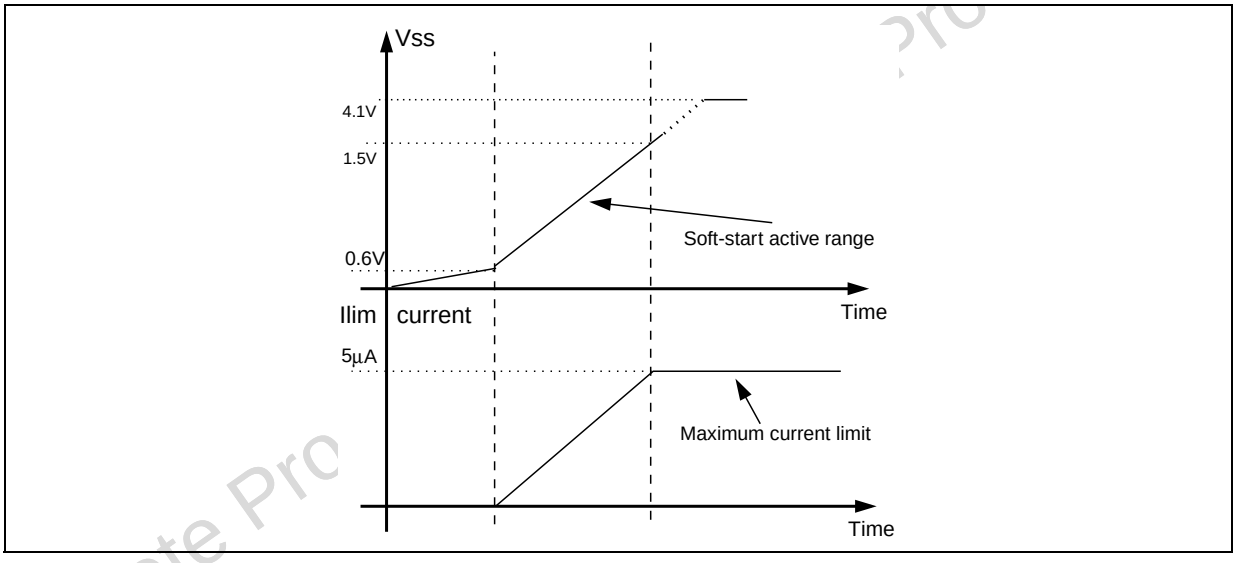
ductor value is, the smaller the threshold is. On the other hand, the bigger the inductor value is, the slower the transient response is. In PFM mode the frequency changes, with the output current changing, more than in PWM mode; in fact if the output current increase, the output voltage decreases more quickly; so the successive turn-on arrives before, increasing the switching frequency. The PFM waveforms may appear more noisy and asynchronous than normal operation, but this is normal behaviour mainly due to the very low load. If the PFM is not compatible with the application it can be disabled connecting to V_{CC} the NOSKIP pin.

4.4 Softstart

If the supply voltages are already applied, the SHDN pin gives the start-up. The system starts with the high side MOSFET off and the low side MOSFET on. After the SHDN pin is turned on the SS pin voltage begins to increase and the system starts to switch. The softstart is realized by gradually increasing the current limit threshold to avoid output overvoltage. The active soft start range for the V_{SS} voltage (where the output current limit increase linearly) starts from 0.6V to 1.5V. In this range an internal current source (5µA Typ) charges the capacitor on the SS pin; the reference current (for the current limit comparator) forced through ILIM pin is proportional to SS pin voltage and it saturates at 5µA (Typ.) when SS voltage is close to 1.5V and the maximum current limit is active. Undervoltage protection is disabled until SS pin voltage reaches 1.5V; instead the overvoltage is always present (see figure 7).

Once the SS pin voltage reaches the 1.5V value, the voltage on SS pin doesn't impact the system operation anymore. If the SHDN pin is turned on before the supplies, the correct start-up sequence is the following: first turn-on the power section and after the logic section (V_{CC} pin).

Figure 8. Soft -Start Diagram



Because the system implements the soft start controlling the inductor current, the soft start capacitor selection is function of the output capacitance, the current limit and the soft start active range (ΔV_{SS}).

In order to select the softstart capacitor it must be imposed that the output voltage reaches the final value before the soft start voltage reaches the under voltage value (1.5V). In other words the output voltage charging time has to be lower than the uvp time.

The UVP time is given by:

$$\text{Eq 7} \qquad T_{uvp}(C_{SS}) = \frac{V_{uvp}}{Iss} \cdot C_{SS}$$

In order to calculate the output volatge chargin time it should be calculated, before, the output volatrge function versus time. This function can be calculated from the inductor current function; the inductor current function can

be supposed linear function of the time.

Eq 8 $$I_L(t,C_{SS}) = \frac{(R_{ilim}/R_{dson} \cdot K_C \cdot I_{SS} \cdot t)}{(\Delta V_{SS} \cdot C_{SS})}$$

so the output voltage is given by:

Eq 9 $$V_{out}(t,C_{SS}) = \frac{Q(t,C_{SS})}{C_{out}} = \frac{(R_{ilim}/R_{dson} \cdot K_C \cdot I_{SS} \cdot t^2)}{(C_{out} \cdot \Delta V_{SS} \cdot C_{SS} \cdot 2)}$$

calling V_{out} as the V_{out} final value, the output charging time can be estimated as:

Eq 10 $$I_{out}(C_{SS}) = \left[\frac{(V_{out} \cdot C_{out} \cdot \Delta V_{SS} \cdot C_{SS} \cdot 2)}{(R_{ilim}/R_{dson} \cdot K_C \cdot I_{SS})}\right]^{0.5}$$

the minimum C_{SS} value is given imposing this condition:

Eq 11 $T_{out} = T_{uvp}$

4.5 Current limit

The current limit comparator senses the inductor current through the low side MOSFET RDS_{ON} drop and compares this value with the ILIM pin voltage value. While the current is above the current limit value, the control inhibits the one-shot start.

To properly set the current limit threshold, it should be noted that this is a valley current limit. Average current depends on the inductor value, V_{IN} V_{OUT} and switching frequency.

The average output current in current limit is given by:

Eq 12 $$I_{OUT_{CL}} = I_{max\ valley} + \frac{\Delta I}{2}$$

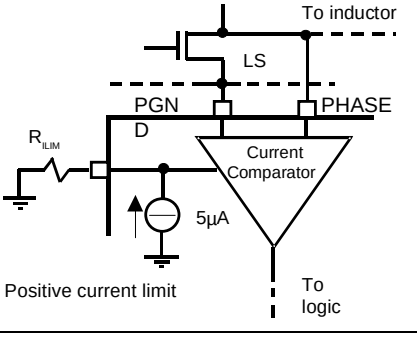
Thus, to set the current threshold, choose RILIM according to the following equation:

Eq 13 $$I_{max\ valley} = \frac{R_{ILim}}{Rds_{on}} \cdot \frac{I_{Lim}}{5.2}$$

In current limit the system keeps the current constant until the output voltage meets the undervolatge threshold. The system is capable to sink current, but it has not a negative current limit.

The system accuracy is function of the exactness of the resistance connected to ILIM pin and the low side MOSFET RDS_{ON} accuracy. Moreover the voltage on ILIM pin must range between 10mV and 2V to ensure the system linearity.

Figure 9. Current limit schematic



4.6 Protection and fault

Sensing VSENSE pin voltage performs output protection. The nature of the fault (that is, latched OV or latched UV) is given by the PGOOD and OVP pins. If the output voltage is between the 89% (typ.) and 110% (typ) of the regulated value, PGOOD is high. If a hard overvoltage or an undervoltage occurs, the device is latched: low side MOSFET is turned on, high side MOSFET is turned off and PGOOD goes low. In case the system detects an overvoltage the OVP pin goes high.

To recover the functionality the device must be shut down and restarted thought the SHDN pin, or the supply has to be removed, and restart with the correct sequence.

These features are useful to protect against short-circuit (UV fault) as well as high side MOSFET short (OV fault).

4.7 Drivers

The integrated high-current drivers allow using different size of power MOSFET, maintaining fast switching transition. The driver for the high side MOSFET uses the BOOT pin for supply and PHASE pin for return (floating driver). The driver for the low side MOSFET uses the VDR pin for the supply and PGND pin for the return. The main feature is the adaptive anti-cross-conduction protection, which prevents from both high side and low side MOSFET to be on at the same time, avoiding a high current to flow from VIN to GND. When high side MOSFET is turned off the voltage on the pin PHASE begins to fall; the low side MOSFET is turned on only when the voltage on PHASE pin reaches 250mV. When low side is turned off, high side remains off until LGATE pin voltage reaches 500mV. This is important since the driver can work properly with a large range of external power MOSFETS.

The current necessary to switch the external MOSFETS flows through the device, and it is proportional to the MOSFET gate charge and the switching frequency. So the power dissipation of the device is function of the external power MOSFET gate charge and switching frequency.

Eq 14 $$P_{driver} = V_{cc} \cdot Q_{gTOT} \cdot F_{SW}$$

The maximum gate charge values for the low side and high side are given from:

Eq 15 $$Q_{MAXHS} = \frac{f_{SW0}}{f_{SW}} \cdot 75nC$$

Eq 16 $$Q_{MAXLS} = \frac{f_{SW0}}{f_{SW}} \cdot 125nC$$

Where f_{SW0} = 500Khz. The equations above are valid for T_J = 150°C. If the system temperature is lower the Q_G can be higher.

For the Low Side driver the max output gate charge meets another limit due to the internal traces degradation; in this case the maximum value is Q_{MAXLS} = 125nC.

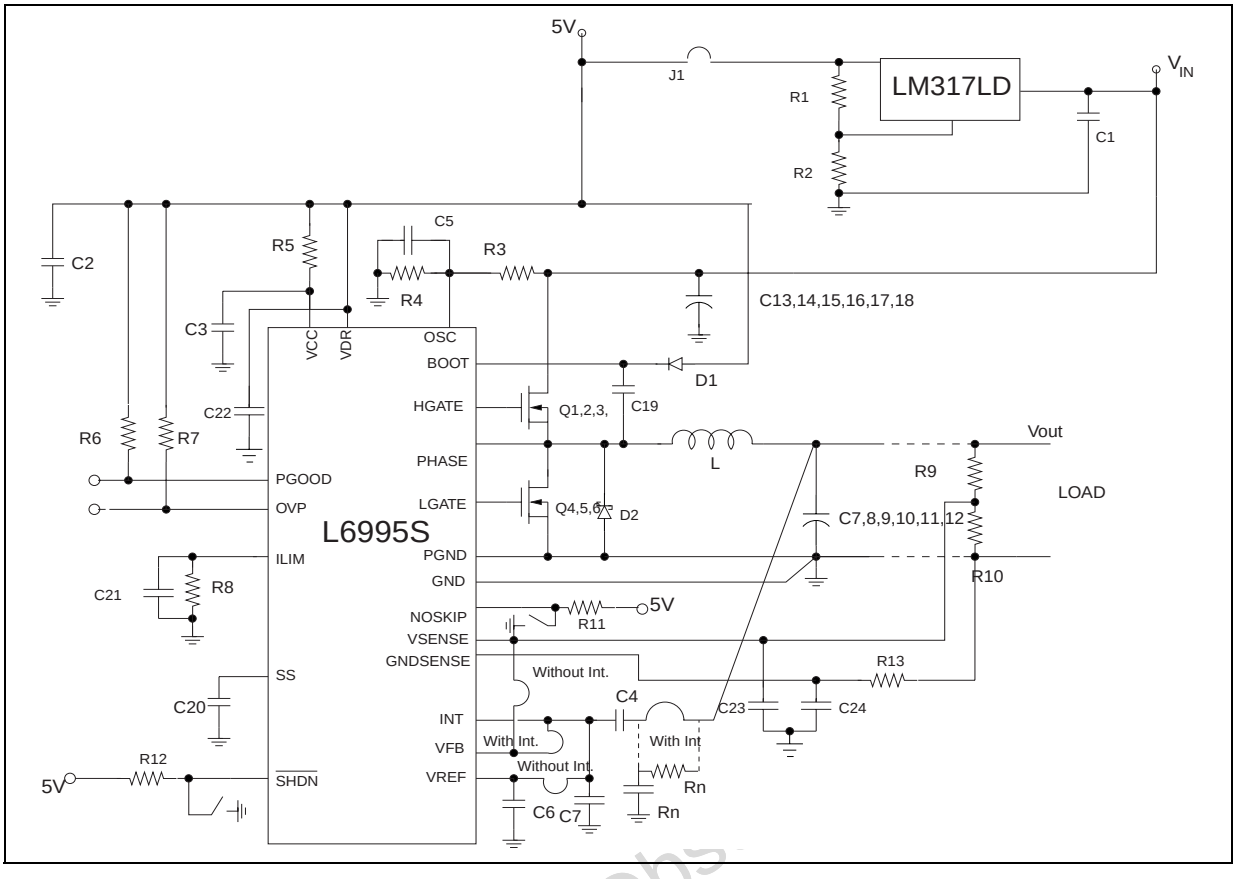
The low side driver has been designed to have a low resistance pull-down transistor, around 0.5 ohms. This prevents the voltage on LGATE pin raises during the fast rise-time of the pin PHASE, due to the Miller effect.

5 APPLICATION INFORMATION

5.1 20A Demo board description

The demoboard shows the device operation in general purpose applications. The evaluation board allows using only one supply because the on board linear regulator LM317LD; the linear regulator supplies the device through the J1. Output current in excess of 20A can be reached dependently on the MOSFET type. The SW1 is used to start the device (when the supplies are already present) and to select the PFM/PWM mode.

Figure 10. Demoboard Schematic Diagram



5.2 Jumper Connection

Table 6. Jumper connection with integrator

Component	Connection
C4	Mounted
C7	Mounted *
INT	Close
NOINT	Open

* This component is not necessary, depends from the output ESR capacitor. See the integrator section.

Table 7. Jumper connection without integrator

Component	Connection
C4	Not mounted
C7	Not Mounted
INT	Open
NOINT	Close

5.3 NOTE

There is a linear regulator on board, it allows to use one generator (only for the power section, in fact the IC section is powered by the linear regulator); if the regulator is used close the J1, other wise it has to keep open.

Be careful measuring the efficiency with the linear regulator asserted.

At high current in the integrator configuration (around 20A), it can be seen an oscillation in the switching frequency due to the noise interaction, to reduce this oscillation put a noise filter R_N, C_N like in the figure 9. Note the R_N resistor is in the place of the INT jumper near C4. R_N, C_N, should be selected with a pole frequency around 1Mhz, but anyway higher than switching frequency (five times).

5.4 DEMOBOARD LAYOUT

Real dimensions: 5,7 cm X 7,7 cm (2,28inch X 3, 08inch)

Figure 11. PCB layout: bottom side

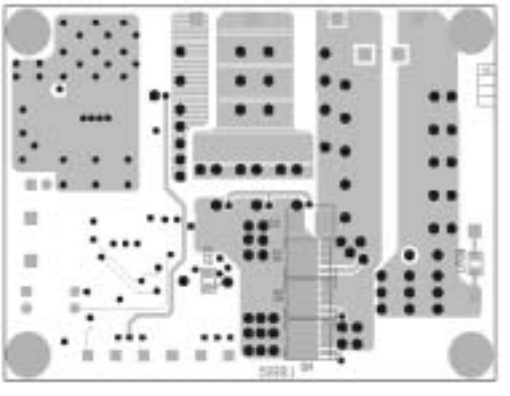


Figure 12. PCB Layout: Top side

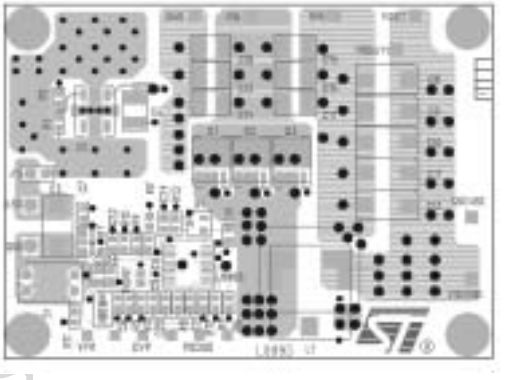


Figure 13. Internal ground plane

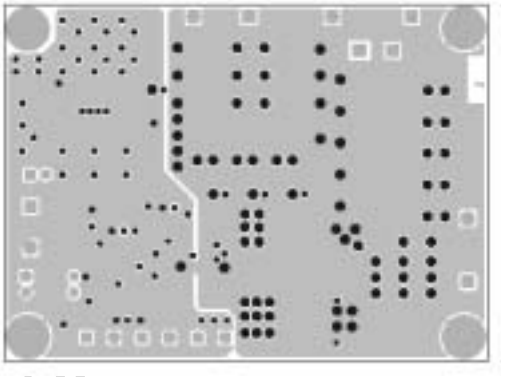


Figure 14. Power & signal plane

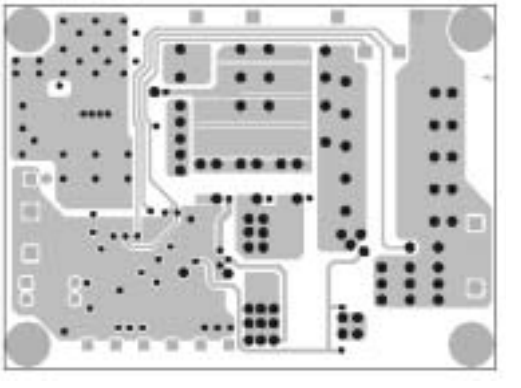


Table 8. PCB Layout guidelines

Goal	Suggestion
Low radiation and low magnetic coupling with the adjacent circuitry.	1) Small switching current loop areas. (For example placing C_{IN}, High Side and Low side MOSFETS, Shottky diode as close as possible). 2) Controller placed as close as possible to the power MOSFET. 3) Group the gate drive component (Boot cap and diode together near the IC.
Don't penalty the efficiency.	Keep power traces and load connections short and wide.
Ensure high accuracy in the current sense system.	Phase pin and PGND pin must be made with Kelvin connection and as close as possible to the Low Side MOSFETS.
Reduce the noise effect on IC.	1) Put the feedback component (like output divider, integrator network, etc) as close as possible to the IC. 2) The feedback traces must be parallel and as close as possible. Moreover they must be routed as far as possible from the switching current loops. 3) Make the controller ground connection like the figure 19.

Table 9. Component list

The component list is shared in two sections: the first for the general-purpose component, the second for power section:

GENERAL-PURPOSE SECTION

Part name	Value	Dimension	Notes
RESISTOR			
R1	100Ω	0603	Output resistor divider for the linear regulator.
R2	300Ω	0603	
R3	560kΩ	0603	Input resistor divider (To set switching frequency)
R4	33kΩ	0603	
R5	47Ω	0603	
R6, R7, R11, R12	33kΩ	0603	
R8	47kΩ	0603	Current limit resistor (To set current limit)
R9	390Ω	0603	Output resistor divider (To set output voltage)
R10	1KΩ	0603	
R13	220Ω	0603	
CAPACITOR			
C1	220nF	0805	
C2	47µF	KEMET-16V	
C3	220nF	0805	
C4	330pF	0603	First integrator capacitor
C5	47pF	0603	
C6	10nF	0603	
C7	N.M.	0603	Second integrator capacitor
C19	220nF	0805	
C20	220nF	0603	Softstart capacitor

Part name	Value	Dimension	Notes
C21	47pF	0603	
C22	220nF	0805	
C23		0603	N.M.
C24	1nF	0603	
C25	1uF	Tantalum	
DIODES			
D1	BAT54		25V

POWER SECTION

OUTPUT CAPACITORS			
C10-C11-C12	3X330uF	EEFUE0D331R PANASONIC	Output capacitor C8, C9 N.M.
INPUT CAPACITORS			
C13, C14, C16, C17, C15 C18	10uF	C34Y5U1E106Z TOKIN	Input capacitor
	10uF	C3225Y5V1E106Z TDK	
Part name	**Value**	**Dimension**	**Notes**
	10uF	ECJ4XF1E106Z PANASONIC	
	10uF	TMK325F106ZH TAIYO YUDEN	
INDUCTOR			
L1	0.6µH	ETQP6F0R6BFA PANASONIC	
	0.6µH	A959ASR60N TOKO	
	0.6µH	DXM1306-R60-T COEV	
	0.6µH	CEP12D38H0R6 SUMIDA	
POWER MOS			
Q1,Q2	STS11NF3LL	STMicroelectronics	Q3 N.M.
	STSJ25NF3LL	STMicroelectronics	Q3 N.M.
Q5,Q6	STS25NH3LL	STMicroelectronics	Q4 N.M.
DIODES			
D2	STPS3L40U	STMicroelectronics	25V
INTEGRATED CIRCUIT			
U1	LM317LD		Linear regulator
U2	L6995S		
Switcher			

Notes: 1. N.M.=Not Mounted
2. The demoboard with this component list is set to give: V_{OUT} = 1.25V, F_{SW} = 270kHz with an input voltage around V_{IN} = 20V with the integrator feature, and with 20A continuos output current.
3. All capacitors are intended ceramic type otherwise specified.

6 STEP BY STEP DESIGN

V_{IN} = 20V V_{OUT} = 1.25V I_{OUT} = 20A F_{SW} = 270kHz

In this design it is considered a low profile demoboard, so a great attention is given to the components height.

6.1 Input capacitor.

A pulsed current (with zero average value) flows through the input capacitor of a buck converter. The AC component of this current is quite high and dissipates a considerable amount of power on the ESR capacitor:

Eq 17 $$P_{CIN} = ESR_{CIN} \cdot Iout^2 \cdot \frac{Vin \cdot (Vin - Vout)}{Vin^2}$$

The I_{RMS} current is given by:

Eq 18 $$Icin_{rms} = \sqrt{Iout^2 \delta(1-\delta) + \frac{\delta}{12}(\Delta I_L)^2}$$

Neglecting the last term, the equation reduces to:

Eq 19 $$Icin_{rms} = Iout\sqrt{\delta(1-\delta)}$$

which maximum value corresponds to $\delta = 1/2$.

$ICIN_{RMS}$, has a maximum equal to $\delta = 1/2$ (@ VIN = 2×VOUT, that is, 50% duty cycle). The input capacitor, therefore, should be selected with an RMS rated current higher than $ICIN_{RMS}$. Electrolytic capacitors are the most used because are the cheapest ones and are available with a wide range of RMS current ratings. The only drawback is that, considering a requested ripple current rating, they are physically larger than other capacitors. Very good tantalum capacitors are coming available, with very low ESR and small size. The only problem is that they occasionally can burn out if subjected to very high current during the charge. So, it is better avoid this type of capacitors for the input filter of the device. In fact, they can be subjected to high surge current when connected to the power supply. If available for the requested value and voltage rating, the ceramic capacitors have usually a higher RMS current rating for a given physical size (due to the very low ESR). From the equation 18 it is found:

$$Icin_{rms} = 4.8A$$

Considering 10µF capacitors ceramic, that have $ICIN_{RMS}$ =1.5A, 6 pzs. are needed.

6.2 Inductor

In order to determine the inductor value is necessary considering the maximum output current to decide the inductor current saturation. Once the inductor current saturation it is found automatically is found the inductor value. In our design it is considered a very **low profile** inductor.

$$L = 0.6\mu H$$

The saturation current for this choke is around 25A

6.3 Output capacitor

The output capacitor is chosen by the output voltage static and dynamic accuracy. The static accuracy is related to the output voltage ripple value, while the dynamic accuracy is related to the output current load step.

If the static precision is around ± 2% for the 1.25V output, the output accuracy is ±25mV.

To determine the ESR value from the output precision is necessary before calculate the ripple current:

Eq 20 $$\Delta I = \frac{Vin - Vo}{L} \cdot \frac{Vo}{Vin} \cdot T_{sw}$$

Considering a switching frequency around 270kHz from the equation above the ripple current is around 7A.

So the maximum ESR should be:

Eq 21 $$ESR = \frac{\Delta V_{ripple}}{\frac{\Delta I}{2}} = 7m\Omega$$

The dynamic specifications are sometimes more relaxed than the static requirements so the ESR value around 7mΩ should be enough.

The current ripple flows through the output capacitor, so the output capacitors should be calculated also to sustain this ripple: the RMS current value is given from Eq22.

Eq 22 $$Icout_{rms} = \frac{1}{2\sqrt{3}}\Delta I_L$$

But this is usually a negligible constrain when choosing output capacitor.

To allow the device control loop to work properly output capacitor zero should be at the least ten times smaller than switching frequency. The output capacitor value (C_{OUT}) and the output capacitor ESR (ESR_{OUT}) should be large enough and small enough, to keep the output voltage ripple within the specification and to give to the device a minimum signal to noise ratio.

6.4 Power MOSFETS and Schottky Diodes

Since a 5V bus powers the gate drivers of the device, the use of logic-level MOSFETS is highly recommended, especially for high current applications. The breakdown voltage VBR_{DSS} must be greater than VIN_{MAX} with a certain margin.

The RDS_{ON} can be selected once the allowable power dissipation has been established. By selecting identical Power MOSFET for the main switch and the synchronous rectifier, the total power they dissipate does not depend on the duty cycle. Thus, if P_{ON} is this power loss (few percent of the rated output power), the required RDS_{ON} (@ 25 °C) can be derived from:

Eq 23 $$RDS_{ON} = \frac{P_{ON}}{Iout^2 \cdot (1 + \alpha \cdot \Delta T)}$$

α is the temperature coefficient of RDS_{ON} (typically, $\alpha = 510^{-3}$ °C^{-1} for these low-voltage classes) and ΔT the admitted temperature rise. It is worth noticing, however, that generally the lower RDS_{ON}, the higher is the gate charge Q_G, which leads to a higher gate drive consumption. In fact, each switching cycle, a charge Q_G moves from the input source to ground, resulting in an equivalent drive current:

Eq 24 $$Iq = Qg \cdot F_{SW}$$

For application with low Duty Cycle, where the input voltage is high (around 20V) it is very important to select the high side MOSFET with low gate charge, to reduce the switching losses as STS11NF3LL. For the low side section should be selected a low RDS_{ON} as STS25NH3LL.

A SCHOTTKY diode can be added to increase the system efficiency at high switching frequency (where the dead times could be an important part of total switching period).

This optional diode must be placed in parallel to the synchronous rectifier must have a reverse voltage VRRM greater than VIN_{MAX}. The current size of the diode must be selected in order to keep it in safe operating conditions.

6.5 Output voltage setting

To select the output divider network there isn't a specific criteria, but a low divider network value (around 100Ω) reduces the efficiency at low current; instead a high value divider network (500KΩ) increase the noise effects. A network divider values from 1K to 50K is right. From the Eq4:

R10 = 1KΩ

R9 = 390Ω

The device output voltage is adjustable by connecting a voltage divider from output to VSENSE pin. Minimum output voltage is $V_{OUT} = V_{REF} = 0.9V$. Once output divider and frequency divider have been designed as to obtain the required output voltage and switching frequency, the following equation gives the smallest input voltage, which allows L6995S to regulate (which corresponds to $T_{OFF} = T_{OFF, MIN}$):

Eq 25 $$\delta < 1 - \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{\left(\frac{K_{OSC}}{T_{OFFMIN}}\right)}$$

where the K_{OSC}/T_{OFFMIN} ratio worst-case is given in electrical characteristic table (pag. 4).

6.6 Voltage Feed Forward

Choosing the switching frequency around 270KHz from the Eq1. It can be selected the input divider. For example:

R3=560KΩ

R4=28KΩ

In order to compensate the comparator delay R4 resistor should be increased around 20%.

R4=33KΩ

6.7 Current limit resistor

From the Eq13 can be set the valley current limit, knowing the low side RDS_{ON}. To set the exact current limit it must be considered the temperature effect. So two STS25NH3LL have 2.75mΩ @ 25°C, at 100°C can be considered 3.85mΩ.

R8 = 47KΩ

6.8 Integrator capacitor

Let it be F_U = 15kHz.

Since VREF = 0.9V, from Eq4, it follows $\alpha_{OUT} = 0.72$ and, from Eq5 it follows C_{INT1} = 330pF. Because the ripple is lower than 150mV the system doesn't need the second integrator capacitor.

6.9 Soft start capacitor

Considering the soft start equations (Eq. 11) at page 10, it can be found:

C_{SS} = 200pF

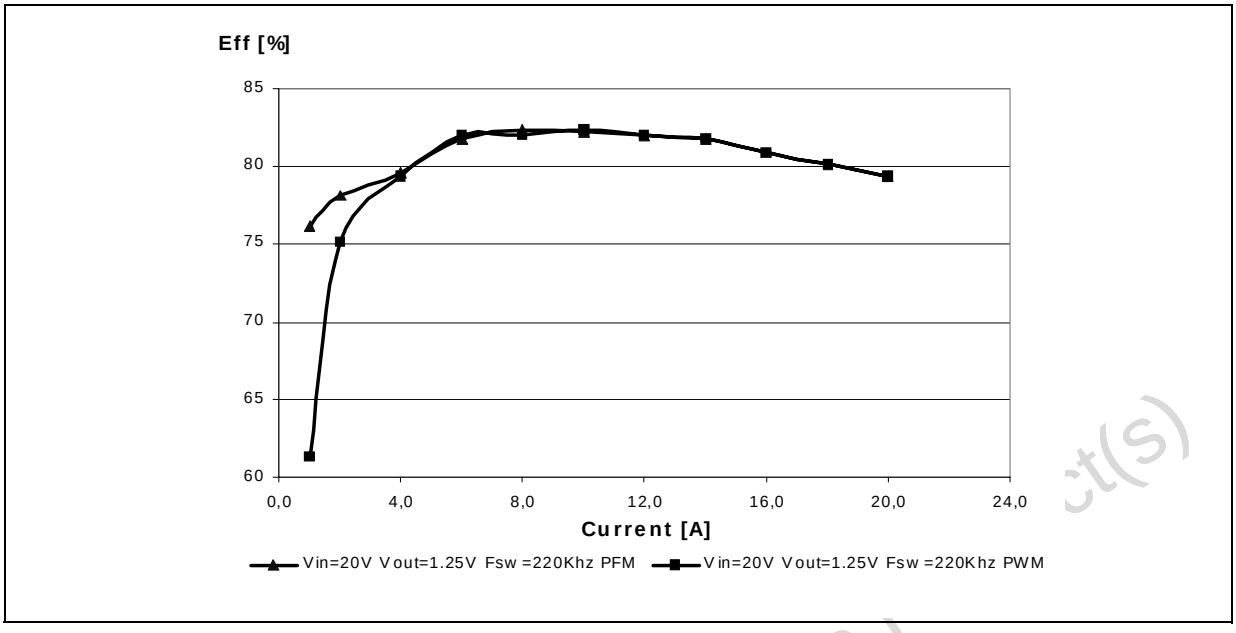
These equations are valid whitout load. When an active load is present the equantions result more complex; further some active loads have unexpected effect, as higher current than the expected one during the start up, that can change the start up time.

In this case the capacitor value can be selected on the application; anyway the Eq11 gives an idea about the C_{SS} value.

6.9.1 Efficiency

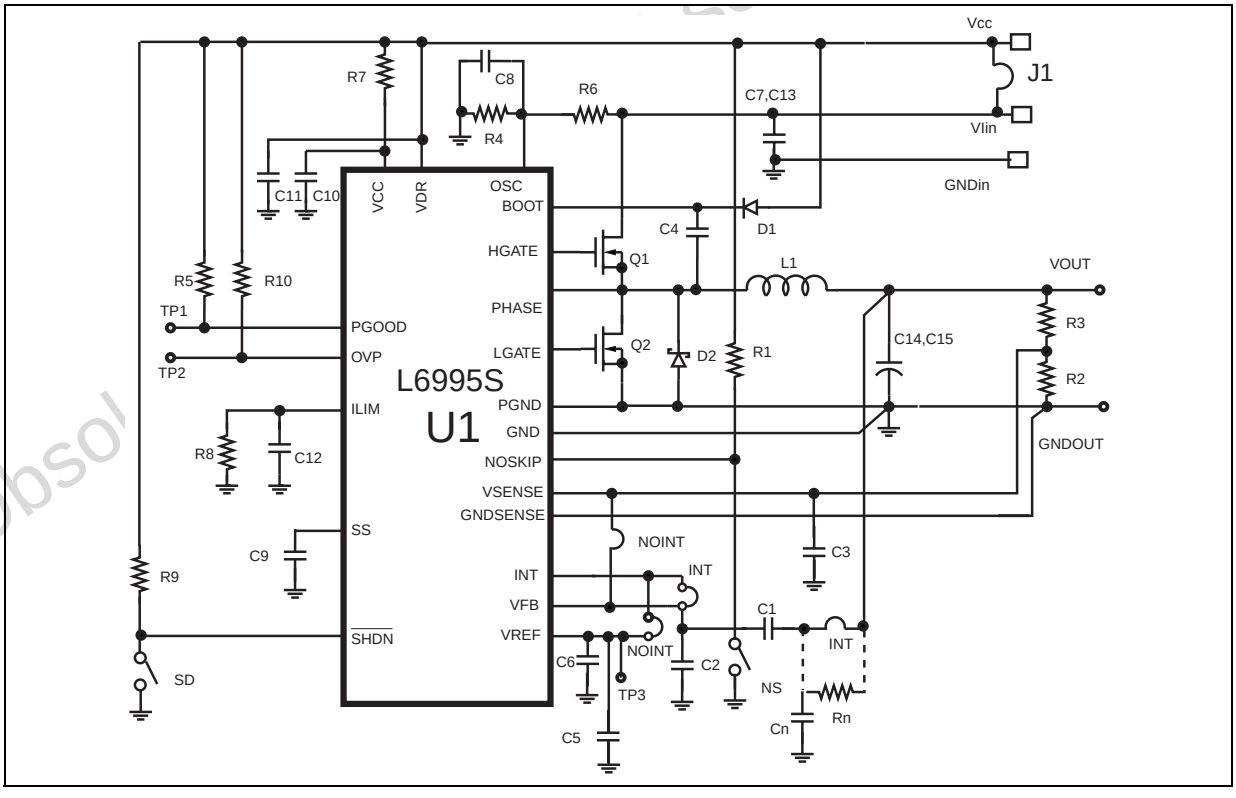
V_{IN} = 20V V_{OUT} = 1.25V F_{SW} = 270KHz

Figure 15. Efficiency vs output current



6.10 5A demo Board

Figure 16. Schematic Diagram



6.11 DEMOBOARD LAYOUT

Real dimensions: 4.7 cm X 2.7 cm (1.85inch X1.063inch)

Figure 17. Top side components placement

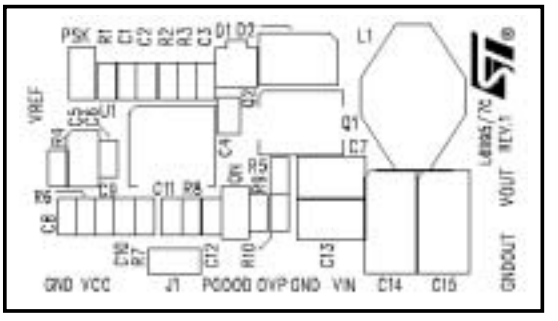


Figure 18. Bottom side Jumpers distribution

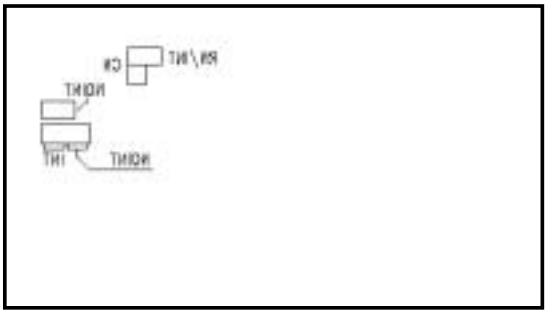


Figure 19. Top side layout

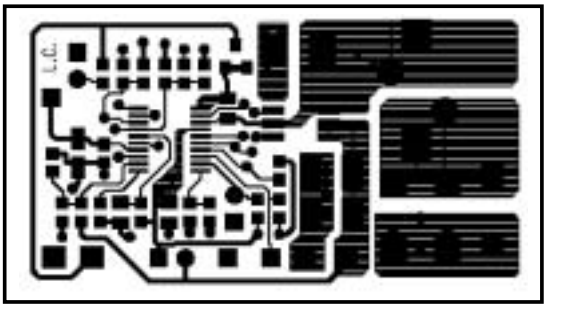


Figure 20. Bottom side layout

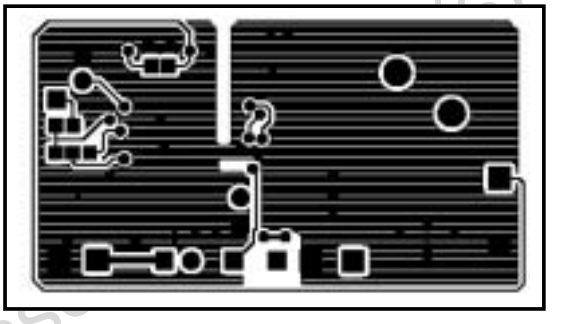


Table 10. Component list

GENERAL-PURPOSE SECTION

Part name	Value	Dimension	Notes
RESISTOR			
R1, R5, R9, R10	33kΩ	0603	Pull-up resistor
R2	10kΩ	0603	Output resistor divider (To set output voltage)
R3	10kΩ	0603	
R4	21kΩ	0603	Input resistor divider (To set switching frequency)
R6	470kΩ	0603	
R7	47Ω	0603	
R8	120kΩ	0603	Current limit resistor
CAPACITOR			
C1	330pF	0603	First integrator capacitor
C2	N.M.	0603	Second integrator capacitor
C3	N.M.	0603	N.M.
C4	100nF	0603	
C5	1µF	Tantalum	
C6	10nF	0603	
C8, C12	47pF	0603	
C9	22nF	0603	Softstart capacitor

Part name	Value	Dimension	Notes
C10	100nF	0603	
C11	100nF	0603	
DIODE			
D1	BAR18		

POWER SECTION

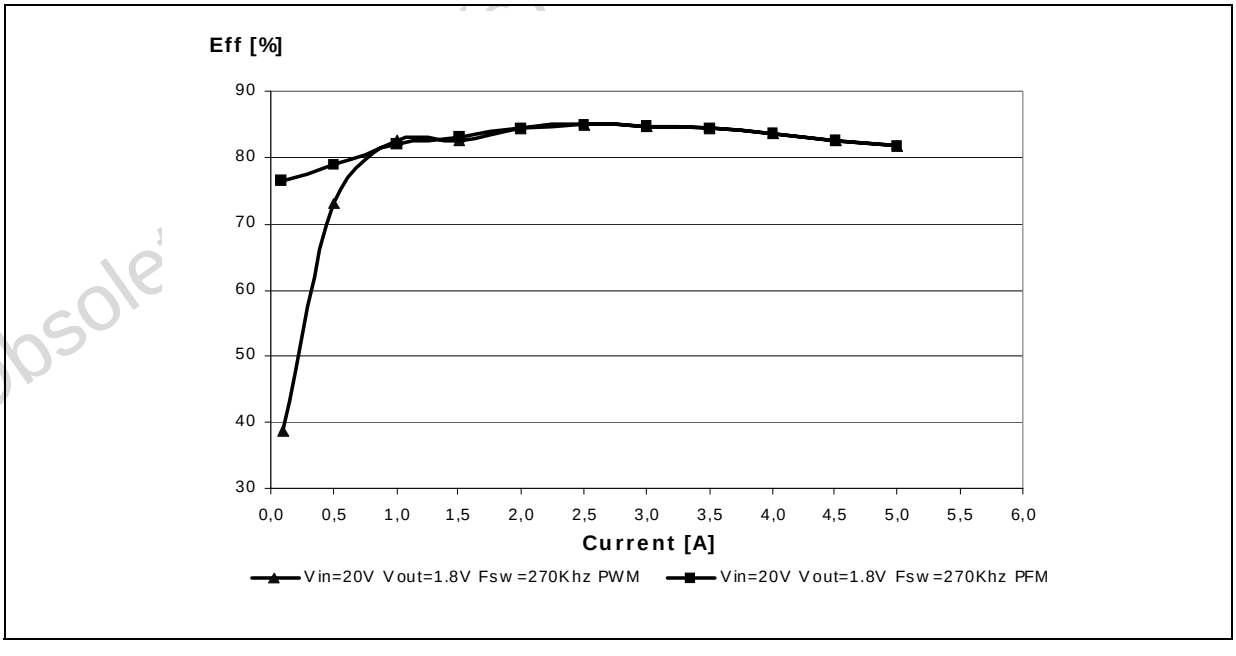
INPUT CAPACITORS			
C7, C13	10µF	C34Y5U1E106ZTE12 TOKIN	
OUTPUT CAPACITORS			
C14, C15	330µF	EEFUE0D331R PANASONIC	
INDUCTOR			
L1	2.7µH	DO3316P-272HC COILCRAFT	
	2.2µH	ETQP6H2R2GF PANASONIC	
	3.3µH	DQ7545 COEV	
POWER MOS			
Q1,Q2	STS8DNF3LL	STMicroelectronics	Dual MOSFETS in single package
DIODE			
D2	STPS3L40U	STMicroelectronics	3

Notes: 1. N.M.=Not Mounted
2. The demoboard with this component list is set to give: V_{OUT} = 1.8V, F_{SW} = 250kHz with an input voltage around V_{IN} = 20V and with the integrator feature.
3. The diode efficiency impact is very low; it is not a necessary component.
4. All capacitors are intended ceramic type otherwise specified.

6.11.1Efficiency

V_{in} = 20V V_{out} = 1.8V F_{sw} = 270kHz

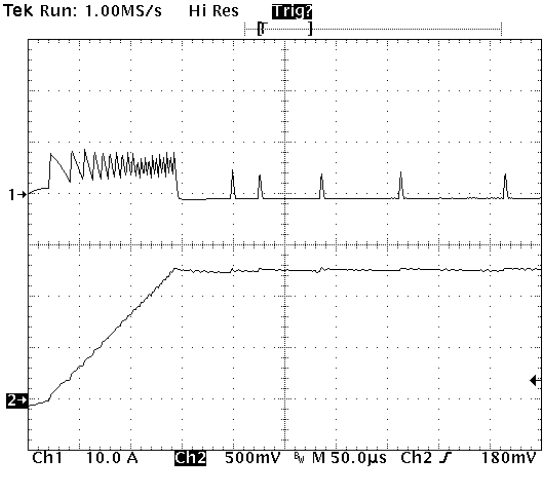
Figure 21. Efficiency vs output current



7 TYPICAL OPERATING WAVEFORMS

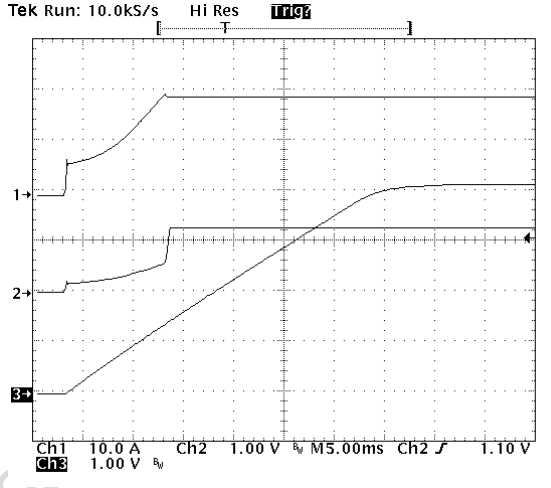
The measurements refer to the part list in table 4. V_{in} = 20V V_{out} = 1.25V F_{sw} = 270kHz T_{amb} = 25°C.

Figure 22. Soft Start with no load.



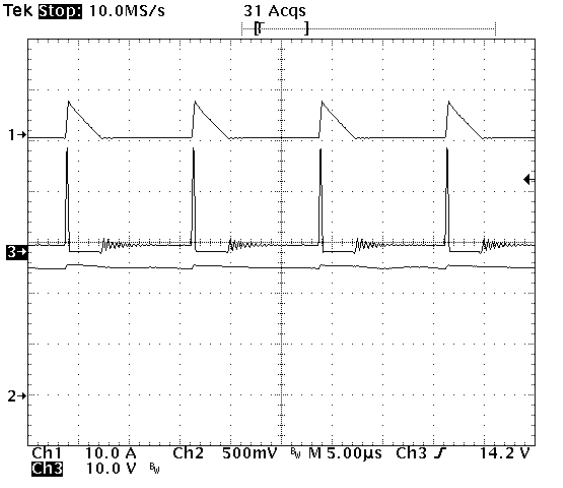
Ch1-> Inductor current
Ch2-> Output voltage

Figure 23. Soft Start with 20A load.



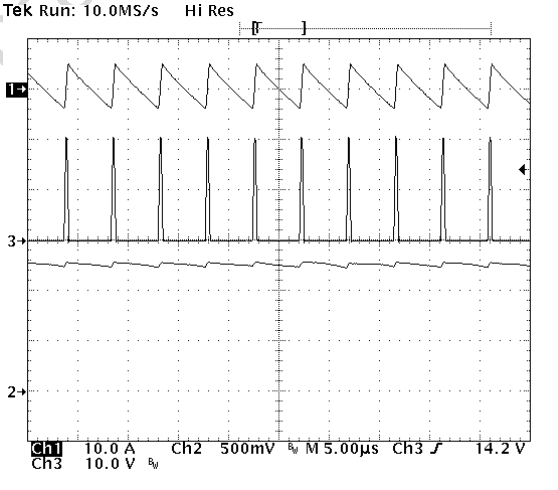
Ch1-> Inductor current
Ch2-> Output voltage
Ch3-> Soft Start voltage

Figure 24. Normal functionality in PSK mode.



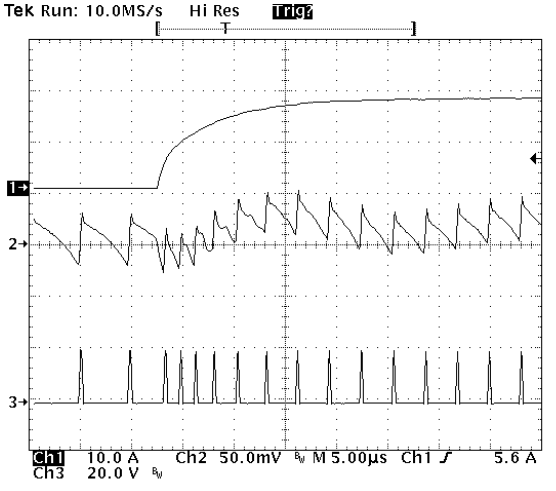
Ch1-> Inductor current
Ch2-> Output voltage
Ch3-> Phase voltage

Figure 25. Normal functionality in PWM mode.



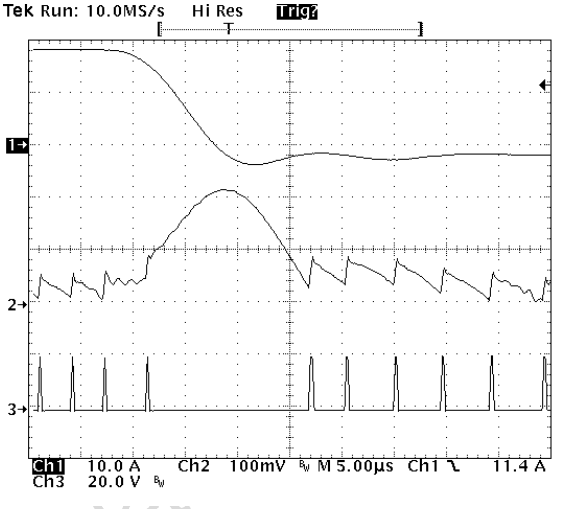
Ch1-> Inductor current
Ch2-> Output voltage
Ch3-> Phase voltage

Figure 26. Load transient from 0 to 18A.



Ch1-> Output current
Ch2-> Output voltage
Ch3->Phase voltage

Figure 27. Load transient from 18A to 0A..



Ch1-> Output current
Ch2-> Output voltage
Ch3->Phase voltage

Figure 28. Switching Frequency Vs Output current

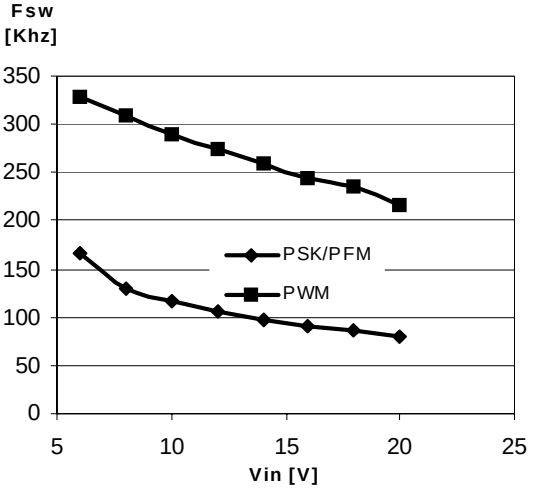


Figure 29. Switching Frequency Vs Input Voltage

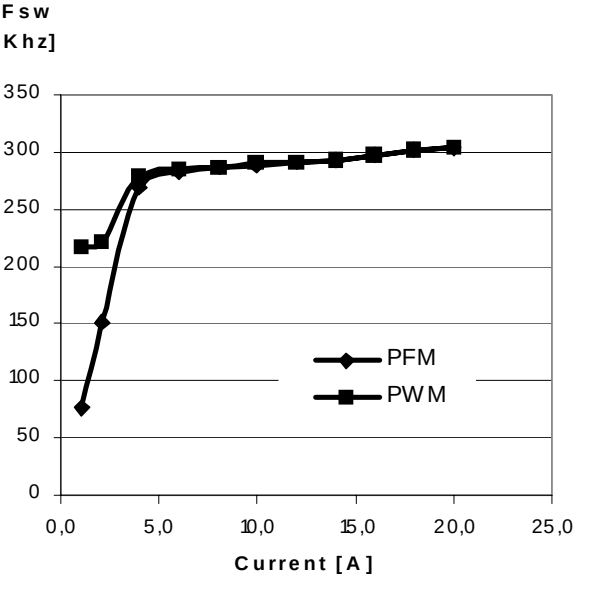
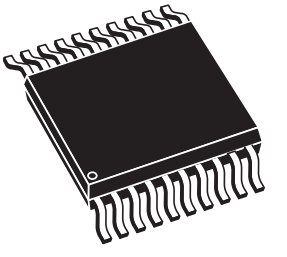


Figure 30. TSSOP20 Mechanical Data & Package Dimensions

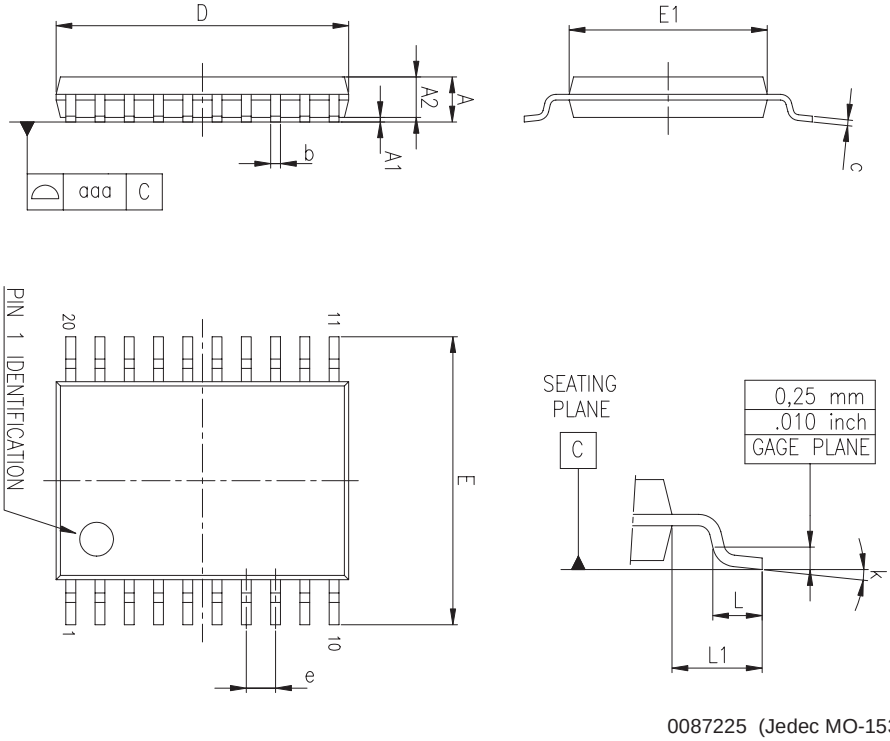
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D (1)	6.400	6.500	6.600	0.252	0.256	0.260
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 (1)	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° (min.) 8° (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

OUTLINE AND MECHANICAL DATA



TSSOP20
Thin Shrink Small Outline Package



0087225 (Jedec MO-153-AC)

Table 11. Revision History

Date	Revision	Description of Changes
April 2004	1	First Issue