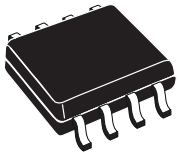
STS8C5H30L

N-channel 30 V, 0.018 Ω, 8 A, P-channel 30 V, 0.045 Ω, 5 A SO-8 low gate charge STripFET™ III MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STS8C5H30L(N-channel)	30 V	< 0.022 Ω	8 A
STS8C5H30L(P-channel)	30 V	< 0.055 Ω	5 A

- Conduction losses reduced
- Switching losses reduced
- Low threshold drive
- Standard outline for easy automated surface mount assembly



SO-8

Application

- Switching applications

Description

The STS8C5H30L is a Power MOSFET realized with the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

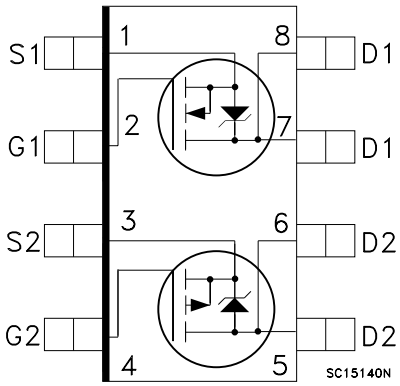


Table 1. Device summary

Part number	Marking	Package	Packaging
STS8C5H30L	S8C5H30L	SO-8	Tape and reel

Note: For the p-channel MOSFET actual polarity of voltages and current has to be reversed

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		N-channel	P-channel	
V_{DS}	Drain-source voltage (v_{gs} = 0)	30		V
V_{GS}	Gate- source voltage	±16	±16	V
I_D	Drain current (continuos) at T_C = 25°C single operating	8	5.4	A
I_D	Drain current (continuos) at T_C = 100°C single operating	6.4	4.3	A
I_{DM} (1)	Drain current (pulsed)	32	21.6	A
P_{TOT}	Total dissipation at T_C = 25°C dual operating Total dissipation at T_C = 25°C single operating	1.6 2		W W
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Operating junction temperature	150		°C

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}a}$ (1)	Thermal resistance junction-ambient single operating	62.5	°C/W
$R_{thj\text{-}a}$ (1)	Thermal resistance junction-ambient dual operating	78	°C/W

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., t ≤ 10 sec

Note: For the p-channel MOSFET actual polarity of voltages and current has to be reversed

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	n-ch p-ch	30 30			V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS}=Max rating, T_C=125 °C	n-ch p-ch			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±16 V V_{GS} = ±16 V	n-ch p-ch			±100 ±100	nA nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	n-ch p-ch	1 1	1.6 1.6	2.5 2.5	V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 4 A V_{GS} = 10 V, I_D = 2.5 A V_{GS} = 4.5 V, I_D = 4 A V_{GS} = 4.5 V, I_D = 2.5 A	n-ch p-ch n-ch p-ch		0.018 0.045 0.020 0.070	0.022 0.055 0.025 0.075	Ω Ω Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D= 4 A V_{DS} = 15 V, I_D= 2.5 A	n-ch p-ch		8.5 10		S S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	n-ch p-ch		857 1350		pF pF
C_{oss}	Output capacitance		n-ch p-ch		147 490		pF pF
C_{rss}	Reverse transfer capacitance		n-ch p-ch		20 130		pF pF
Q_g	Total gate charge	**N-channel** V_{DD}=24 V I_D=8 A V_{GS}=5 V **P-channel** V_{DD} = 24 V I_D = 4 A V_{GS}= 5 V *(see Figure 27)*	n-ch p-ch		7 12.5	10 16	nC nC
Q_{gs}	Gate-source charge		n-ch p-ch		2.5 5		nC nC
Q_{gd}	Gate-drain charge		n-ch p-ch		2.3 3		nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5.

For the p-channel MOSFET actual polarity of voltages and current has to be reversed

Table 6. Switching times

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	**N-channel** V_{DD} = 15 V, I_D = 4 A R_G=4.7 Ω, V_{GS} = 4.5 V **P-channel** V_{DD} = 15 V, I_D = 2 A R_G=4.7 Ω, V_{GS} = 4.5 V *Figure 26*	n-ch p-ch		12 25		ns ns
t_r	Rise time		n-ch p-ch		14.5 35		ns ns
$t_{d(off)}$	Turn-off delay time		n-ch p-ch		23 125		ns ns
t_f	Fall time		n-ch p-ch		8 35		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		n-ch p-ch			8 5	A A
I_{SDM} (1)	Source-drain current (pulsed)		n-ch p-ch			32 20	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0 I_{SD} = 5 A, V_{GS} = 0	n-ch p-ch			1.5 1.2	V V
t_{rr}	Reverse recovery time	**N-channel** I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}=15 V,T_j =150 °C **P-channel** I_{SD} = 5 A, di/dt = 100 A/µs V_{DD}=15 V, T_j =150 °C *Figure 28*	n-ch p-ch		15 45		ns ns
Q_{rr}	Reverse recovery charge		n-ch p-ch		5.7 36		nC nC
I_{RRM}	Reverse recovery current		n-ch p-ch		0.76 1.6		A A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Note: For the p-channel MOSFET actual polarity of voltages and current has to be reversed

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area n-ch

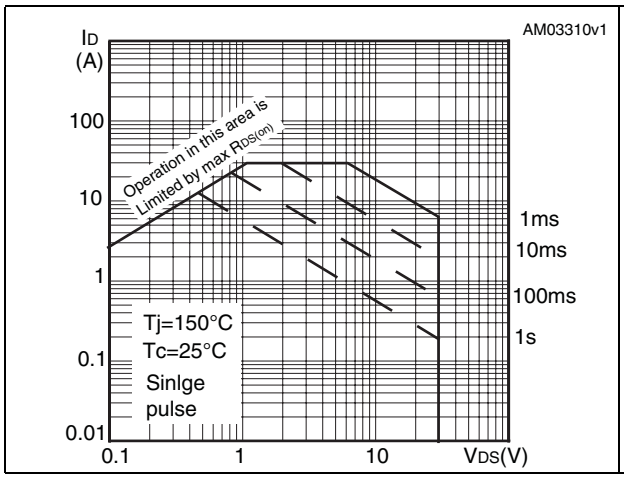


Figure 3. Thermal impedance n-ch

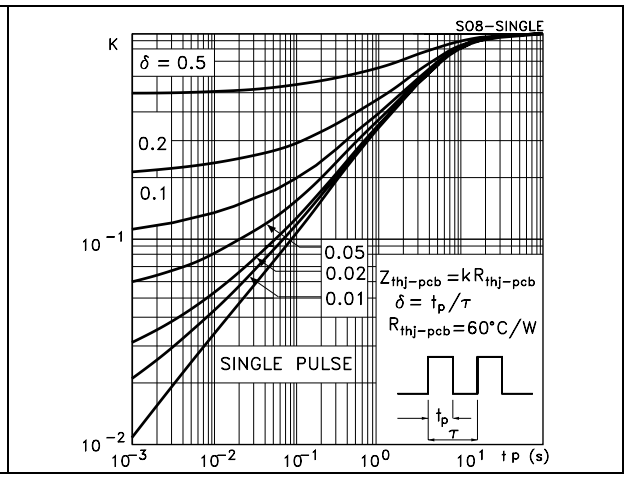


Figure 4. Output characteristics n-ch

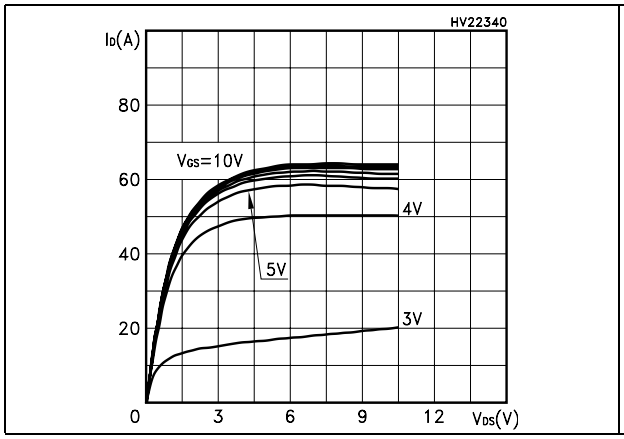


Figure 5. Transfer characteristics n-ch

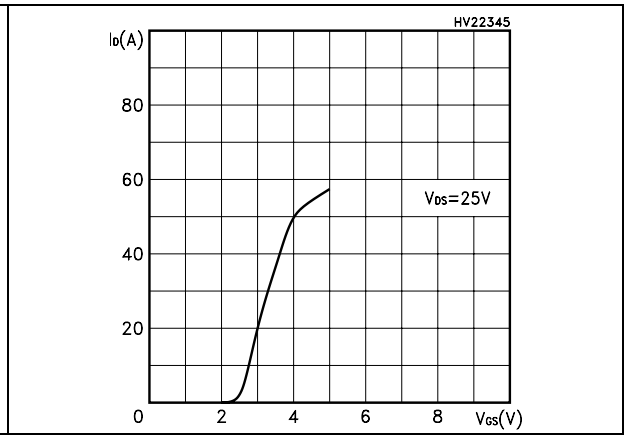


Figure 6. Transconductance n-ch

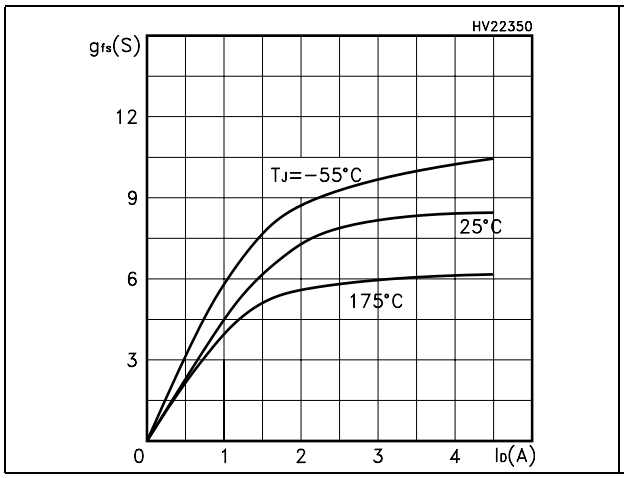


Figure 7. Static drain-source on resistance n-ch

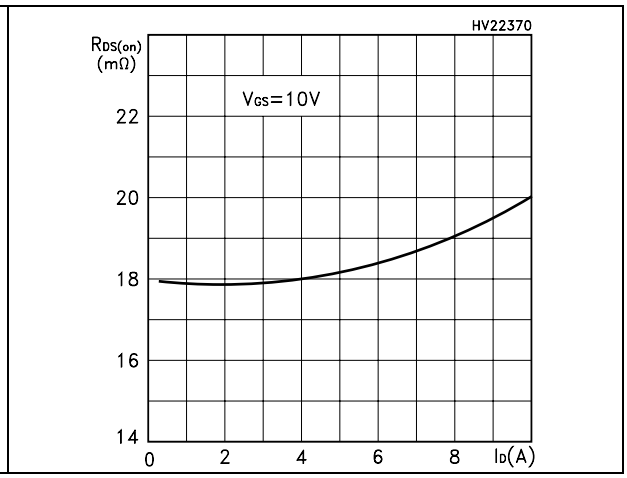


Figure 8. Gate charge vs. gate-source voltage n-ch

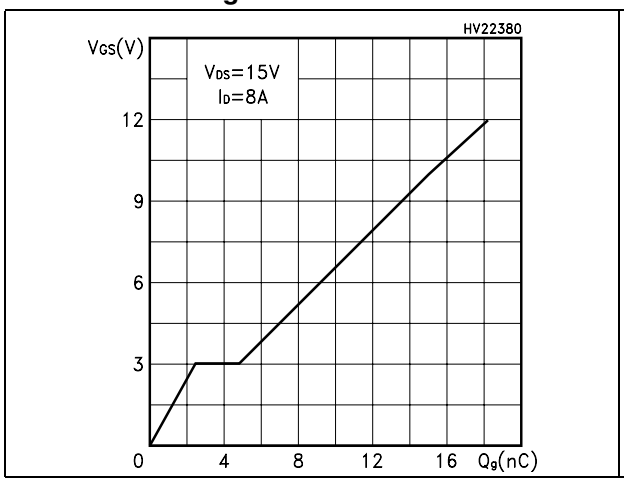


Figure 9. Capacitance variations n-ch

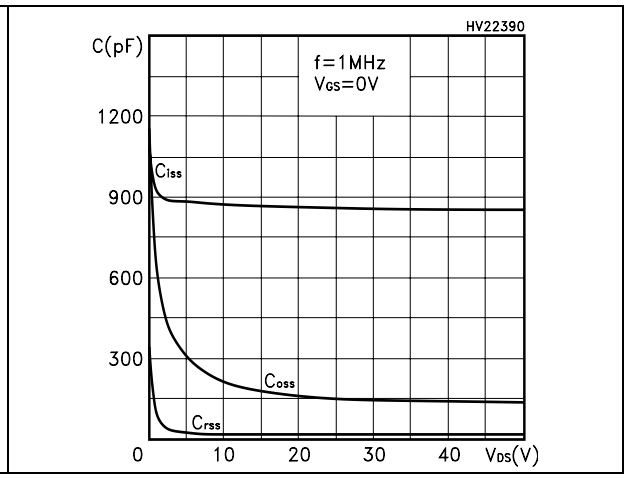


Figure 10. Normalized gate threshold voltage vs. temperature n-ch

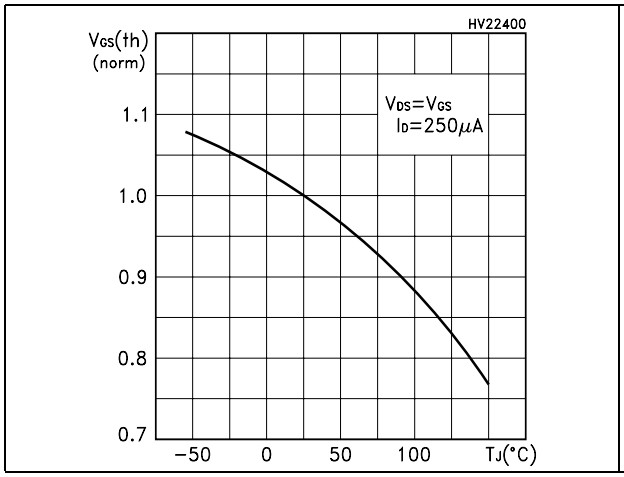


Figure 11. Normalized on resistance vs. temperature n-ch

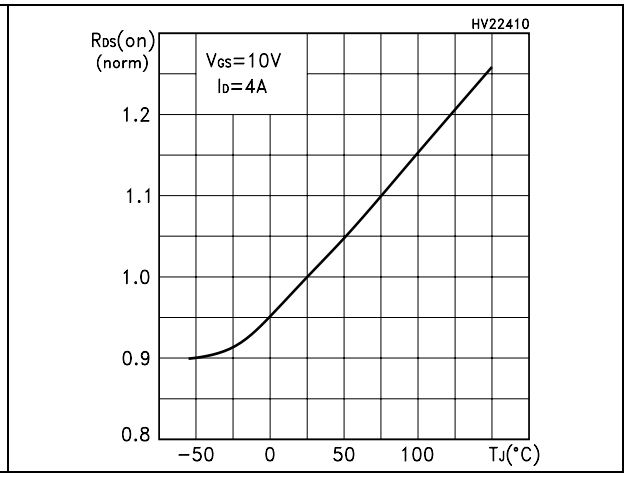


Figure 12. Source-drain diode forward characteristics n-ch

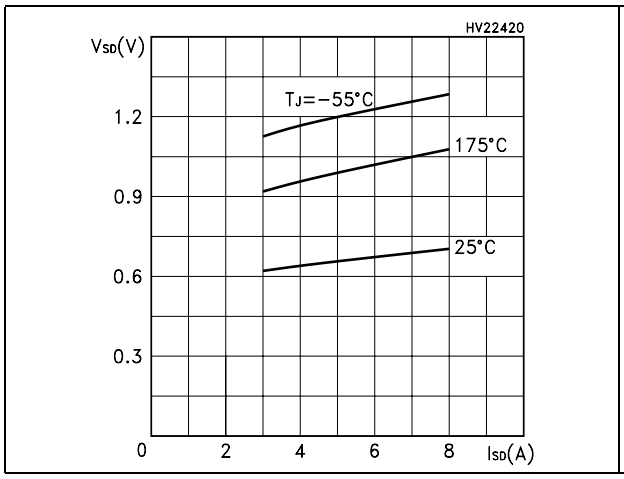


Figure 13. Normalized breakdown voltage vs. temperature n-ch

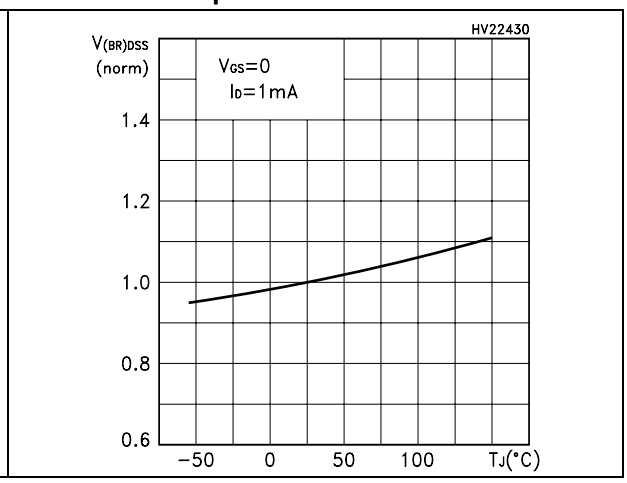


Figure 14. Safe operating area p-ch

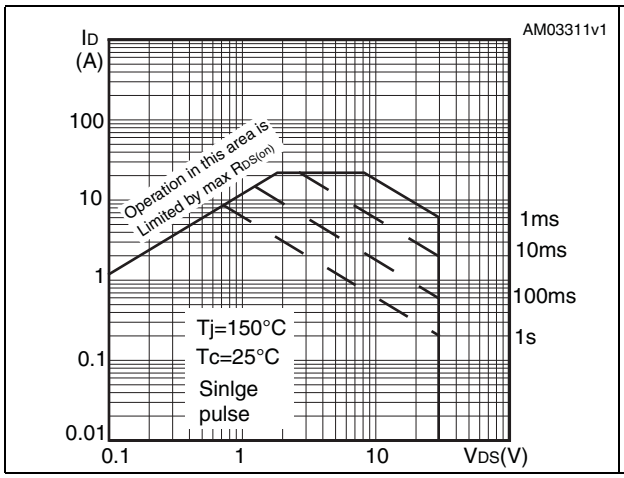


Figure 15. Thermal impedance p-ch

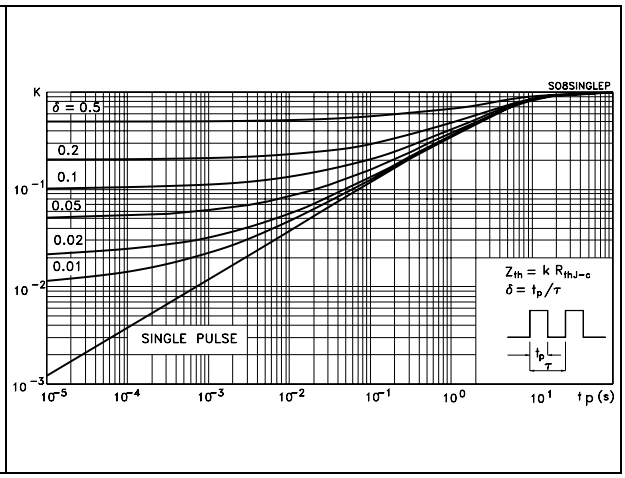


Figure 16. Output characteristics p-ch

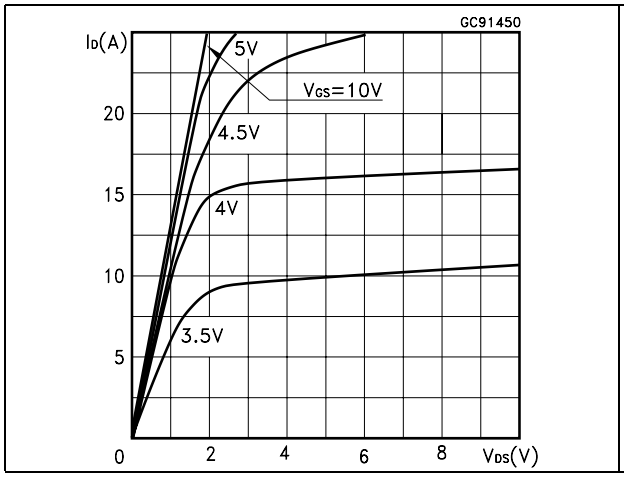


Figure 17. Transfer characteristics p-ch

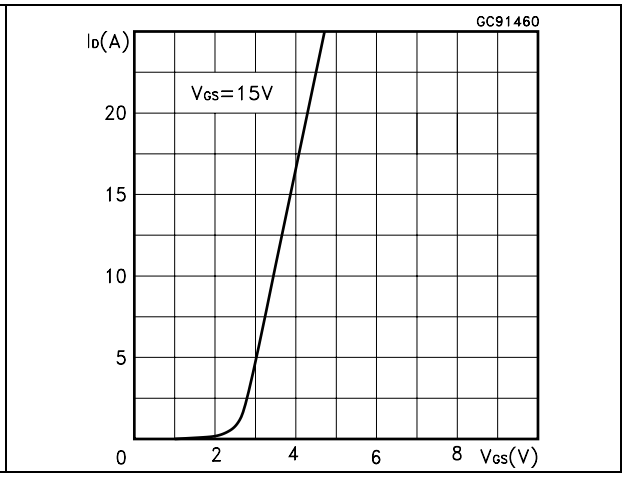


Figure 18. Transconductance p-ch

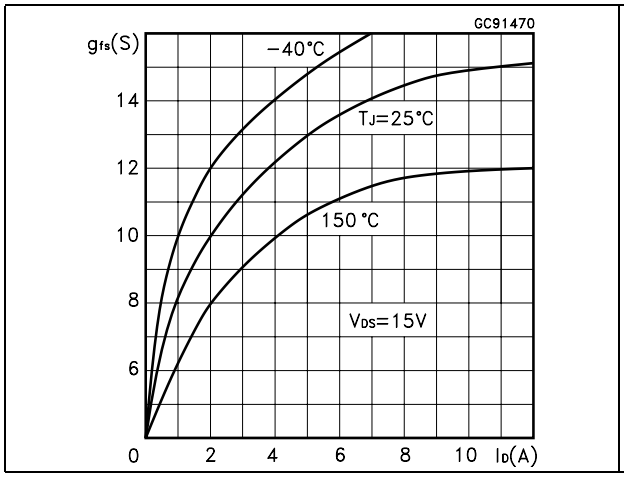


Figure 19. Static drain-source on resistance p-ch

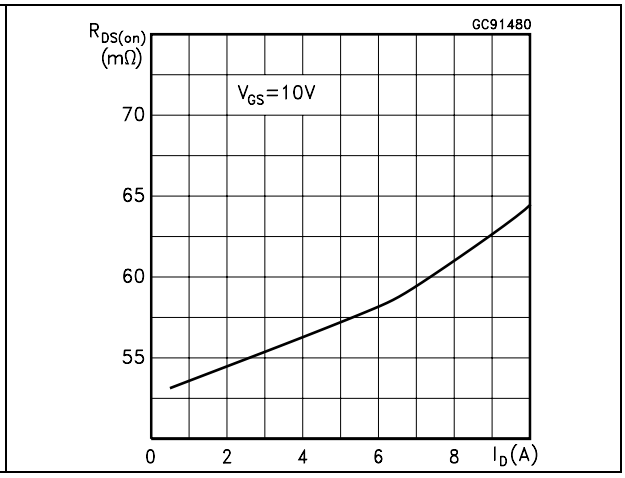


Figure 20. Gate charge vs. gate-source voltage p-ch

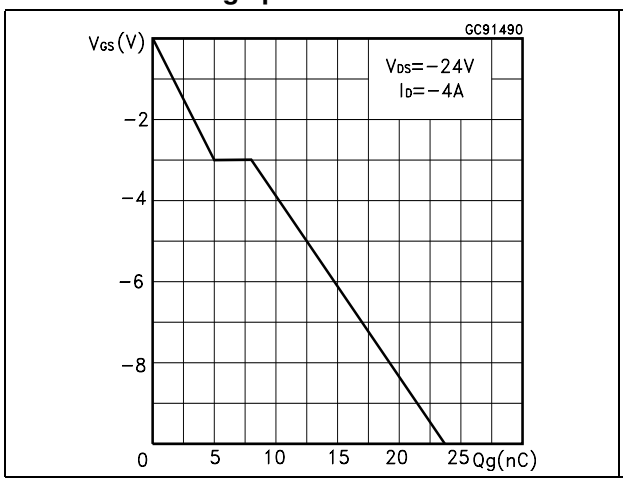


Figure 21. Capacitance variations p-ch

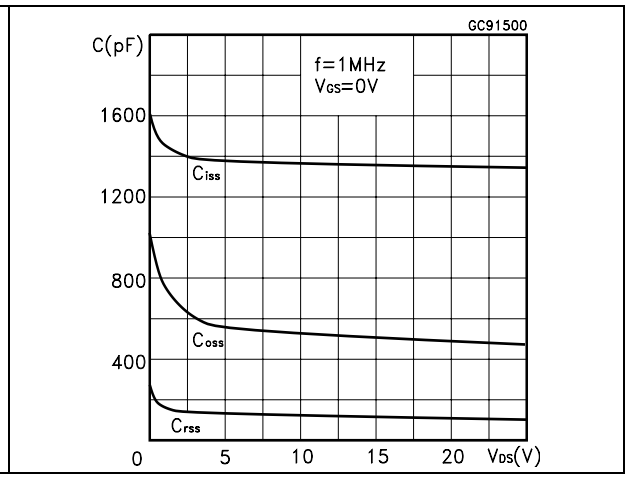


Figure 22. Normalized gate threshold voltage vs. temperature p-ch

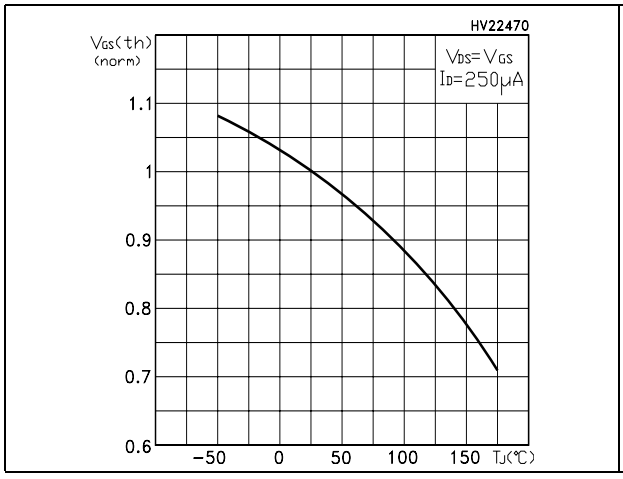


Figure 23. Normalized on resistance vs. temperature p-ch

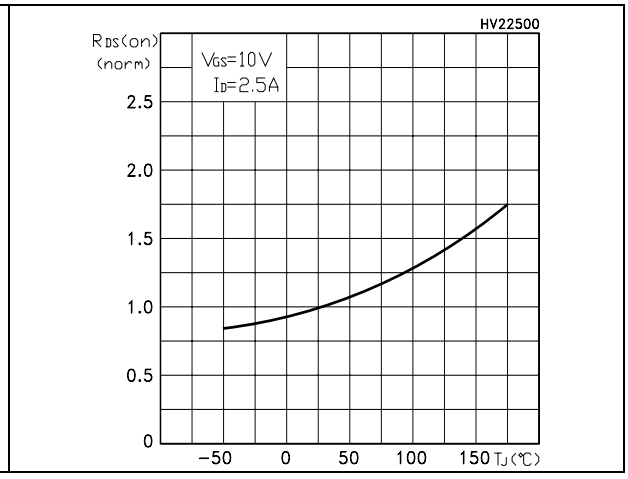


Figure 24. Source-drain diode forward characteristics p-ch

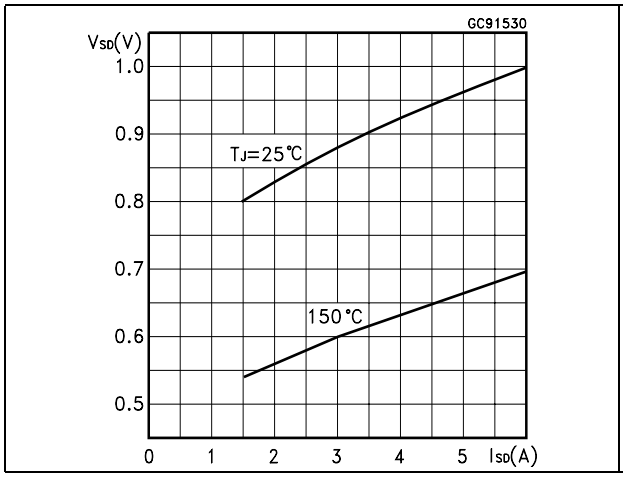
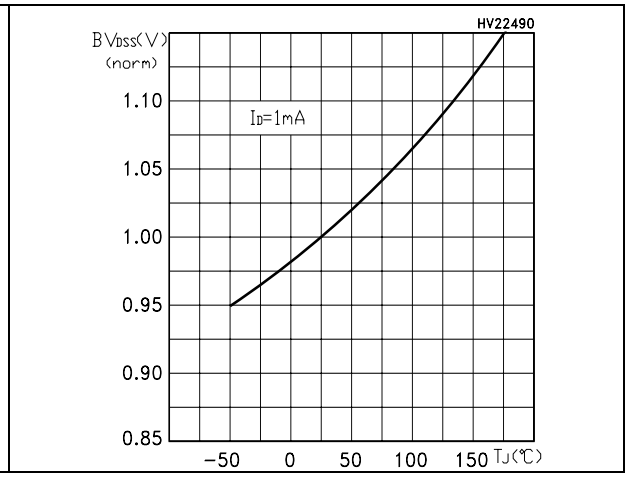


Figure 25. Normalized breakdown voltage vs. temperature p-ch



3 Test circuits

Figure 26. Switching times test circuit for resistive load

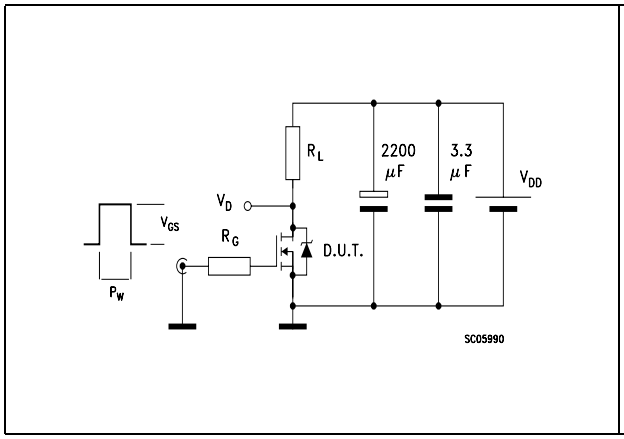


Figure 27. Gate charge test circuit

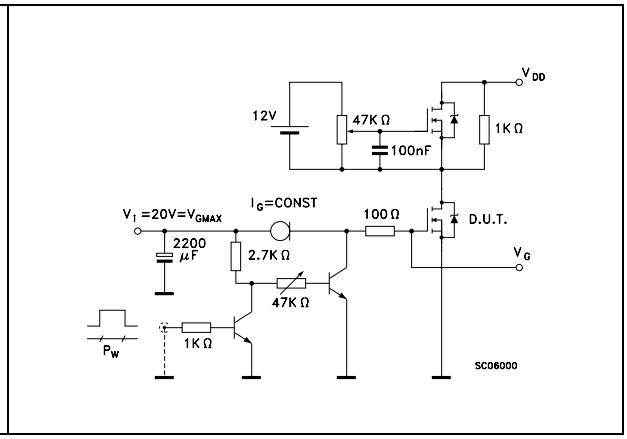


Figure 28. Test circuit for inductive load switching and diode recovery times

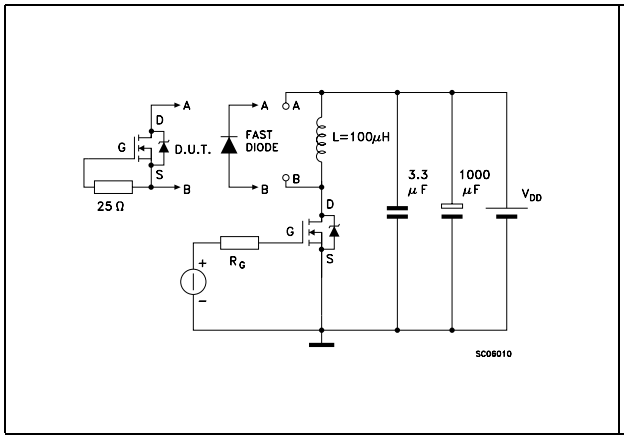


Figure 29. Unclamped inductive load test circuit

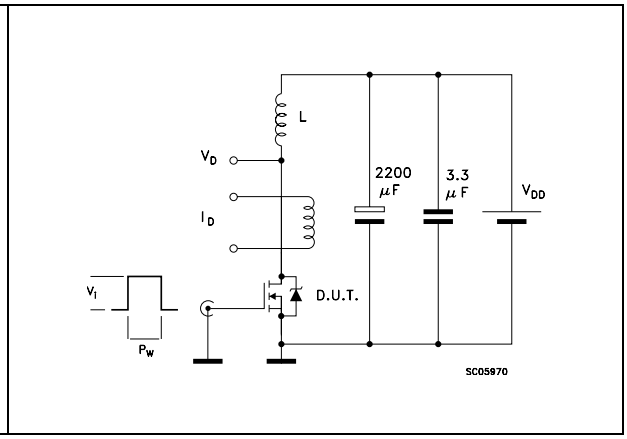


Figure 30. Unclamped inductive waveform

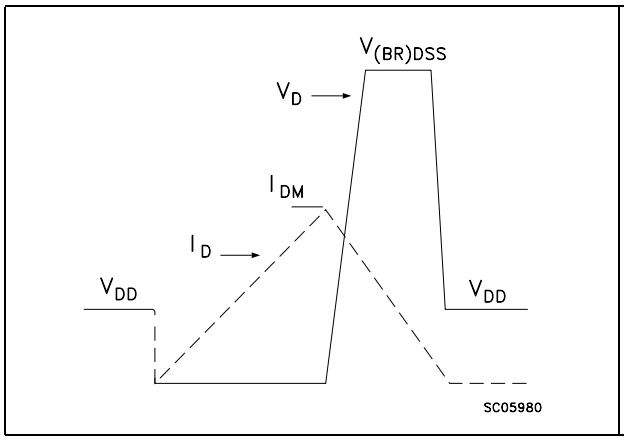
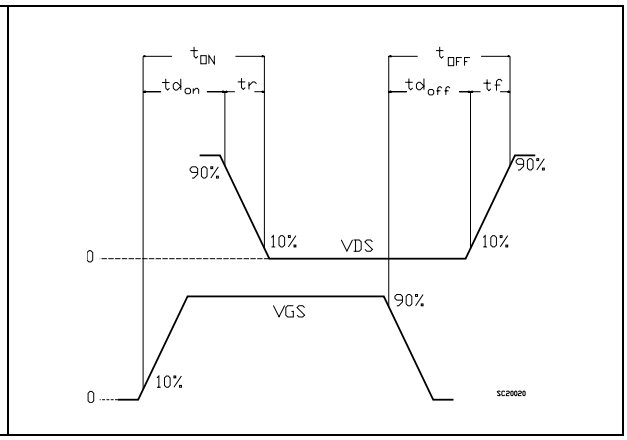


Figure 31. Switching time waveform

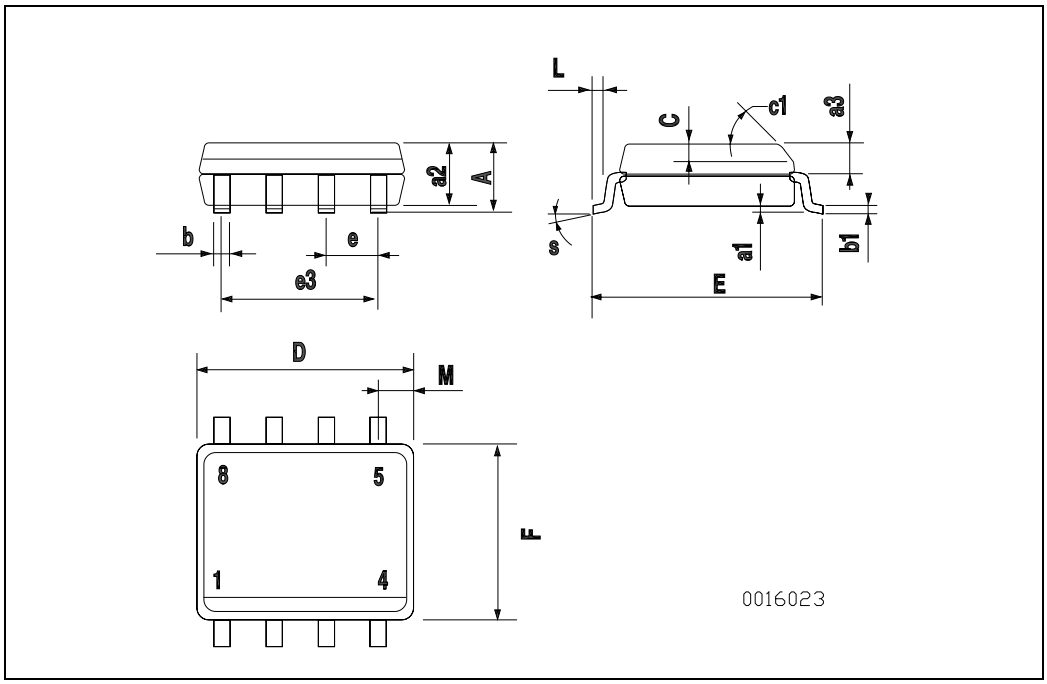


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Revision history

Date	Revision	Changes
17-Sep-2004	1	First revision.
31-Oct-2006	2	The document has been reformatted.
30-Jan-2007	3	typo mistake on *Table 2*.
23-Jul-2007	4	*Figure 14* has been updated.
23-Feb-2009	5	*Figure 2*, *Figure 3*, *Figure 14* and *Figure 15* have been changed.
10-Jun-2010	6	Updated $V_{GS(th)}$ in *Table 4: On/off states*.

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