STLQ50xx

50 mA, 3 µA supply current low drop linear regulator

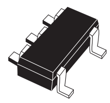
Datasheet — production data

Features

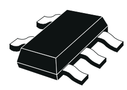
- 2.3 V to 12 V input voltage range
- 50 mA maximum output current
- 3 µA quiescent current
- Available in 1.8 V, 2.5 V, 3.3 V, 5.0 V and adjustable voltage
- 200 mV dropout voltage at 25 mA output current
- Internal thermal protection
- Available in SOT323-5L package, and SOT23-5L package (upon request)

Applications

- Portable/battery-powered equipment
- Electronic sensors
- Microcontroller power
- Real-time clock backup power



SOT323-5L



SOT23-5L
(available on request)

Description

The STLQ50xx is a BiCMOS linear regulator specifically designed for operating in environments where very low power consumption is required.

Its very low quiescent current (3 µA) results in extended battery life, making the device suitable for applications which have very long standby time.

The PMOS pass element allows very good dropout values (200 mV at 25 mA I_O and 350 mV at full load) without affecting the consumption characteristics.

Housed in the very small SOT323-5L or SOT23-5L, it meets space-saving requirements in battery-powered equipment.

Table 1. Device summary

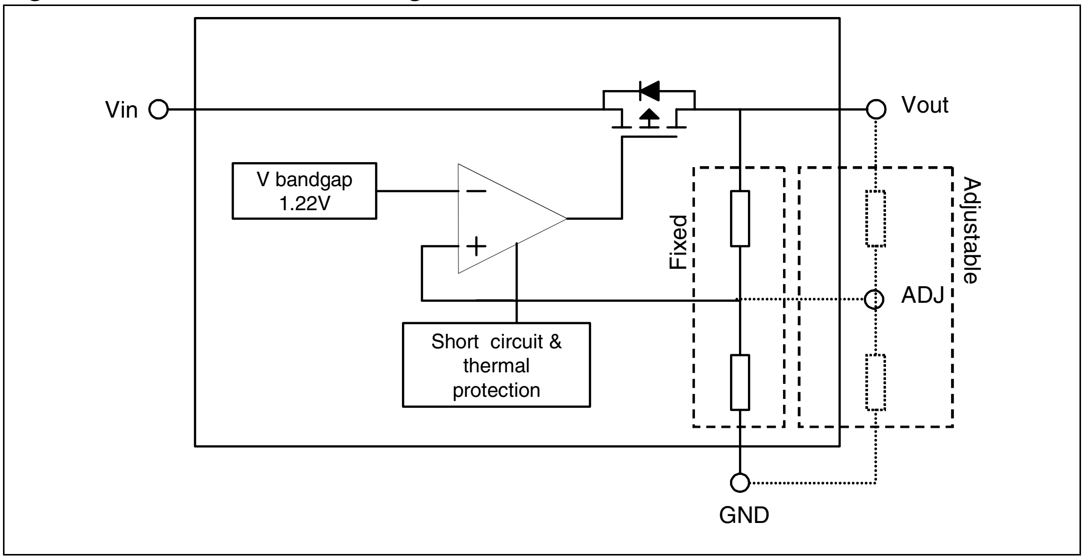
Part number	Order codes		Output voltage
	SOT323-5L (T&R)	SOT23-5L (T&R) (1)	
STLQ50XX18	STLQ50C18R	STLQ50M18R	Fixed V_O = 1.8 V
STLQ50XX25	STLQ50C25R	STLQ50M25R	Fixed V_O = 2.5 V
STLQ50XX33	STLQ50C33R	STLQ50M33R	Fixed V_O = 3.3 V
STLQ50XX50	STLQ50C50R	STLQ50M50R	Fixed V_O = 5.0 V
STLQ50	STLQ50C-R	STLQ50M-R	Adjustable

1. Available upon request.

Contents

1 Block diagram

Figure 1. STLQ50xx block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

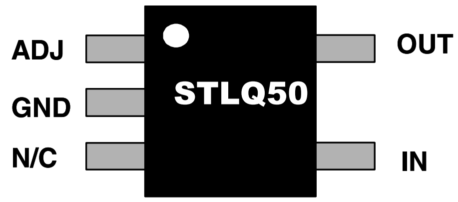


Table 2. Pin description

Pin n°	Symbol	Note
1	ADJ	STLQ50: output voltage adjust
	N/C	STLQ50xx: not connected
2	GND	Ground
3	N/C	Not connected
4	IN	Input voltage
5	OUT	Output voltage

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC Input voltage	-0.3 to +14	V
V_{FB}	FB voltage	-0.3 to +7	V
ESD	Human body model (all pins)	±2	kV
T_J	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	SOT323-5L	SOT23-5L	Unit
R_{thJA}	Thermal resistance junction-ambient	331.4 (1)	191 (1)	°C/W

1. This value is referred to a 4-layer PCB, JEDEC standard test board.

4 Electrical characteristics

$V_I = V_{O(NOM)}$ +1 V or V_I = 2.5 V if V_O < 1.5 V; T_A= -40 °C to 125 °C; I_O = 1 mA; typical values are at T_A = 25 °C, C_O = 1 µF unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Input voltage range	I_O = 20 mA	2.3		12	V
		I_O = 50 mA	2.5		12	
I_Q	Quiescent current (measured on ground pin, fixed version)	V_I = 5 V		3.5	5.0	µA
		V_I = 12 V		4.1	6.0	
V_O	Output voltage range (STLQ50ADJ)		1.222		11	V
	Accuracy as percentage of nominal voltage at T_J = 25 °C		-2		+2	%
$V_{DROP-MAX}$	Max dropout voltage [1]	I_O = 50 mA;		0.4	0.7	V
ΔV_O	Load regulation	1 mA < I_O < 50 mA			0.15	%/mA
ΔV_O	Line regulation	V_O = 1.5 V: V_O + 1 V < V_I < 12 V; V_O < 1.5 V: 2.5 V < V_I < 12 V;			0.3	%/V
SVR	Supply voltage rejection	V_{RIPPLE} = 0.1 V, I_O = 20 mA, f = 120 Hz		30		dB
eN	Output noise voltage	B_W from 200 Hz to 100 kHZ; I_O = 10 mA		560		μV_{RMS}
T_h	Thermal protection			160		°C
I_{OMAX}	Maximum output current [2]	V_O = 0 V		500		mA

1. V_I = 2.5 V when $V_{O(NOM)} \leq 2.1$ V
2. The maximum power dissipation must not be exceeded, see application information for details.

5 Typical application

Figure 3. Fixed versions: STLQ5018- STLQ5025- STLQ5033- STLQ5050

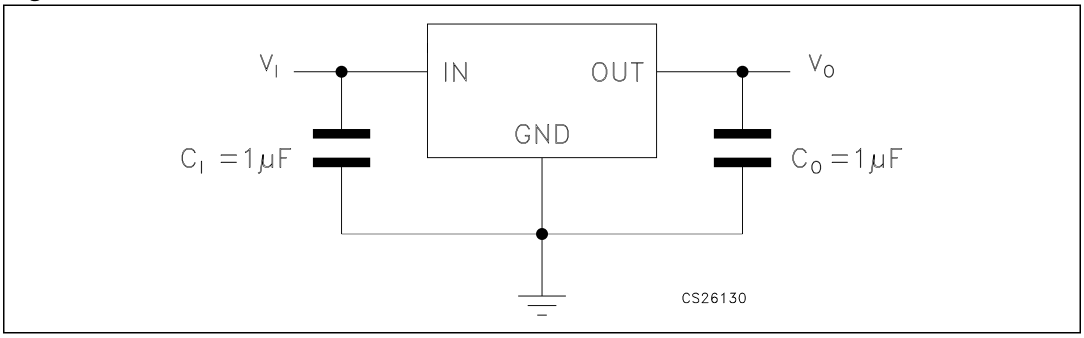
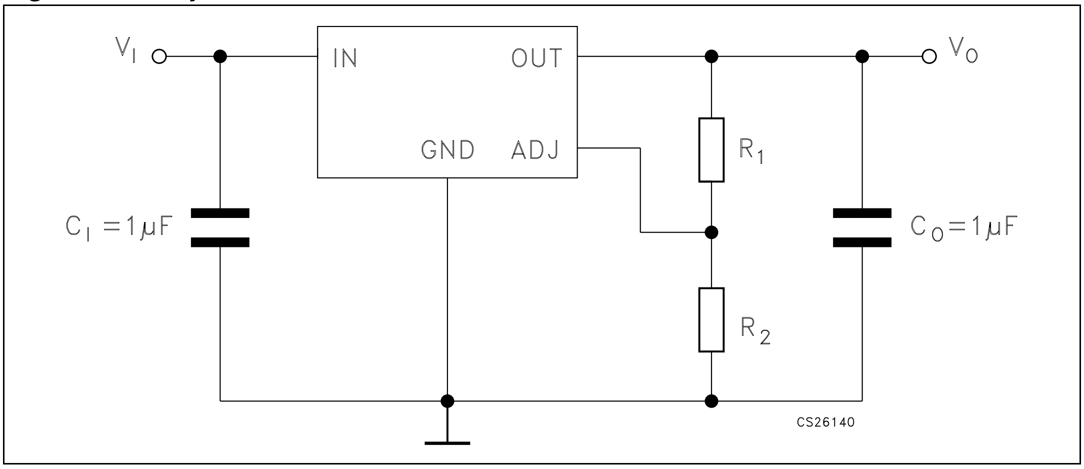


Figure 4. Adjustable version STLQ50ADJ



6 Typical characteristics

Figure 5. V_O vs. T_J

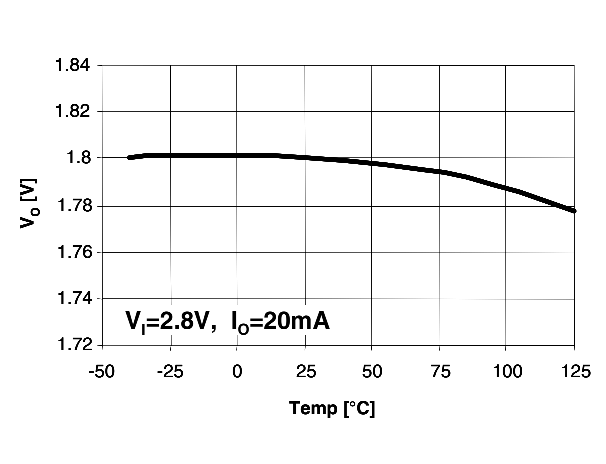


Figure 6. V_O vs. V_I

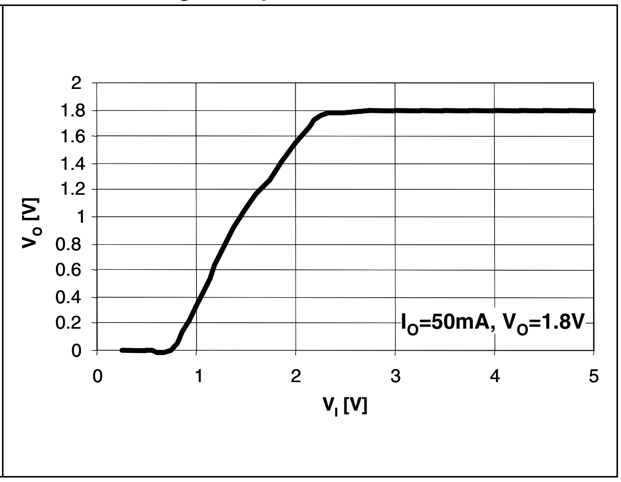


Figure 7. I_Q vs. T_J

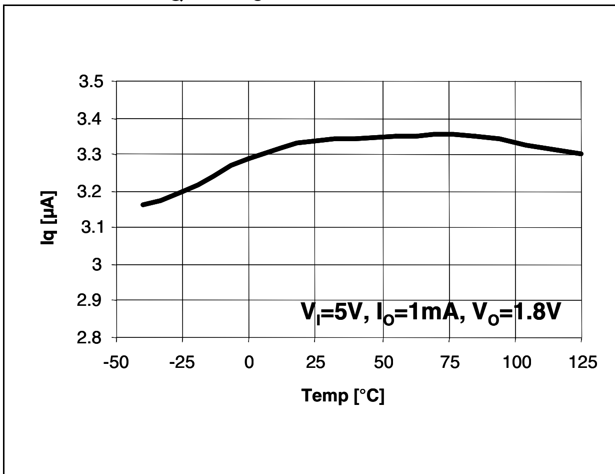


Figure 8. V_{DROP} vs. I_O

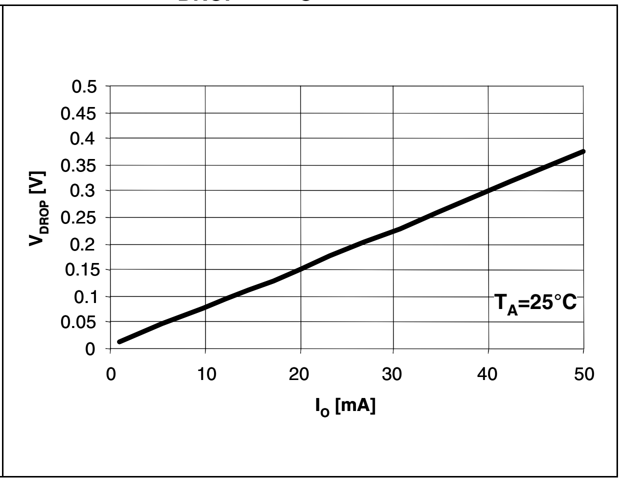


Figure 9. V_{DROP} vs. T_J

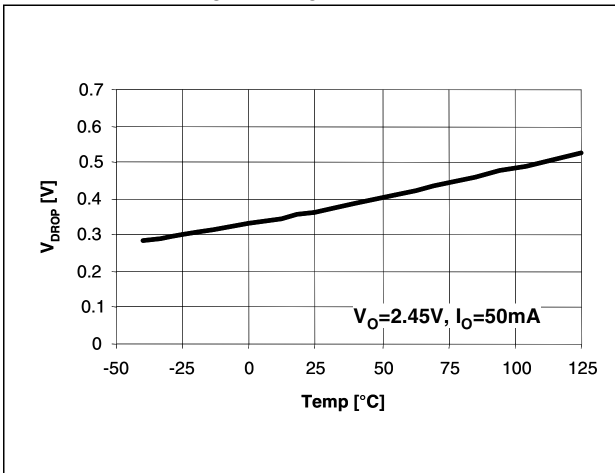


Figure 10. Stability

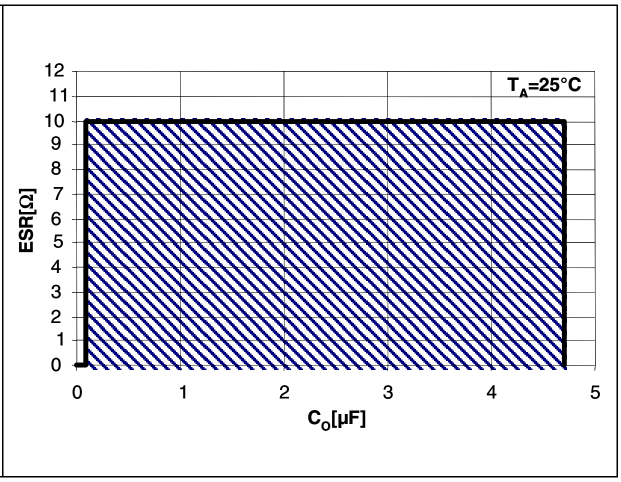


Figure 11. S.V.R. vs. Freq.

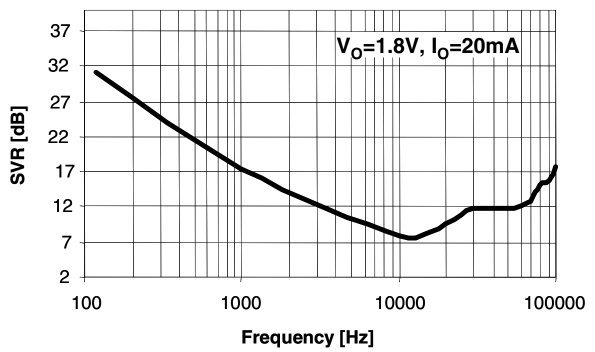


Figure 12. S.V.R. vs. I_O

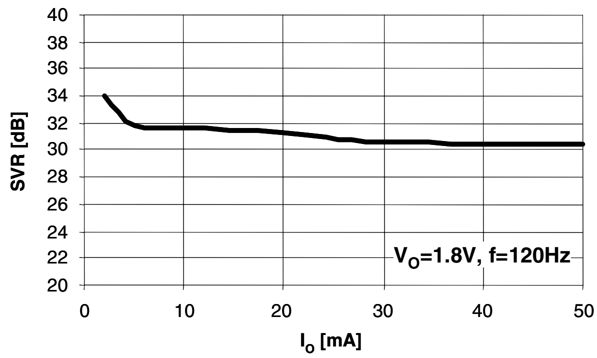
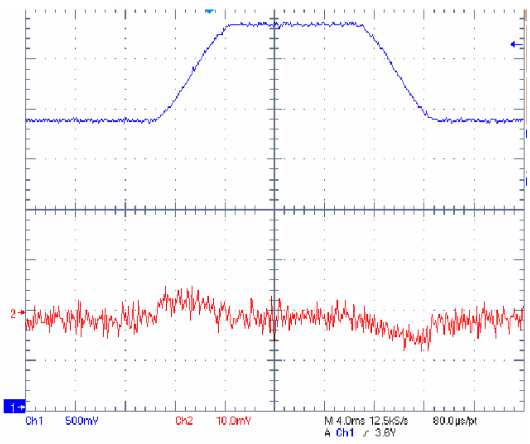
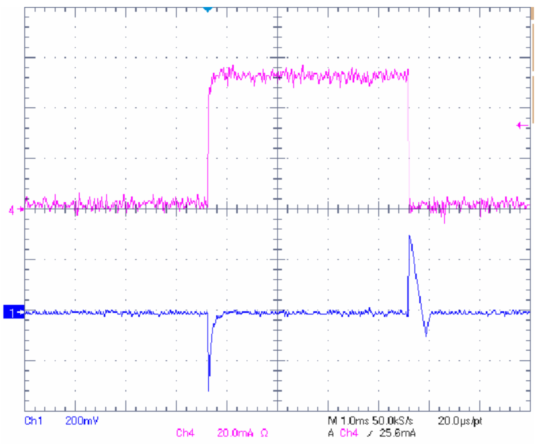


Figure 13. Line transient response



I_O=50mA; C_O=10µF; V_I=2.8V, V_I rise/fall=5ms

Figure 14. Load transient response



C_O=1µF; V_O=1.8V; V_I=2.8V, Curr. rise/fall=1µs

Figure 15. Short-circuit current

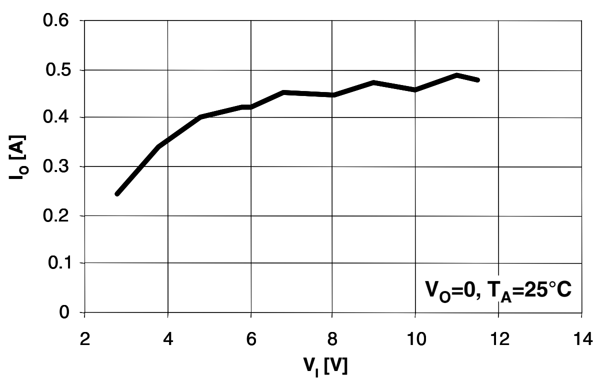
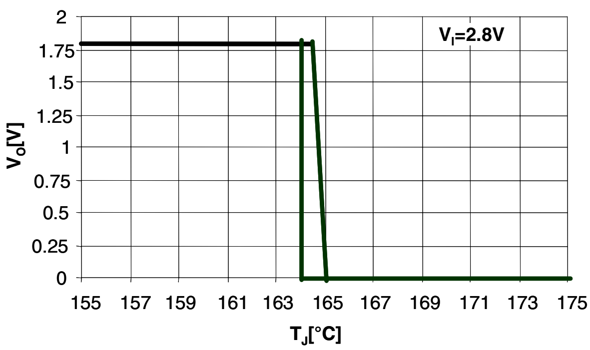


Figure 16. Thermal protection



7 Application information

The STLQ50xx is a BiCMOS linear regulator specifically designed for operating in environments with very low power consumption requirements. The very low quiescent current of 3 µA is obtained through the use of CMOS technology which makes the device suitable for application that have long standby time. Its very low power consumption allows extended battery life and the tiny packages (SOT323-5L or SOT23-5L) satisfy the space-saving requirements of battery-powered equipment. Moreover, the STLQ50xx provides wide input voltage operation from 2.5 V up to 12 V.

The PMOS pass element also permits a very good dropout values of 0.7 V at full load and at 125 °C without affecting consumption characteristics.

7.1 External components

The typical application schematic of the STLQ50xx is shown in *Figure 1* - *Figure 2*, 1 µF input and output capacitors placed close to the device are required for proper operation. The device is stable with electrolytic and ceramic output capacitors having values higher than 1 µF (see *Figure 10* for stability details).

In the adjustable version (STLQ50) the output voltage is programmed using an external resistor divider, as shown in *Figure 2*. The output voltage can be adjusted from 1.22 to 11 V and it can be calculated using the following equation:

Equation 1

$V_O = V_{FB} \times (1+R_1/R_2)$

where V_{FB} = 1.222 V is the internal reference voltage.

The sum of the R_1 and R_2 resistors should be chosen in order to guarantee at least 1 µA of divider current. Lower value resistors improve the noise performance but the quiescent current will increase. Higher value resistors should be avoided because the ADJ leakage current will influence the voltage set by the resistor divider, rendering the formula above no longer valid.

The suggested design procedure is to choose R_2 = 1 MΩ and then calculate R_1 using the following equation:

Equation 2

$R_1 = (V_O/V_{FB}-1) \times R_2$

7.2 Power dissipation

In order to ensure proper operation, the STLQ50 junction temperature should never exceed 125 °C; this limits the maximum power dissipation the regulator can sustain in any application. The maximum power dissipation can be calculated as:

Equation 3

$P_{DMAX} = (T_{JMAX} - T_A)/R_{thJA}$

where T_{JMAX} = 125 °C;

T_A is the ambient temperature;

R_{thJA} is the junction-to-ambient thermal resistance of the package (see *Table 4* thermal data).

The power dissipation can be calculated simply as:

Equation 4

$P_D = (V_I - V_O) \times I_O$

In every application condition, P_D must be lower than P_{DMAX}.

7.3 Protection

The PMOS pass element has an internal diode with anode connected to V_O and cathode to V_I. In case $V_O > V_I$, the current will flow from output to input without limitation. In this case, a proper limiting network is recommended.

The current limitation is automatically provided by the characteristics of the PMOS pass element (see typical characteristics), so the short-circuit current is dependent on the input voltage. When considering short-circuit current, take care in any case not to exceed the maximum sustainable power dissipation of the device.

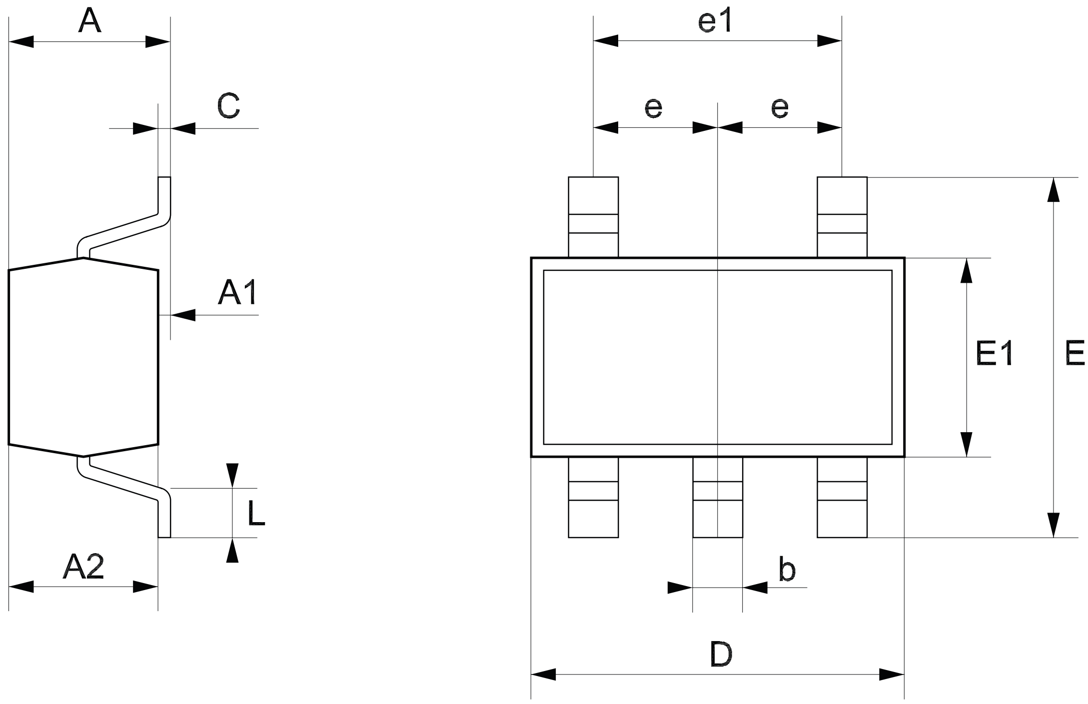
The STLQ50 features an internal thermal protection that linearly reduces the output current when the internal temperature increases. Consequently, at a given load, the output voltage decreases also. The action of the thermal protection starts at 125 °C when the output voltage slightly decreases, while close to 163 °C the output voltage drops to 0 V. Since this is a linear control, sudden overcurrent conditions can quickly raise the chip temperature without giving time for the thermal protection to act, so it cannot be used as a limitation for the output current.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

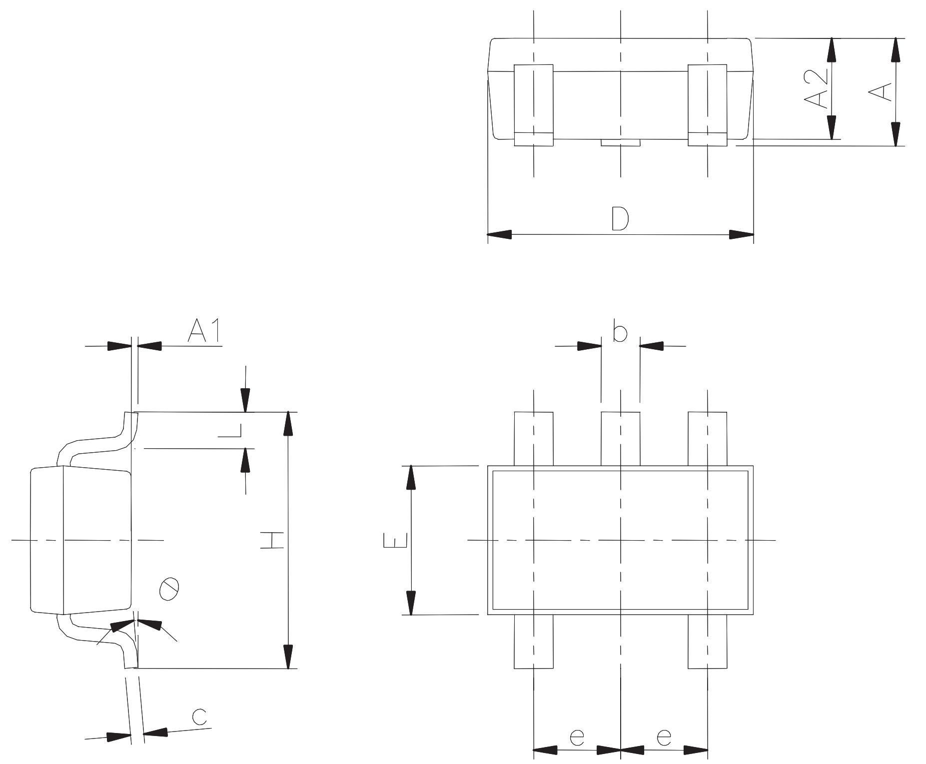
SOT323-5L mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	31.5		43.3
A1	0.00		0.10	0.0		3.9
A2	0.80		1.00	31.5		39.4
b	0.15		0.30	5.9		11.8
C	0.10		0.18	3.9		7.1
D	1.80		2.20	70.9		86.6
E	1.80		2.40	70.9		94.5
E1	1.15		1.35	45.3		53.1
e		0.65			25.6	
e1		1.3			51.2	
L	0.10		0.30	3.9		11.8



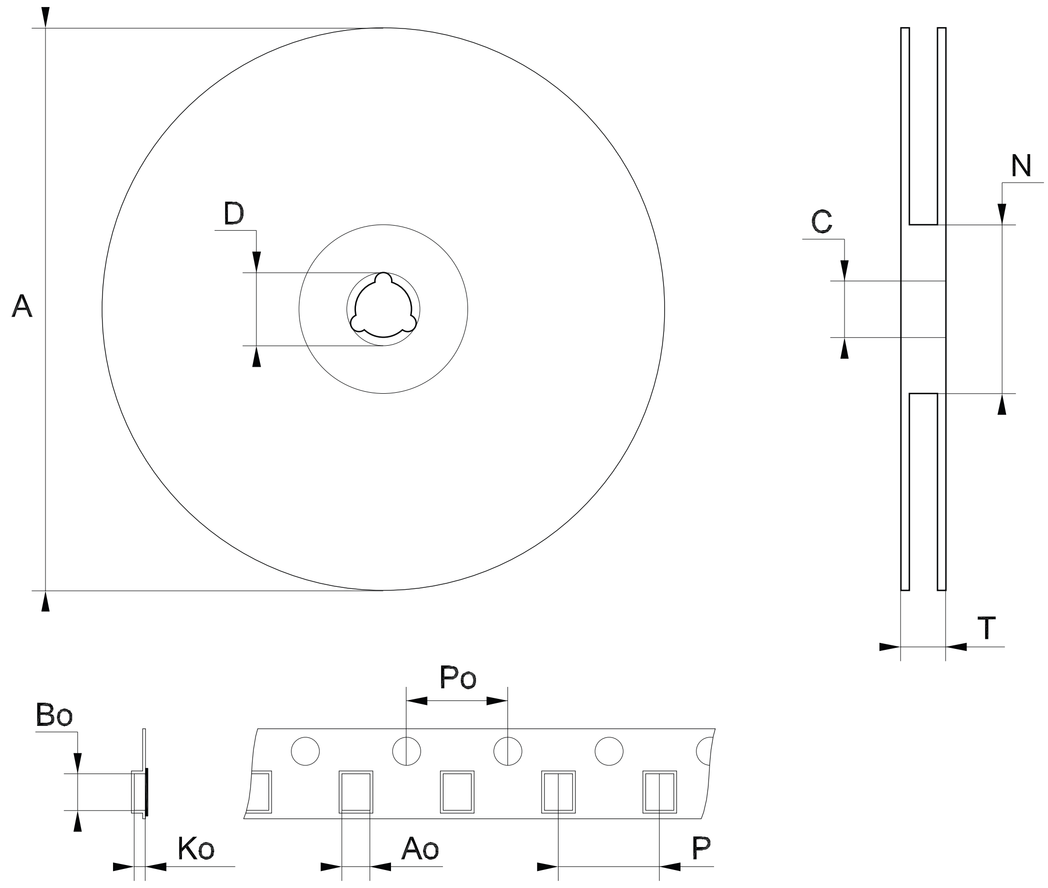
SOT23-5L mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



Tape & reel SOT323-xL mechanical data

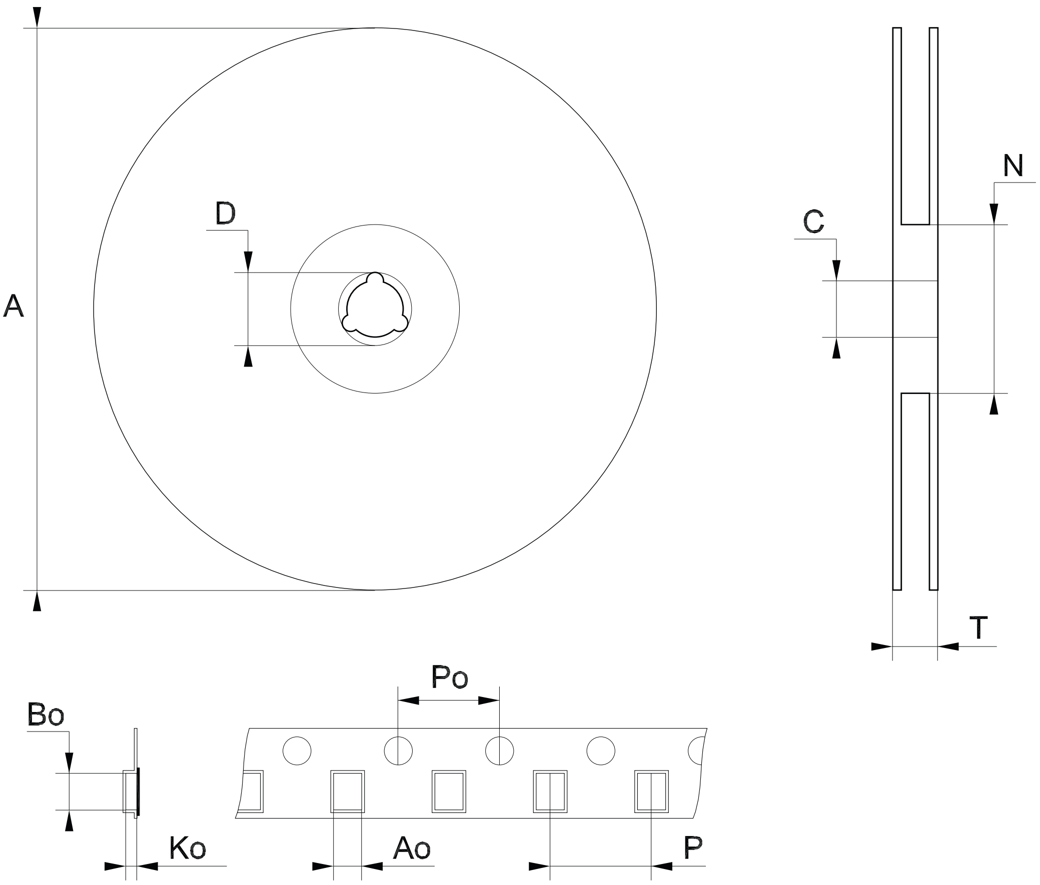
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	175	180	185	6.889	7.086	7.283
C	12.8	13	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	59.5	60	60.5		2.362	
T			14.4			0.567
Ao		2.25			0.088	
Bo		2.7			0.106	
Ko		1.2			0.047	
Po	3.9	4	4.1	0.153	0.157	0.161
P	3.8	4	4.2	0.149	0.157	0.165



Note: Drawing not in scale

Tape & reel SOT23-xL mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.0.58
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Note: Drawing not in scale

9 Revision history

Table 6. Document revision history

Date	Revision	Changes
07-Feb-2007	1	Initial release.
13-Feb-2007	2	Typo in cover page 350 mA ==> 350 mV.
06-Jul-2007	3	Added part number.
14-Nov-2007	4	Added *Table 1*.
31-Jan-2013	5	– Modified line regulation test condition *Table 5 on page 6*. – Minor text changes throughout the document.