AN2982
Application note

1 x 54 W T5 fluorescent lamp ballast in wide input voltage range using the L6585DE - STEVAL-ILB005V2

Introduction

This application note describes the STEVAL-ILB005V2 demonstration board equipped with the L6585DE lighting controller, STD7NM50N MOSFETs and an STTH1L06 Shottky diode able to drive a 54 W linear T5 fluorescent lamp in a wide input voltage range (88 - 277 Vac). The design steps, schematic and board performance are also given.

The L6585DE lighting controller embeds both the PFC stage and ballast stage suitable for driving all kinds of lamps (T8, T5, T4, CFLn,...) and all kinds of topologies having an input power greater than 25 W.

New T5 lamps are characterized by very high luminous efficiency and compactness. To optimize their performance, high accuracy in both preheating of the cathodes and steady-state parameters is required. The minimum performance of T5 ballasts together with their minimum safety requirements are summarized in international norms, especially IEC61347-2-3, IEC60929, and IEC60081.

The demand for these lamps is rapidly growing and the L6585DE is able to control electronic ballasts meeting all performance specifications and reliability with low component count and a small PCB.

The STEVAL-ILB005V2 has been developed to drive a 54 W T5-HO lamp.

Figure 1. STEVAL-ILB005V2 demonstration board

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1 Designing the application

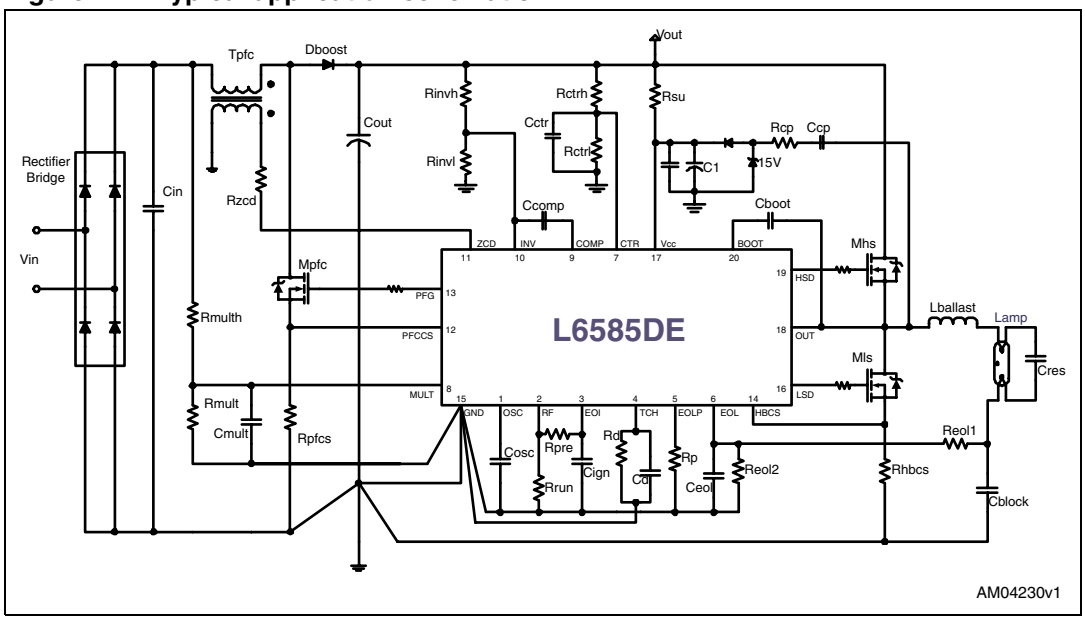
The STEVAL-ILB005V2 design follows the AN2870 design guidelines. In this section the design specifications and the equations used are given.

1.1 Design requirements

Table 1. Summary of design requirements

Description	Values
Input voltage	88 to 277 Vac (110 to 230 Vac ±20%)
Mains frequency	50 Hz – 60 Hz
PF	> 0.975
Current THD	< 10%
Lamp type	T5 -54 W HO (I_{lamp} = 460 mArms; V_{lamp} = 117 Vrms)
Max output voltage	900 Vrms
Lamp connection	Current preheated, C_{block} to ground topology
Efficiency	90%

Figure 2. Typical application schematic



1.2 PFC design

1.2.1 Output voltage and dynamic OVP

The maximum input voltage is equal to:

Equation 1

$$V_{in,max} = 277\ V \cdot \sqrt{2} = 391.7\ V$$

An output voltage equal to V_{out} = 420 V is chosen for better PFC performance.

Choosing R_{invh} = 3 x 2.2 MΩ, the output voltage is equal to:

Equation 2

$$V_{out} = 2.52V \cdot \left(1 + \frac{R_{invh}}{R_{invl}}\right) \rightarrow R_{invl} = \frac{R_{invh}}{\left(\frac{V_{out}}{2.52V} - 1\right)} = 39839\ \Omega \rightarrow R_{invi} = 39.7\,k\Omega$$

The ripple superimposed on V_{out} is chosen equal to 5%. Then, the maximum instantaneous output voltage is equal to 441 V and, therefore, the OVP level must be comprised between 450 V and 500 V.

- V_{OVP} = 480 V is chosen and the CTR pin voltage divider is dimensioned accordingly
- R_{ctrh} = 3 x 825 kΩ

Equation 3

$$V_{OVP} = 3.4\ V \cdot \left(1 + \frac{R_{ctrh}}{R_{ctrl}}\right) \rightarrow R_{ctrl} = \frac{R_{ctrh}}{\left(\frac{V_{OUT,MAX}}{3.4\ V} - 1\right)} = 17656\ \Omega \rightarrow R_{invi} = 18\,k\Omega$$

1.2.2 Boost choke design

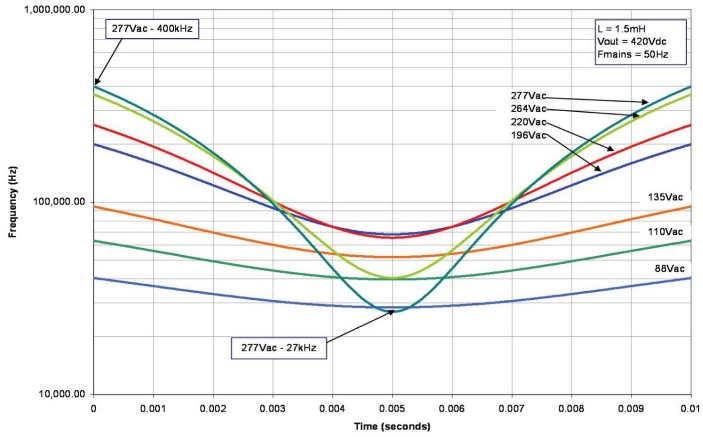
The minimum PFC frequency is chosen equal to $f_{PFC,min}$ > 15 kHz. The maximum inductance value is equal to:

Equation 4

$$f_{PFC,min} = \frac{V_{in}^2}{2 \cdot P_{in} \cdot L} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{in}}{V_{out}}\right) \rightarrow L \leq \frac{V_{in}^2}{2 \cdot P_{in} \cdot f_{PFC,min}} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{in}}{V_{out}}\right) = 2.6\ mH$$

L_{pfc} = 1.5 mH is selected. The following graph depicts the frequencies that are obtained along the mains period for various input voltages.

Figure 3. PFC MOSFET frequencies along mains half period (f_{mains} = 50 Hz) for various input voltages



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The maximum choke current is equal to:

Equation 5

$$I_{L,max} = 2 \cdot \sqrt{2} \cdot \frac{P_{in}}{V_{in,min}} = 1.93\ A$$

A saturation current higher than $I_{L,sat}$ = 2.2 A is used in order to take into account the tolerance of this parameter.

The RMS current flowing into the choke is equal to:

Equation 6

$$I_{L,RMS} = \frac{2}{\sqrt{3}} \frac{P_{in}}{V_{in,min}} = 787\ mA$$

The choke form factor is an EF25 core (A_e = 52 mm^2, l_e = 58 mm, material N87 or equivalent having B_{max}<320 mT).

Its design parameters are as follows:

Equation 7

$$\left.\begin{aligned} N &= \frac{I_{max}L}{B_{max}A_e} = 174\ turns \\ A_L &= \frac{L}{N^2} = 49.5\ nH/turns^2 \end{aligned}\right\} \rightarrow l_{gap} = 2 \times \frac{\mu_0 N^2 A_e}{L} = 2.63\ mm$$

The maximum power dissipation of the core should be less than 2.5 W in the worst condition.

A multi-conductor wire is used in order to reduce the equivalent resistance at high frequency.

When the maximum RMS current is obtained, the minimum frequency is detected and the RHF of the choke must be less than:

Equation 8

$$R_{HF,max} = \frac{P_{L,\Omega}}{I_{L,RMS}^2} = 4\ \Omega$$

Using a 13 x 0.1 mm^2 wire, 3.5 Ω is obtained.

The core losses, at minimum input voltage, are estimated below 0.35 W, therefore the total losses are lower than 2.5 W as expected. The higher the input voltage is, the lower the power dissipation (e.g. at 220 Vac the estimated total power losses are lower than 1.8 W).

The transformer ratio can be calculated as:

Equation 9

$$V_{aux,zcd} = \left(V_{out} - \sqrt{2} \cdot V_{in}\right) > m \cdot 1.4\ V \rightarrow m < 14.18 \rightarrow m = 6 \rightarrow N_{sec} = 29 turns$$

Considering a maximum ZCD current equal to 1 mA, the limiting resistor is:

Equation 10

$$R_{zcd} = \frac{\sqrt{2} \cdot V_{in,max}}{m \cdot I_{ZCD}} \rightarrow R_{zcd} > 65.3\ k\Omega \rightarrow R_{zcd} = 75\ k\Omega$$

1.2.3 MOSFET selection

The PFC MOSFET must have a V_{bdss} = 500 V and a peak drain current greater than $I_{d,max}$ = 2.2 A.

The maximum allowed MOSFET dissipation is equal to $P_{MOS,max}$ = 1 W in all conditions.

The total power dissipation is composed of:

- Conduction losses, dominant at low input voltage:

Equation 11

$$P_{COND} = R_{ds,on} \cdot I_{MOS,RMS}{}^2 = R_{ds,on} \cdot 8\left(\frac{P_{in}}{V_{in,rms}}\right)^2 \left[\frac{1}{6} - \frac{4\sqrt{2}}{9\pi}\frac{V_{in,rms}}{V_{out}}\right] = R_{ds,on} \cdot 0.5278\ A^2$$

Equation 12

$$R_{DS(on)}(max) < \frac{P_{COND,max}}{0.5278\ A^2}$$

- Switching losses, directly proportional to the average switching frequency:

Equation 13

$$\langle f_{SW} \rangle = \frac{V_{in,RMS}^2}{2 \cdot P_{in} \cdot L}\left(1 - \frac{2\sqrt{2}}{\pi} \cdot \frac{V_{IN,RMS}}{V_{out}}\right)$$

Equation 14

$$P_{cross} = t_f \langle f_{sw} \rangle V_{OUT} \frac{P_{in}}{V_{in,rms}} = \frac{t_f \langle f_{sw} \rangle}{V_{in,rms}} \cdot 25200$$

- Capacitive losses, present only when $V_{in} > V_{out}/2$ and have their maximum at $V_{in,max}$

The maximum time when the input voltage is greater than $V_{out}/2$ can be calculated as follows:

Equation 15

$$t_1 = \frac{\arcsin\left(\frac{V_{out}}{2 \cdot \sqrt{2} \cdot V_{in,rms}}\right)}{2\pi f_{mains}} \rightarrow 1.8\ \text{ms}$$

$$t_2 = \frac{1}{2f_{mains}} - t_1 \rightarrow 8.2\ \text{ms}$$

Within this interval the capacitive losses are:

Equation 16

$$P_{cap} = \langle f_{sw} \rangle \left(3.3 C_{oss} \langle V_{Drain} \rangle^{\frac{3}{2}} + \frac{1}{2}(C_{rss} + C_{oss} + C_{ext}) \langle V_{Drain} \rangle^2 \right)$$

where $<f_{sw}> = 173$ kHz and:

Equation 17

$$\langle V_{Drain} \rangle = \sqrt{2 f_{mains} \int_{t_1}^{t_2} \left[2\sqrt{2} \cdot V_{in,rms} \sin(\omega t) - V_{out} \right]^2 dt} = 209.7\ \text{V}$$

Using *Equation 11* to *17* with the constraint $P_{tot} < 1$ W, the following parameters are found:

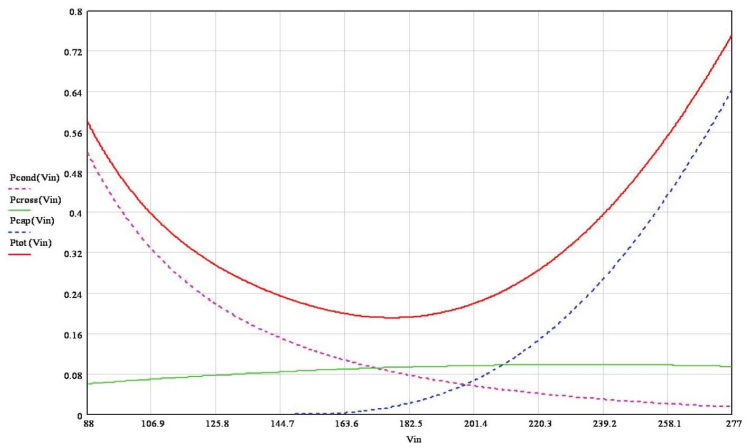
- $R_{DS(on)} < 1.4\ \Omega$ (P_{cond} at 88 V < 0.75 W)
- $t_f < 10$ ns (P_{cross} at 88 V < 0.10 W)
- $C_{oss} < 110$ pF (considering C_{ext} and C_{rss} equal respectively 68 pF and 4 pF)

The following ST MOSFETs meet these constraints:

- STD5NK50Z
- STD6NK50Z
- STD7NM50N

The STD7NM50N has $R_{DS(on)} = 1.12\ \Omega$ (at 100° C), $t_f = 9$ ns and $C_{oss} = 67$ pF and therefore is considered suitable for this design. The total power dissipation is shown in *Figure 4*.

Figure 4. Summary of PFC MOSFET power losses



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1.2.4 Boost diode selection

Both the boost diode maximum RMS current and the RMS current are equal to:

Equation 18

$$I_{d,rms} = \frac{4}{3}\frac{\sqrt{2\sqrt{2}}}{\pi}\frac{P_{in}}{\sqrt{V_{OUT}V_{in,rms}}} = 222\ \text{mA}$$

Their average current is equal to:

Equation 19

$$\frac{P_{out}}{V_{out}} = 142\,\text{mA}$$

The STTH1L06 Shottky diode is selected, having V_{rrm} = 600 V and an average forward current $I_{f(AV)}$ = 1 A. Total power dissipation is equal to:

Equation 20

$$P_D = 0.89 \cdot 0.142 + 0.165 \cdot 0.222^2 = 134.5\ \text{mW}$$

1.2.5 Bulk capacitor selection

The ripple superimposed on the output voltage is equal to ±20 V:

Equation 21

$$\Delta V_{out} = 20\ \text{V} = \frac{P_{out}}{4\pi \cdot f_{mains} \cdot V_{out} \cdot C_{out}} + ESR_{@f_{PFC,min}} \cdot I_{C_{out},RMS} =$$

$$= \frac{2.0463 \times 10^{-4}}{C_{out}} + ESR \cdot 373\ \text{mA}$$

The RMS value of the bulk capacitor current is:

Equation 22

$$I_{C_{out},RMS} = \sqrt{\frac{32 \cdot \sqrt{2}}{9\pi} \cdot \frac{P_{in}^2}{V_{in,rms} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}}\right)^2} = 373\ mA$$

Considering the first term of *Equation 21* as dominant, C_{out} > 10.2 µF, and then C_{out} = 22 µF is selected.

The voltage rating of the capacitor is equal to V_{Cout} = 450 V and the temperature class is T_{Cout} = 105 °C. With this value the typical ESR is around 2 Ω, adding only 740 mV to the total ripple.

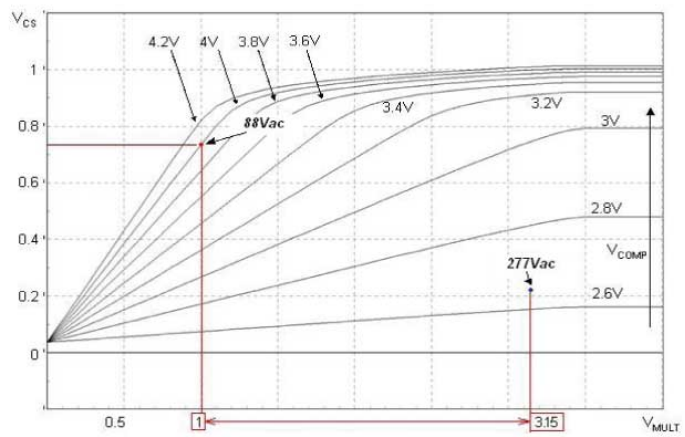
1.2.6 Multiplier biasing and selection of PFC current sense resistor

The peak values of the input voltage are between 124.4 V and 391.7 V. The ratio between these two values is equal to 3.15. The MULT pin is biased to 1 V when input voltage is equal to 124.4 V. If R_{multh} = 3x680 kΩ:

Equation 23

$$kp = \frac{V_{MULT,1}}{V_{in,min}\big|_{pk}} = 0.00804 \rightarrow R_{multl} = \frac{kp}{1-kp} R_{multh} = 16.53\ k\Omega \rightarrow \ R_{multh} = 16.2\ k\Omega$$

Figure 5. Multiplier bias points



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with $V_{CS,1}$ = 0.75 V:

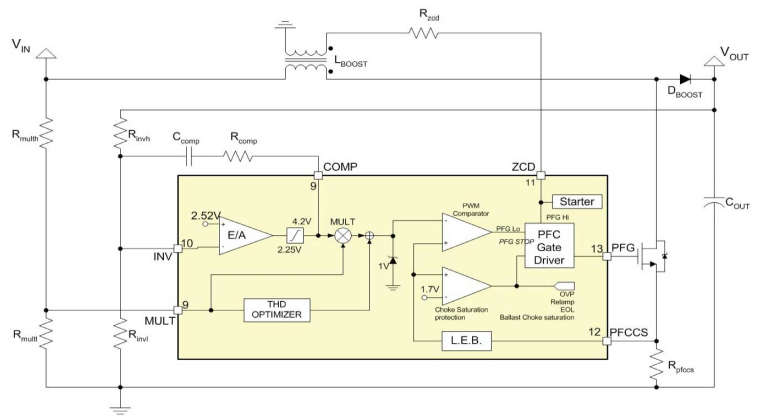
Equation 24

$$R_{pfccs} = \frac{V_{CS,1}}{I_{L,max}} = \frac{V_{CS,1} \cdot V_{in,min}}{2 \cdot \sqrt{2} \cdot P_{in}} = 0.364\ \Omega \rightarrow \ R_{pfccs} = 0.33\ \Omega$$

A C_{mult}=1 nF capacitor is used in parallel with R_{multl} for HF noise filtering.

1.2.7 Error amplifier compensation

Figure 6. Control loop block diagram



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Equation 25

$$G(s) = \frac{1}{4}\frac{k_M k_p V_{in,rms}^{\ 2}}{V_{out}}\frac{R_{out}}{R_{pfcs}}\frac{1}{1+s\frac{R_{out}C_{out}}{2}} = 0.020308 \cdot V_{in,rms}^{\ 2} \cdot \frac{1}{1+0.029623s}$$

where:

- k_M = multiplier factor = 0.52
- k_p = mult pin divider = 0.007879
- R_{out} = equivalent output resistor = 2.693 kΩ
- C_{out} = 22 µF

Using the simplest compensation network (a capacitor placed between the INV and COMP pin) whose transfer function is equal to:

Equation 26

$$G_{comp}(s) = \frac{1}{sC_{comp}R_{invh}} = \frac{1}{sC_{comp} \cdot 6.6\ M\Omega}$$

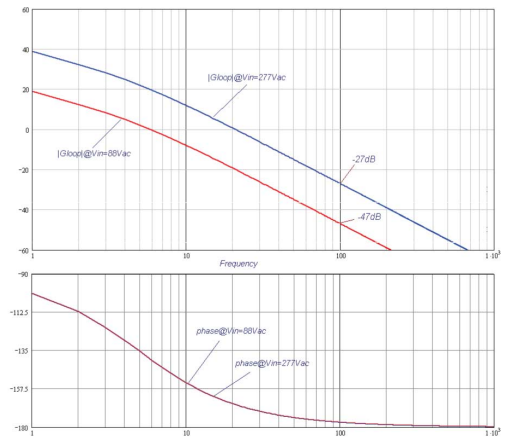
and setting an open loop gain less than 0.001 when frequency is equal to twice the mains frequency, it is possible to calculate the minimum capacitance needed.

Equation 27

$$G_{loop}(s)\Big| = G(s) \cdot G_{comp}(s)\Big| = \left|\left(\frac{1}{sC_{comp}6.6\ M\Omega}\right) \cdot 0.020308 \cdot V_{in,rms}^{\ 2} \cdot \frac{1}{1+0.029623s}\Bigg|_{s=2\ \pi 100\ Hz}\right| = 0.001$$

A C_{comp} = 1 µF ceramic capacitor could be a good trade-off between performance and cost, but better performance can be obtained using a more complicated structure in order to obtain a phase margin equal to 45°.

Figure 7. Bode plot with simple compensation network: $|Gloop|_{MAX}$ < 35dB



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For example, an RC-series network is connected between the INV and COMP pin. The obtained $G_{loop}(s)$ can be written as:

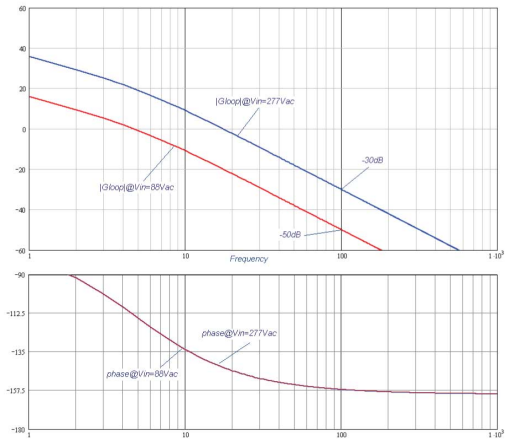
Equation 28

$$G_{loop}(s)\Big| = G(s)\cdot G_{comp}(s)\Big| = \left|\left(\frac{1+sC_{comp}R_{comp}}{sC_{comp}6.6\ M\Omega}\right)\cdot 0.020308\cdot V_{in,rms}{}^{2}\cdot\frac{1}{1+0.029623s}\right|$$

A phase margin equal to 45° is obtained at Vin = 277 Vac using C_{comp}=1.5 µF and R_{comp}=39 kΩ. At minimum input voltage the phase margin is equal to 85°.

Higher values of C_{comp} or a lower value of C_{out} can also improve the PFC performance.

Figure 8. Bode plot with enhanced compensation network: $|G_{loop}|_{MAX}$ < 35 dB and Φ margin > 45°



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1.2.8 Input rectifier

A 2KBP06M bridge rectifier is able to sustain 600 V in reverse condition and 2 A of forward current. Its maximum power dissipation is equal to:

Equation 29

$$P_B = 2\sqrt{2}\frac{P_{in}}{V_{in,rms(min)}}V_F = 1.73\ W$$

1.2.9 Input capacitor

Let r = 10% be the maximum allowed ratio between the high-frequency ripple amplitude seen at the input of the PFC stage and the mean value of the input current:

Equation 30

$$C_{in,min} = \frac{P_{in}}{2\pi \cdot r \cdot \langle f_{sw} \rangle_{min} \cdot V_{in,RMS(min)}^{2}} = 401.87\ nF \rightarrow C_{in} = 470\ nF$$

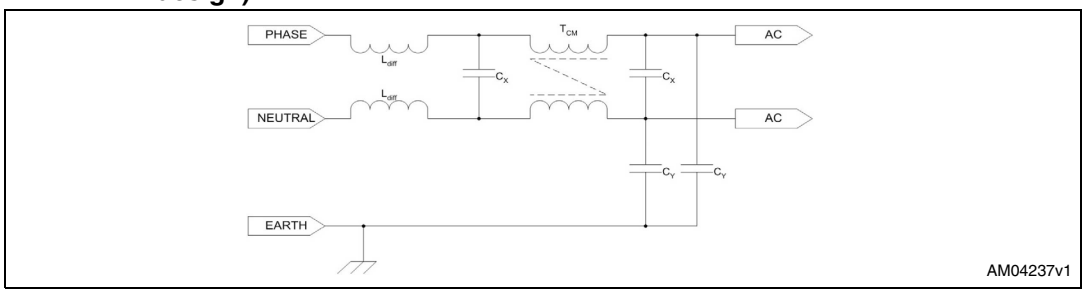
1.2.10 Input circuitry

The input circuitry is composed of:

- A fuse: avoids damage due to ballast breaking or excessive current from the mains
- An NTC: limits the inrush current which avoids blowing the fuse and reduces the effects of a burst from the mains. This component reduces its resistance at a higher temperature. A 5 Ω NTC (at 25 °C) is used
- A varistor (not present): absorbs the energy associated with a mains surge avoiding that V_{out} increases over the rated voltage of the components (C_{out}, MOSFETs, IC,…)
- An EMI filter: an LC network able to reduce the HF noise coming from the application and traveling through the mains. This filter has to filter both the common mode component of the noise (which can be measured between the AC input and the EARTH) and the differential mode component of the noise (which can be measured between the two AC inputs)

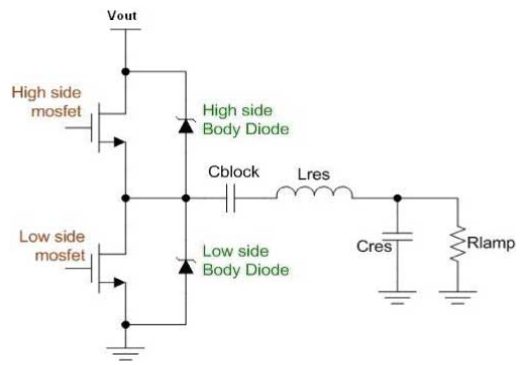
The first component (the fuse) is filtered by a CM filter (a current transformer that forces the AC input currents to travel in the opposite way) and two 1 nF capacitor placed between each AC input and EARTH. The second component (the NTC) is filtered by two capacitors placed across the AC inputs and by the leakage inductance of the CM filter. In fact by using a CM transformer having a high leakage inductance, a differential filtering can be obtained. The differential capacitors are equal to C_X = 100 nF, while the CM capacitors are equal to C_Y = 1 nF. The CM transformer, T_{CM}, is a B82733F series transformer from EPCOS.

Figure 9. Complete EMI filter (differential mode inductors are not present in this design)



2 Ballast stage design

Figure 10. Resonant inverter simplified schematic



2.1 Resonant network and operating point design

Equivalent voltage applied to the resonant network:

Equation 31

$$V_{bal,pk} = \frac{2}{\pi} V_{out} = 267.38 \text{ Vpk}$$

L and C are chosen in order to fit the following constraints:

- Preheating voltage has to be less than 240 Vac = 339.4 Vpk
- Maximum striking voltage is equal to 700 Vac
- Nominal lamp voltage = 117 Vac
- Nominal lamp current = 0.46 A

Selecting a common value equal to L_{res}=1.35 mH and C_{res}=4.7 nF, the following parameters are obtained:

Equation 32

$$\begin{cases} f_0 = \dfrac{1}{2\pi\sqrt{L_{res}C_{res}}} = 64387 \text{ Hz} \\ Z_0 = \sqrt{\dfrac{L_{res}}{C_{res}}} = 526\ \Omega \\ Q = \dfrac{R_{lamp}}{Z_0} = \dfrac{V_{run}}{I_{run}Z_0} = 0.4836 \end{cases}$$

The run and preheating frequencies are calculated using the values calculated in *Equation 33:*

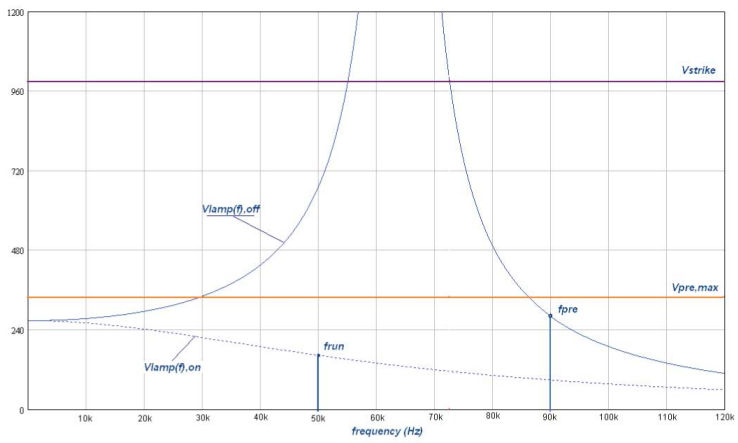
Equation 33

$$f_{run} = f_0 \sqrt{\frac{\left(2-\frac{1}{Q^2}\right)+\sqrt{\left(2-\frac{1}{Q^2}\right)^2-4+\left(\frac{4V_{out}}{\pi \cdot Z_0 \cdot Q \cdot \sqrt{2} I_{run}}\right)^2}}{2}} = 48.5\ \text{kHz}$$

$$f_{pre} = f_0 \sqrt{1+\frac{2V_{out}}{\pi V_{pre}}} > 86\ \text{kHz} \rightarrow f_{pre} = 100\ \text{kHz}$$

$$f_{ign} = f_0 \sqrt{1+\frac{2V_{out}}{\pi \cdot \sqrt{2} \cdot V_{ign}}} \approx 72.5\ \text{kHz}$$

Figure 11. Resonance curves



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The maximum striking current is equal to:

Equation 34

$$I_{ballast,ign} = \left(\frac{2 \cdot V_{out}}{\pi \cdot Z_0} \sqrt{\frac{1+\left(Q\frac{f_{ign}}{f_0}\right)}{Q^2\left[1-\left(\frac{f_{ign}}{f_0}\right)^2\right]^2+\left(\frac{f_{ign}}{f_0}\right)^2}} \right) = 2.121\ \text{Apk}$$

This current is also the saturation current of the ballast choke ($I_{sat,ballast}$ > 2.2 A).

Limiting the current to this value, the lamp voltage is limited to 700 Vac ($V_{Cres,max}$ > 700 Vac). The half-bridge current sense resistor is chosen according to:

Equation 35

$$R_{hbcs} = \frac{V_{hbcsh}}{I_{ballast,ign}} = \frac{1.6\ \text{V}}{2.121\ \text{A}} = 0.7543\ \Omega \rightarrow R_{pfccs} = 0.33\ \Omega$$

The RMS value of one side of the half bridge is equal to:

Equation 36

$$I_{hb,RMS} \approx \frac{I_{ballast,pk}}{2} = \frac{1}{2} \cdot \frac{2 \cdot V_{out}}{\pi \cdot Z_0} \sqrt{\frac{1 + \left(Q \frac{f_{run}}{f_0}\right)}{Q^2 \left[1 - \left(\frac{f_{run}}{f_0}\right)^2\right]^2 + \left(\frac{f_{run}}{f_0}\right)^2}} = 0.3465 \text{ A}$$

The power dissipation of the half-bridge current sense resistor is equal to:

Equation 37

$$P_{hbcs} \approx R_{hbcs} \cdot I^2_{hbcs,RMS} < 100 \text{ mW}$$

A blocking capacitor C_{block} = 100 nF (400 Vac) is used.

The choke form factor is an EF25 core (A_e = 52 mm^2, l_e = 58 mm, material N87 or equivalent having B_{max}<300 mT).

Its design parameters are as follows:

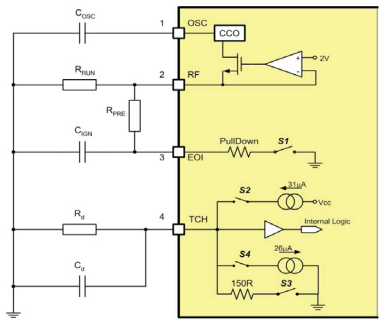
Equation 38

$$\left.\begin{aligned} N &= \frac{I_{max} L}{B_{max} A_e} = 183 \text{ turns} \\ A_L &= \frac{L}{N^2} = 38.8 \text{ nH/turns}^2 \end{aligned}\right\} \rightarrow I_{gap} = 2 \times \frac{\mu_0 N^2 A_e}{L} = 3.37 \text{ mm}$$

For this component a multi-conductor wire is also used to reduce the HF equivalent resistance, and therefore the power dissipation.

2.2 Selection of parameters

Figure 12. Parameters setting block



C_{osc} = 1 nF (5% or better) is chosen.

The following constant values are calculated (C_{OSC} in pF):

Equation 39

$$k = \frac{499.6 \cdot 10^3}{(C_{OSC})^{0.872}} = 1209.55$$

Equation 40

$$e = 1 - \frac{1.33}{(C_{OSC})^{0.581}} = 0.976$$

Given the run frequency and the preheating frequency (both in kHz), the following components are found:

Equation 41

$$R_{run} = \left(\frac{k}{f_{run}}\right)^{\frac{1}{e}} = 26.99\ k\Omega \rightarrow R_{run} = 26.7\ k\Omega$$

$$R_{pre} // R_{run} = \left(\frac{k}{f_{pre}}\right)^{\frac{1}{e}} = 12.86\ k\Omega \rightarrow R_{pre} = \frac{R_{run} \cdot 12.86\ k\Omega}{R_{run} - 12.86\ k\Omega} = 24.9\ k\Omega$$

An ignition time equal to 50 ms is obtained using a C_{ign} corresponding to:

Equation 42

$$T_{ign} = 3R_{pre}C_{ign} \rightarrow C_{ign} = 680nF$$

A protection time equal to 120 ms is adopted, then:

Equation 43

$$T_{prot} = 269740 \cdot C_d \rightarrow C_d = 470nF$$

The preheating time is equal to almost 1 s, therefore:

Equation 44

$$T_{pre} = 4.63\frac{C_d}{I_{TCH}} + R_d C_d \ln\left(\frac{4.63}{1.5}\right) \rightarrow R_d = 1.755M\Omega$$

The closest commercial resistor for R_d is 1.5 MΩ. With this value T_{pre} is equal to 865 ms.

2.3 Half-bridge design

The maximum power loss acceptable for half-bridge MOSFETs is equal to 500 mW. Each MOSFET experiences a conduction loss equal to:

Equation 45

$$P_{cond} = R_{DS(on)} \cdot (I_{rms})^2 < 0.25\ W$$

With $I_{rms}^2 = 0.120\ A^2$, a maximum $R_{DS(on)} = 2.08\ \Omega$ is obtained.

The following ST MOSFETs meet these constraints:

- STD5NK50Z
- STD6NK50Z
- STD7NM50N

The STD7NM50N has $R_{DS(on)}$= 1.12 Ω (at 100°C), therefore the power dissipation related to the half-bridge MOSFETs is equal to almost 270 mW.

The size of the boostrap capacitor can be calculated by solving the following equation:

Equation 46

$$C_{gate} + C_{boot,min} = \frac{C_{boot,min} \cdot V_{cc}}{V_{cc} - \Delta V}$$

where:

$\Delta V = V_{cc,min} - V_{gate,min} = 9.6\ V - 8\ V = 1.6\ V$

$V_{cc} = 15\ V - V_f$, V_f = forward voltage of charge pump diode = 0.8 V

Q_g = total gate charge of STD7NM50N = 12 nC

$C_{gate} = Q_g/V_{cc} = 845\ pF$

$C_{boot,min}$ = 6.6 nF is obtained

A C_{boot} = 100 nF is selected and the voltage drop is equal to ΔV = 120 mV.

The charging time of the capacitor is calculated to check if ΔV is compensated during the on-time of the low side. The time the capacitor takes to charge to 95% of V_{cc} starting from 0 is equal to:

Equation 47

$$t_0 = 3 \cdot R_{boot} \cdot C_{boot} = 3 \cdot 250\ \Omega \cdot 100\ nF = 75\ \mu s$$

The time the capacitor takes to charge to 95% of V_{cc} minus 120 mV starting from 0 is equal to:

Equation 48

$$t_1 = -R_{boot} \cdot C_{boot} \cdot \ln\left(1 - \frac{0.95 \cdot V_{cc} - 0.12}{V_{cc}}\right) = 2.839 \cdot R_{boot} \cdot C_{boot} = 71\ \mu s$$

The difference $t_0 - t_1$ = 4 µs is smaller than the minimum on-time equal to:

Equation 49

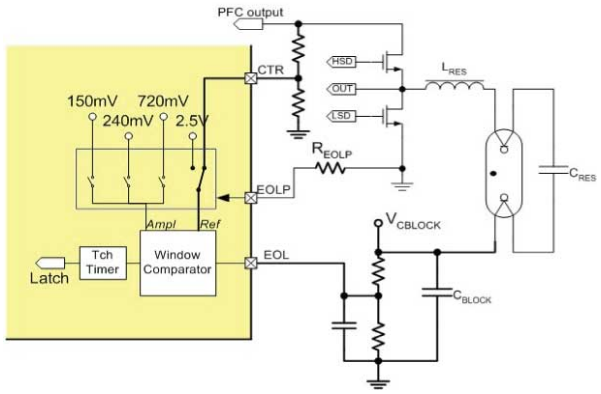
$$T_{on,min} = \frac{1}{2f_{pre}} - T_{DEAD,max} = 4.11\ \mu s$$

The selected capacitor is able to correctly supply the high-side driver.

2.4 End of life detection

In this design the blocking capacitor to ground configuration is chosen.

Figure 13. Blocking capacitor to ground topology



The tracking configuration with a window of amplitude equal to 240 mV is selected, connecting EOLP to ground with R_{EOLP} = 240 kΩ.

The EOL pin detects the blocking capacitor voltage by means of a voltage divider that, in normal conditions, sets its voltage to the same value as the CTR pin:

Equation 50

$$V_{CTR,0} = V_{out}\frac{R_{ctrl}}{R_{ctrl}+R_{ctrh}} = 3.03\ V \leftarrow V_{EOL}$$

Choosing the total upper resistor value equal to R_{eol1} = 1.36 MΩ (2x680 kΩ), and with the steady-state value of the blocking capacitor voltage equal to $V_{out}/2$, the lower resistor is calculated as:

Equation 51

$$R_{eol2} = R_{eol1}\frac{2V_{EOL}}{V_{OUT}-2V_{EOL}} = 19.9\ k\Omega \rightarrow R_{eol2} = 20\ k\Omega$$

A C_{eol} = 10 nF capacitor is used to filter the lamp frequency, maintaining the ripple. The obtained cutoff frequency is calculated higher than 100 Hz, but lower than 49 kHz.

Equation 52

$$f_{c,eol} \approx \frac{1}{2\pi \cdot R_{eol2} \cdot C_{eol}} = 796\ Hz$$

2.5 IC power supply design

The IC current consumption depends on both the PFC frequency and half-bridge frequency. In the worst case, the mean value of the PFC frequency is equal to 162 kHz and the maximum half-bridge frequency is equal to 90 kHz.

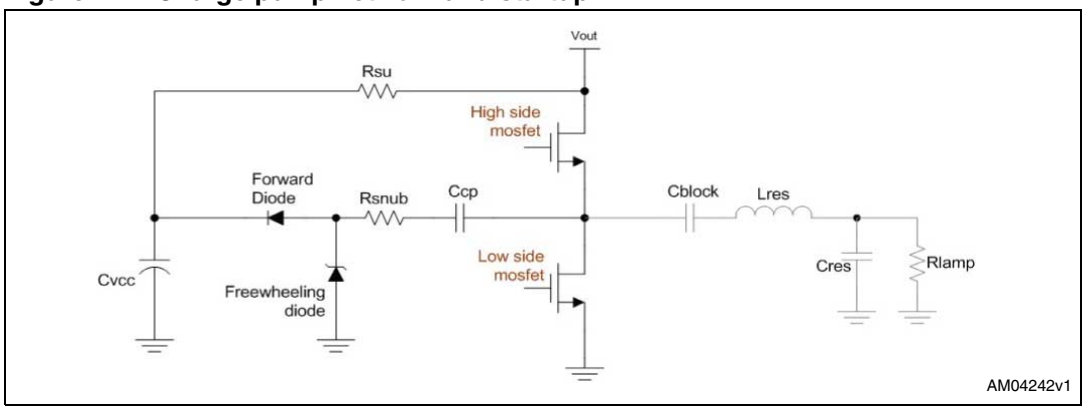
With these values the maximum supply current is approximately equal to:

Equation 53

$$I_{cc_{mA}} = 0.0192 \cdot \langle f_{PFC} \rangle_{kHz} + 0.0373 f_{pre_{kHz}} + 4.56 \approx 11\,mA$$

This current is delivered to the IC by means of a charge pump connected to the middle point of the half bridge.

Figure 14. Charge pump network and startup



The current delivered by the charge pump capacitor is approximately:

Equation 54

$$I_{cp} = I_{cp,pk} \cdot T_{rise} \cdot f_{run} \geq I_{cc}$$

where:

Equation 55

$$I_{cp,pk} = C_{cp} \frac{V_{out}}{T_{rise}}$$

and rearranging the terms:

Equation 56

$$C_{cp} \geq \frac{I_{cp}}{V_{OUT} \cdot f_{run}} = 558\ pF \rightarrow \quad C_{cp} = 1\ nF$$

The startup network works also as a detector of lamp presence. This feature can be implemented by placing one or both of the lamp cathodes along the startup network path. If the lamp is absent, the IC cannot start.

The minimum startup current of the L6585DE is equal to $I_{cc,on}$ = 370 µA. This current has to be delivered to the IC at the minimum input voltage (125 Vpk), therefore a total resistance equal to:

Equation 57

$$R_{su,tot} = \frac{V_{in,min}}{I_{cc,on}} = 337\ k\Omega$$

The network is divided into 5 x 68 kΩ resistors in order to avoid damage due to the lamp striking voltage.

A C1 = 10 µF followed by a 100 nF ceramic capacitor is used as the V_{cc} bulk capacitor.

3 Demonstration board schematic and bill of material

Figure 15. STEVAL-ILB005V2 schematic

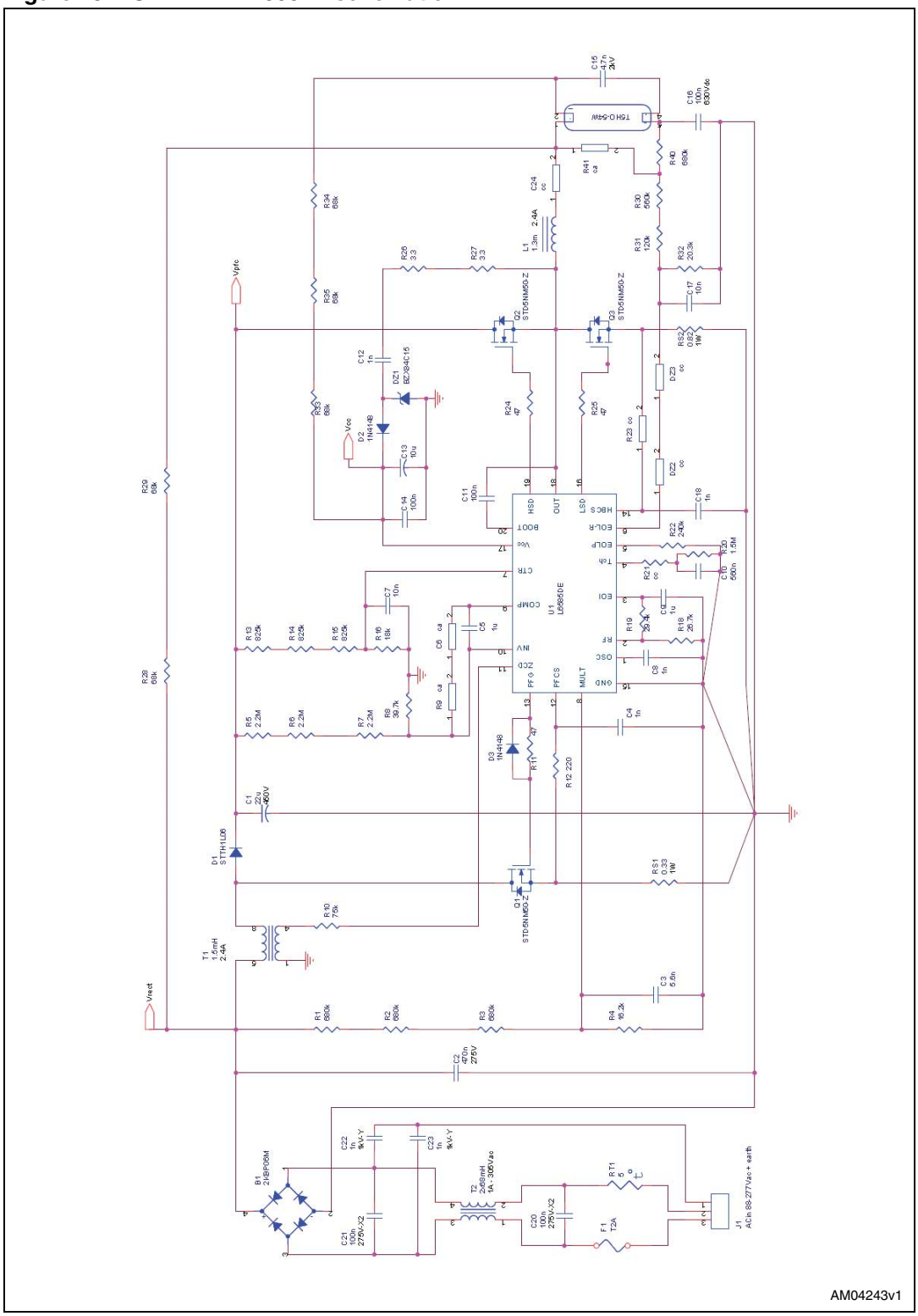


Table 2. BOM

Reference	Value	Note
R1	681 kΩ	$R_{mult,hi}$
R2	681 kΩ	
R3	681 kΩ	
R4	16.2 kΩ	$R_{mult,lo}$
R5	2.2 MΩ	$R_{inv,hi}$
R6	2.2 MΩ	
R7	2.2 MΩ	
R8	39.2 kΩ	$R_{inv,lo}$
R9	n.m.	
R10	75 kΩ	R_{zcd}
R11	47 Ω	PFC MOSFET gate resistor
R12	220 Ω	PFC current sense filtering resistor
R13	825 kΩ	$R_{ctr,hi}$
R14	825 kΩ	
R15	825 kΩ	
R16	18 kΩ	$R_{ctr,lo}$
R18	26.1 kΩ	R_{run}
R19	29.4 kΩ	R_{pre}
R20	1.5 MΩ	R_D
R21	0R0	
R22	240 kΩ	R_{eolp}
R23	0R0	
R24	47 Ω	High-side MOSFET gate resistor
R25	47 Ω	Low-side MOSFET gate resistor
R26	3.3 Ω	Charge pump limiting resistor
R27	3.3 Ω	
R28	68 kΩ	Startup network
R29	68 kΩ	
R30	560 kΩ	$R_{EOL,hi}$ (1)
R31	120 kΩ	
R32	20.5 kΩ	$R_{EOL,lo}$
R33	68 kΩ	Startup network
R34	68 kΩ	
R35	68 kΩ	

Table 2. BOM (continued)

Reference	Value	Note
R40	680 kΩ	$R_{EOL,hi}$ (2)
R41	n.m.	
RS1	0.33 Ω – 0.5 W	R_{pfccs}
RS2	0.82 Ω – 0.5 W	R_{hbcs}
C1	22 µF – 450 V	C_{OUT}
CA1	0R0	
C2	470 nF – 305 Vac	C_{in}
C3	4.7 nF	MULT filtering capacitor
C4	1 nF	PFCCS filtering capacitor
C5	1 µF	C_{comp}
C6	n.m.	
C7	10 nF	CTR filtering capacitor
C8	1 nF - 1%	C_{osc}
C9	1 µF	C_{ign}
C10	470 nF	C_d
C11	100 nF	C_{boot}
C12	1 nF - 630Vdc	C_{cp}
C13	10 µF	C_{Vcc}
C14	100 nF	$C_{Vcc,b}$
C15	4.7 nF - 2 kV	C_{res}
C16	100 nF - 630Vdc	C_{block}
C17	10 nF	EOL filtering capacitor
C18	1 nF	
C20	100 nF, X2, 275Vac	Differential mode EMI filter
C21	100 nF, X2, 275Vac	Differential mode EMI filter
C22	1 nF Y1	Common mode EMI filter (capacitive)
C23	1 nF Y1	Common mode EMI filter (capacitive)
C24	0R0	
D1	STTH1L06	Boost diode
D2	1N4148	Charge pump forward diode
D3	1N4148	PFC gate speed-up diode
DZ1	BZX84C15	Charge pump free-wheeling Zener diode
DZ2	0R0	
DZ3	0R0	
DZ4	n.m.	

Table 2. BOM (continued)

Reference	Value	Note
B1	2KBP06M	Rectifier bridge
U1	L6585DE	Ballast controller
Q1	STD7NM50N	PFC MOSFET
Q2	STD7NM50N	Half-bridge high-side MOSFET
Q3	STD7NM50N	Half-bridge low-side MOSFET
T1	1.5 mH - 2.6 A	PFC transformer – EPCOS B78313P8140
T2	2 x 68 mH - 0.9 A	Common mode EMI filter – EPCOS B82733F2901
L1	1.3 mH - 2.6 A	Ballast choke – ITACOIL E2543-H
F1	T 2 A – 250 Vac	Fuse
RT1	NTC 5 Ω	Inrush current limiter

3.1 Demonstration board performances

Figure 16. Input performance - power factor

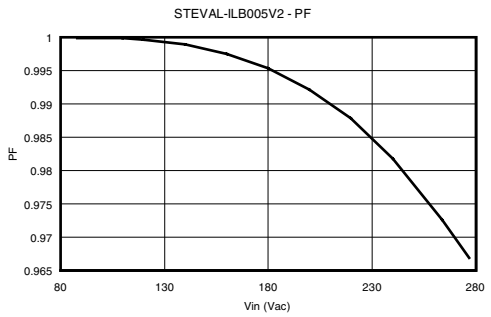


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Figure 17. Input performance - total harmonic distortion

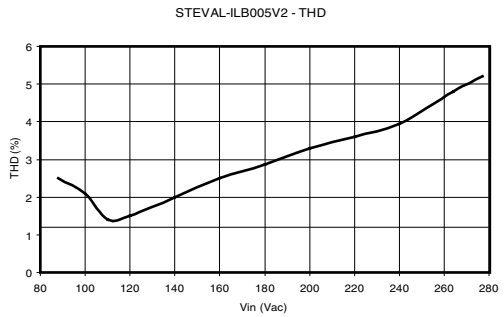

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Figure 18. EMI spectrum at 277 Vac

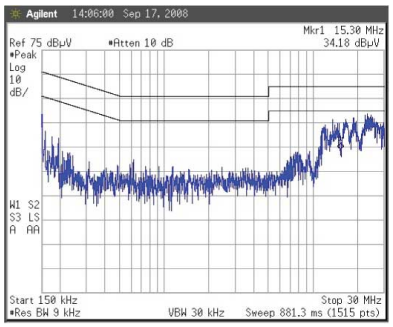

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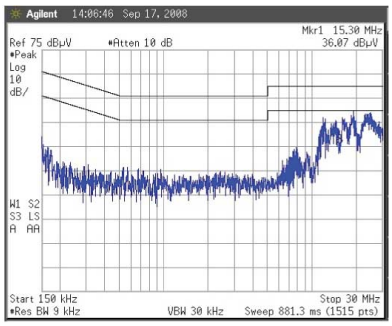
Figure 19. EMI spectrum at 88 Vac



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3.2 Ballast stage performance and reliability

Figure 20 shows the lamp parameters. Small discrepancies between theoretical and real measurements are due to the tolerance of the passive components of the resonance network (L_{res} and C_{res}).

Figure 20. Steady-state lamp parameters

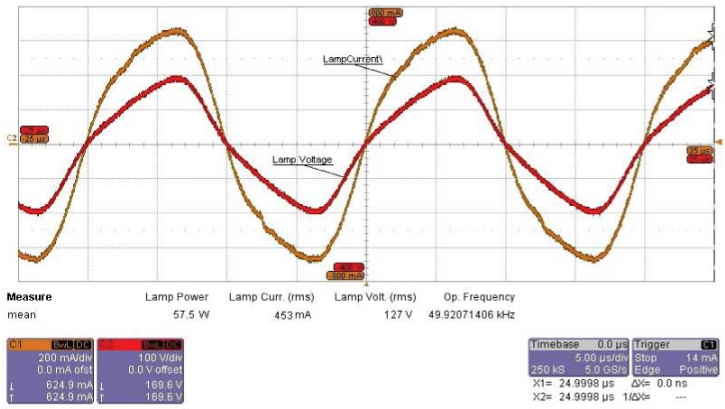
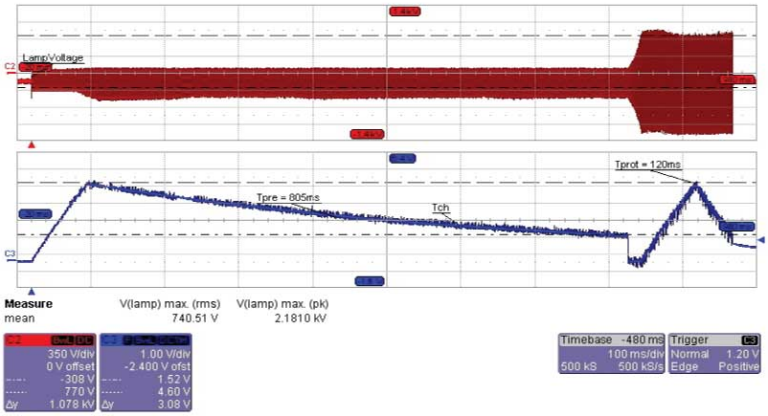


Figure 21 summarizes the T_{ch} sequences during preheating and protections. During the open lamp test, T_{ch} voltage (lower trace) sets the preheating time (T_{pre} = 805 ms). After that the lamp voltage (upper trace) increases up to the maximum value allowed by the HBCS resistor (740 Vrms). The subsequent protection time is shorter than the preheating time (120 ms).

Figure 21. Startup sequence with open lamp protection

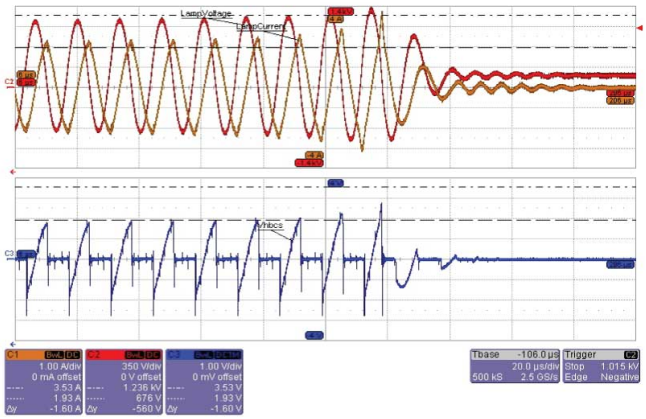


In *Figure 22* a close-up of the waveforms during a ballast choke saturation is shown. The upper graph illustrates the lamp parameters. While the lamp voltage remains essentially sinusoidal, the lamp current becomes triangular cycle by cycle. The lower trace illustrates the half-bridge current sense voltage (V_{HBCS}). As soon as this voltage reaches 2.75 V, the application is immediately stopped.

The saturation effect does not have a definite threshold. Once the current is close to saturation, the inductance value starts to decrease slowly and constantly, therefore a current

limiting that maintains the frequency constant is not suitable to counter this effect. Actually the application should be stopped as soon as the saturation effect is detected.

Figure 22. Ballast anti-choke saturation protection



Asymmetrical ageing of the lamp is detected by the EOL pin. *Figure 23* and *24* illustrate the behavior of this protection. In the upper trace the lamp voltage and T_{ch} voltage are shown. When the lamp starts ageing, the lamp voltage increases in one direction. The EOL voltage (lower trace) moves together with the blocking capacitor voltage. Once the difference between the CTR voltage and the EOL voltage is higher than 240 mV, a T_{ch} cycle is started and the application is stopped if this situation persists.

Figure 23. EOL protection (positive deviation)

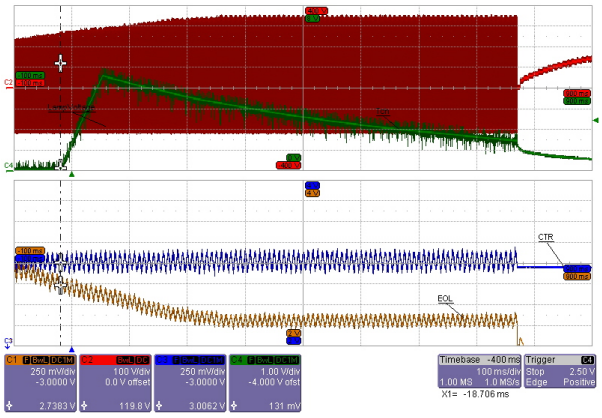
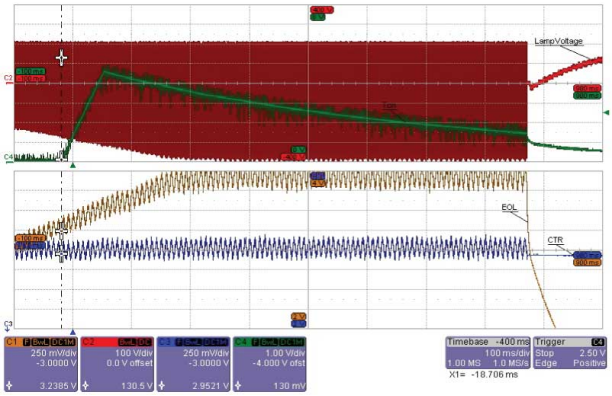


Figure 24. EOL protection (negative deviation)



AM04252v1

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
15-Mar-2010	1	Initial release.

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