



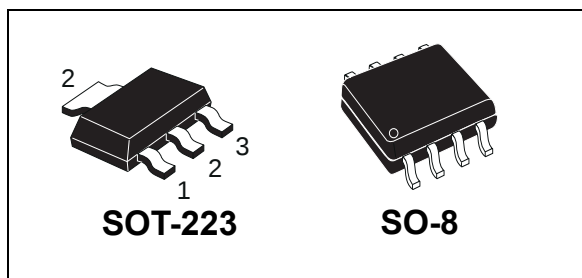
VNL5050N3-E VNL5050S5-E

OMNIFET III
fully protected low-side driver

Features

Type	V _{clamp}	R _{DS(on)}	I _D
VNL5050N3-E	41 V	50 mΩ	19 A
VNL5050S5-E			

- ? Drain current: 19 A
- ? ESD protection
- ? Overvoltage clamp
- ? Thermal shutdown
- ? Current and power limitation
- ? Very low standby current
- ? Very low electromagnetic susceptibility
- ? In compliance with the 2002/95/EC european directive
- ? Open drain status output^(a)



Description

The VNL5050N3-E and VNL5050S5-E are monolithic devices made using STMicroelectronics VIPower Technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. Output current limitation protects the devices in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

a. Valid for VNL5050S5-E only

Table 1. Devices summary

Package	Order codes	
	Tube	Tape & reel
SOT-223	VNL5050N3-E	VNL5050N3TR-E
SO-8	VNL5050S5-E	VNL5050S5TR-E

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1 Block diagrams and pins configurations

Figure 1. VNL5050N3-E block diagram

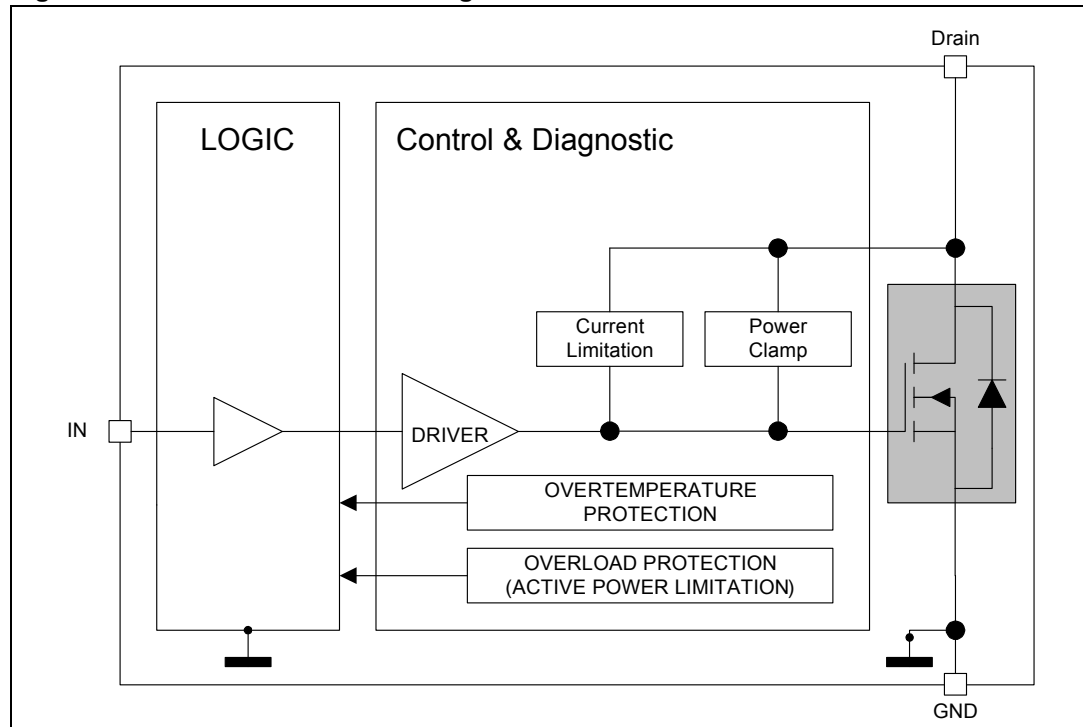


Figure 2. VNL5050S5-E block diagram

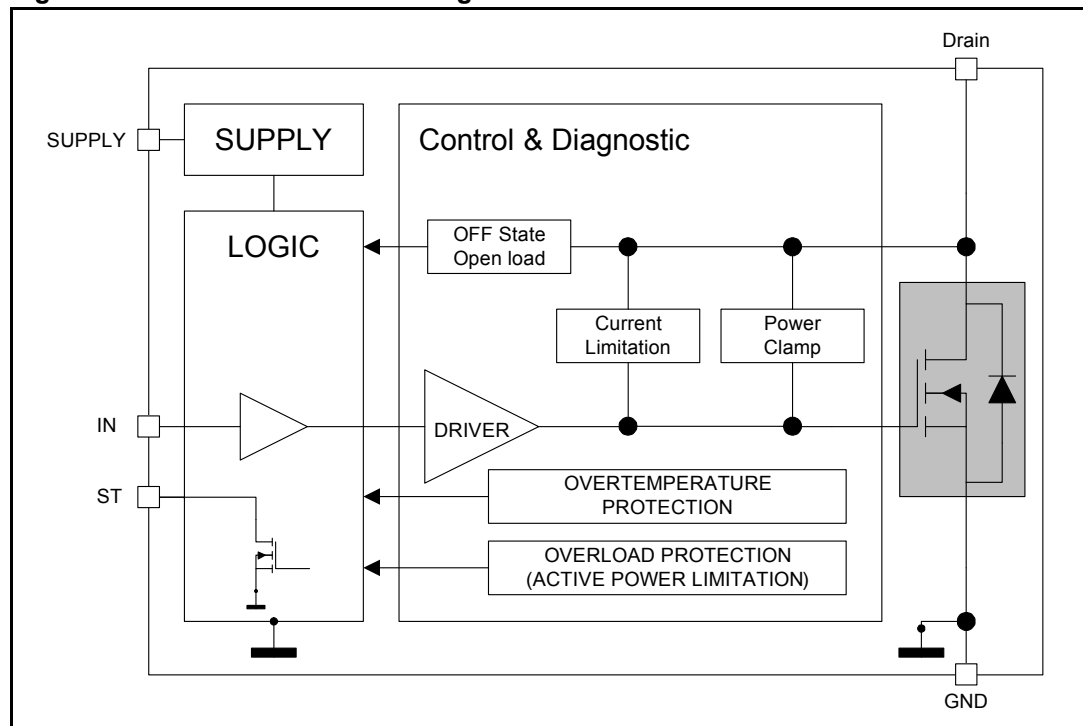


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state ⁽¹⁾
DRAIN	Power MOS drain
SOURCE	Power MOS source and ground reference for the control section
SUPPLY VOLTAGE	Supply voltage connected to the signal part (5 V)
STATUS	Open drain digital diagnostic pin ⁽²⁾

1. Internally connected to V_{supply} in the VNL5050N3-E

2. Valid for VNL5050S5-E only.

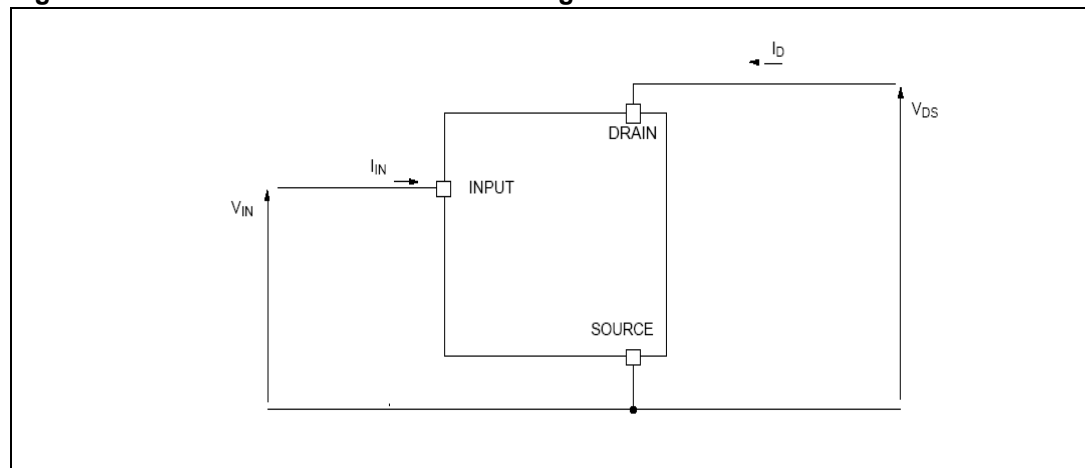
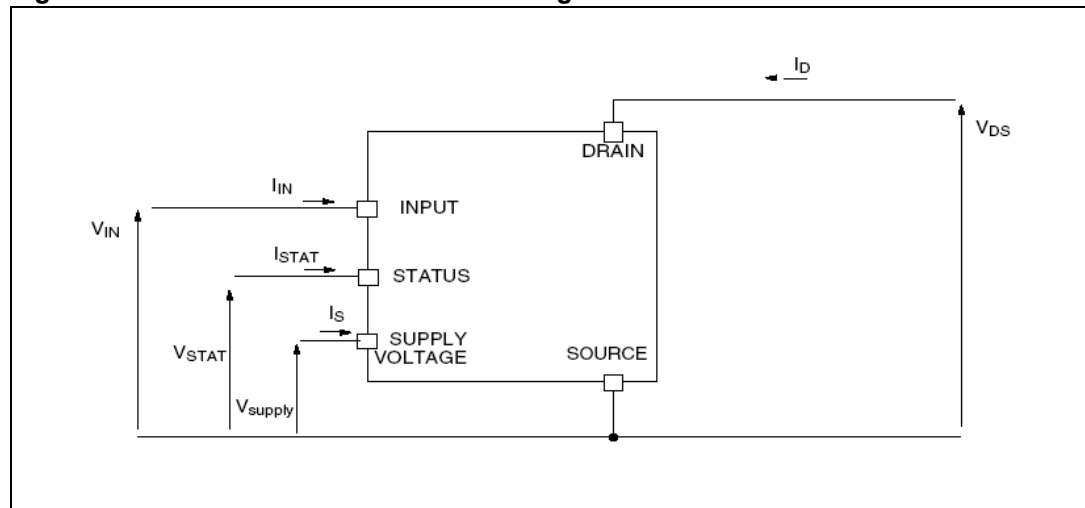
Figure 3. VNL5050N3-E current and voltage conventions**Figure 4. VNL5050S5-E current and voltage conventions**

Figure 5. Configuration diagrams (top view)

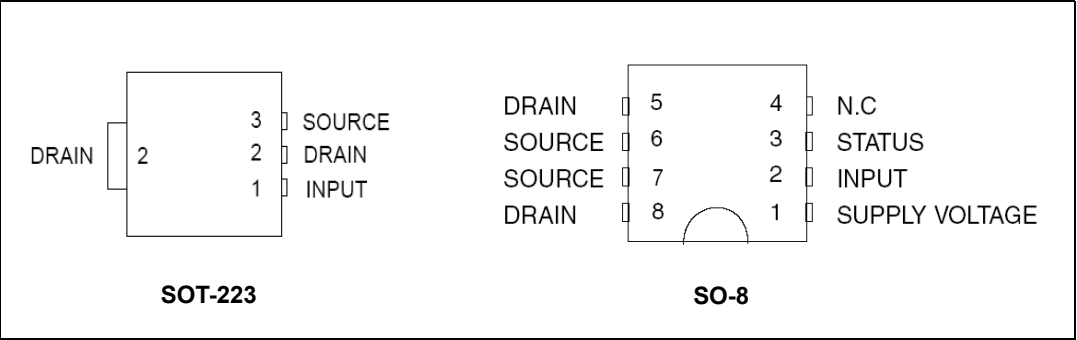


Table 3. Suggested connections for unused and n.c. pins

Connection / pin	STATUS	N.C.	INPUT
Floating	X	X	X
To ground	Not allowed	X	Through 10 kΩ resistor

2 Absolute maximum rating

Stressing the device above the rating listed in the [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document

2.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
V_{DS}	Drain-source voltage ($V_{IN} = 0$ V)	Internally clamped		V
I_D	DC drain current	Internally limited		A
$-I_D$	Reverse DC drain current	-4		A
I_S	DC supply current	-	-1 to 10	mA
I_{IN}	DC input current	-1 to 10		mA
I_{STAT}	DC status current	-	-1 to 10	mA
V_{ESD1}	Electrostatic discharge ($R = 1.5$ k Ω ; $C = 100$ pF) – DRAIN – SUPPLY, INPUT, STATUS	5000 4000		V
V_{ESD2}	Electrostatic discharge on output pin only ($R = 330$ Ω , $C = 150$ pF)	2000		V
T_J	Junction operating temperature	-40 to 150		°C
T_{stg}	Storage temperature	-55 to 150		°C
E_{AS}	Single pulse avalanche energy ($L = 1.1$ mH, $T_J = 150$ °C, $R_L = 0$, $I_{OUT} = I_{limL}$)	93		mJ

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Maximum value		Unit
		SOT-223	SO-8	
$R_{thj-amb}$	Thermal resistance junction-ambient	108.3 ⁽¹⁾	87	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 cm² of Cu (at least 35 μ m thick) connected to all DRAIN pins

3 Electrical characteristics

Values specified in this section are for $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V to } 5.5 \text{ V}$, $-40 \text{ }^{\circ}\text{C} < T_j < 150 \text{ }^{\circ}\text{C}$, unless otherwise stated.

Table 6. Power MOS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{supply}	Operating supply voltage	-	3.5	5	5.5	V
R_{ON}	ON-state resistance	$I_D = 2 \text{ A}$; $T_j = 25 \text{ }^{\circ}\text{C}$, $V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$			50	$\text{m}\Omega$
		$I_D = 2 \text{ A}$; $T_j = 150 \text{ }^{\circ}\text{C}$, $V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$			100	
V_{CLAMP}	Drain-source clamp voltage	$V_{\text{IN}} = 0 \text{ V}$; $I_D = 2 \text{ A}$	41	46	52	V
V_{CLTH}	Drain-source clamp threshold voltage	$V_{\text{IN}} = 0 \text{ V}$; $I_D = 2 \text{ mA}$	36			V
I_{DSS}	OFF-state output current	$V_{\text{IN}} = 0 \text{ V}$; $V_{\text{DS}} = 13 \text{ V}$; $T_j = 25 \text{ }^{\circ}\text{C}$	0		3	μA
		$V_{\text{IN}} = 0 \text{ V}$; $V_{\text{DS}} = 13 \text{ V}$; $T_j = 125 \text{ }^{\circ}\text{C}$	0		5	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	$I_D = 2 \text{ A}$; $V_{\text{IN}} = 0 \text{ V}$	-	0.8	-	V

Table 8. Input section⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ISS}	Supply current from input pin	ON-state: $V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$; $V_{\text{DS}} = 0 \text{ V}$		30	110	μA
V_{ICL}	Input clamp voltage	$I_S = 1 \text{ mA}$	5.5		7	V
		$I_S = -1 \text{ mA}$		-0.7		
V_{INTH}	Input threshold voltage	$V_{\text{DS}} = V_{\text{IN}}$; $I_D = 1 \text{ mA}$	1		3.5	V

1. Valid for VNL5050N3-E option (input and supply pins connected together)

Table 9. Status pin⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{\text{STAT}} = 1 \text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation, $V_{\text{STAT}} = 5 \text{ V}$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation, $V_{\text{STAT}} = 5 \text{ V}$			100	pF

Table 9. Status pin⁽¹⁾ (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{STCL}	Status clamp voltage	I _{STAT} = 1 mA	5.5		7	V
		I _{STAT} = -1 mA		-0.7		

1. Valid for VNL5050S5-E option

Table 10. Logic input⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{IL}	Low-level input voltage	-			0.9	V
I _{IL}	Low-level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	High-level input voltage	-	2.1			V
I _{IH}	High-level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage	-	0.13			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.5		7	V
		I _{IN} = -1 mA		-0.7		

1. Valid for VNL5050S5-E option

Table 11. Openload detection⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{OI}	Openload OFF-state voltage detection threshold	V _{IN} = 0 V	0.6	1.2	1.7	V
t _{d(oloff)}	Delay between INPUT falling edge and STATUS falling edge in openload condition	I _{OUT} = 0 A	45	425	1100	μs

1. Valid for VNL5050S5-E option

Table 12. Supply section⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _S	Supply current	OFF-state: T _j = 25 °C; V _{IN} = V _{DRAIN} = 0 V;		10	25	μA
		ON-state: T _j = 25 °C; V _{IN} = 5 V; V _{DS} = 0 V		25	110	
V _{SCL}	Supply clamp voltage	I _{SCL} = 1 mA	5.5		7	V
		I _{SCL} = -1 mA		-0.7		

1. Valid for VNL5050S5-E option

Table 13. Switching characteristics⁽¹⁾

Symbol	Parameter	Test conditions	SOT-223 ⁽²⁾			SO-8			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on delay time	$R_L = 6.5 \Omega$, $V_{CC} = 13 V^{(3)}$	-	6	-	-	6	-	μs
$t_{d(OFF)}$	Turn-off delay time	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$	-	20	-	-	20	-	μs
t_r	Rise time	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$	-	10	-	-	10	-	μs
t_f	Fall time	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$	-	10	-	-	10	-	μs
W_{ON}	Switching energy losses at turn-on	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$	-	0.04	-	-	0.04	-	mJ
W_{OFF}	Switching energy losses at turn-off	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$	-	0.06	-	-	0.06	-	mJ

1. see [Figure 16: VNL5050N3-E application schematic](#) and [Figure 17: VNL5050S5-E application schematic](#)

2. $3.5 V \leq V_{supply} = V_{IN} \leq 5.5 V$

3. See [Figure 15: Switching characteristics](#)

Table 14. Protection and diagnostics

Symbol	Parameter	Test conditions ⁽¹⁾	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	$V_{DS} = 13 V$; $V_{supply} = V_{IN} = 5 V$	19	27	38	A
I_{limL}	Short-circuit current during thermal cycling	$V_{DS} = 13 V$; $T_R < T_J < T_{TSD}$; $V_{supply} = V_{IN} = 5 V$		11		A
t_{dlimL}	Step response current limit	$V_{DS} = 13 V$; $V_{input} = 5 V$		44		μs
T_{TSD}	Shutdown temperature	-	150	175	200	$^{\circ}C$
$T_R^{(2)}$	Reset temperature	-	$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
$T_{RS}^{(3)}$	Thermal reset of STATUS	-	135			$^{\circ}C$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)	-		7		$^{\circ}C$

1. $V_{supply} = V_{input}$ in VNL5050N3-E version

2. Valid for VNL5050S5-E option

3.1 Electrical characteristics curves

Figure 6. Source diode forward characteristics

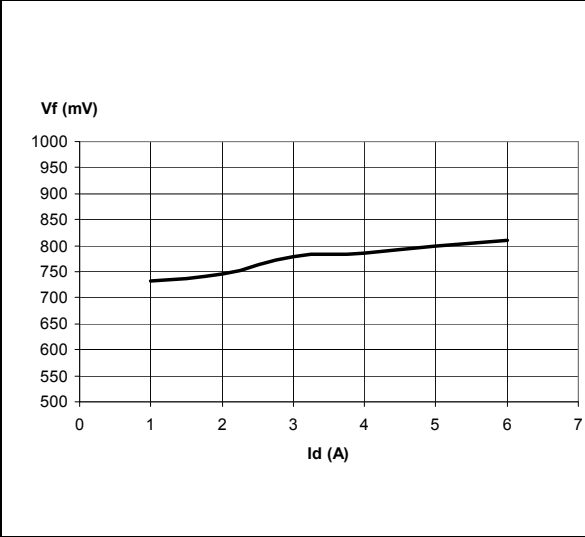


Figure 7. Static drain source on-resistance vs. drain current

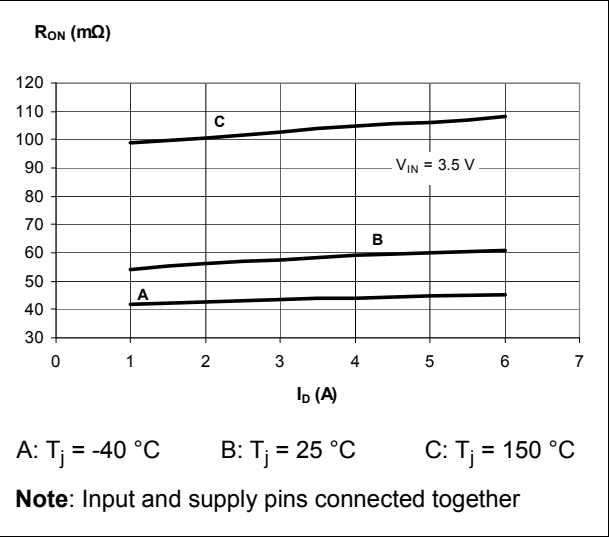


Figure 8. Static drain source on-resistance vs. input voltage

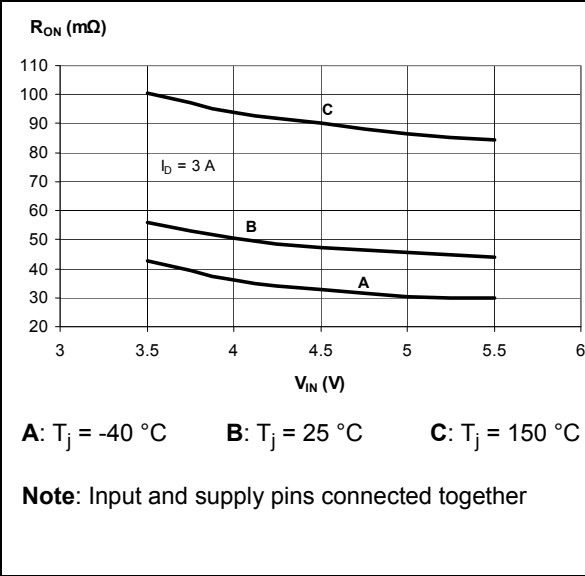


Figure 9. Static drain source on-resistance vs. drain current

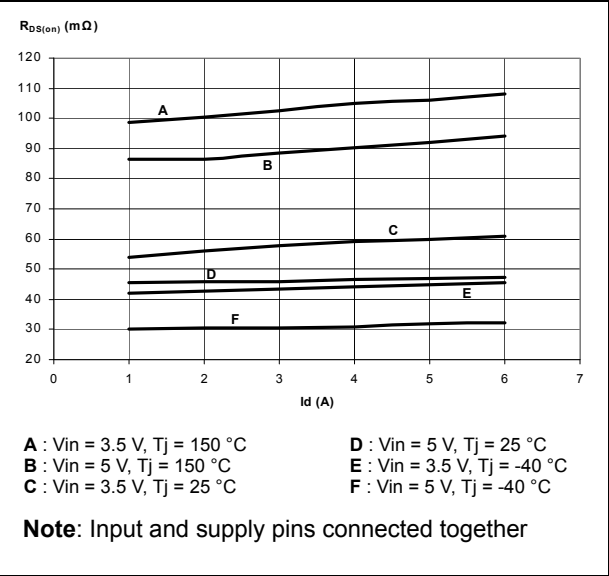


Figure 10. Transfer characteristics

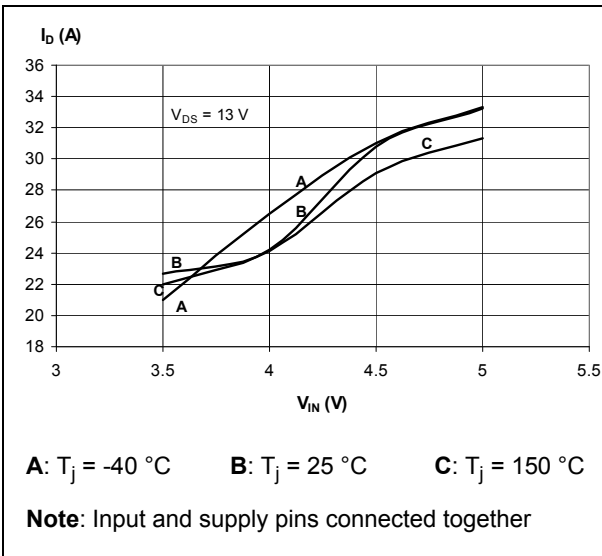


Figure 11. Transfer characteristics (inside view for $V_{IN} = 2\text{ V to }3\text{ V}$)

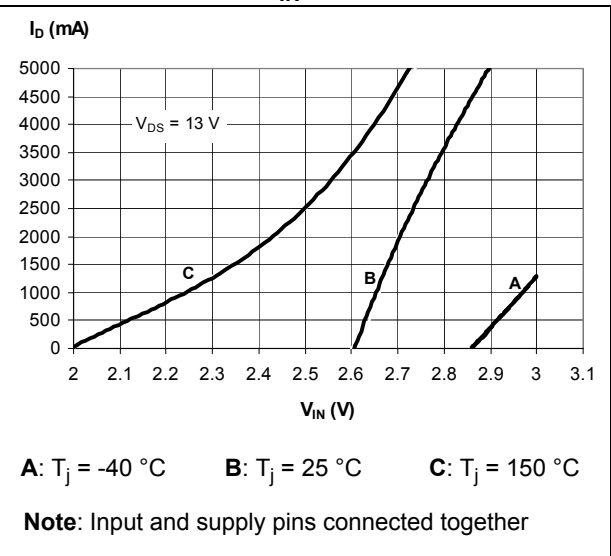


Figure 12. Output characteristics

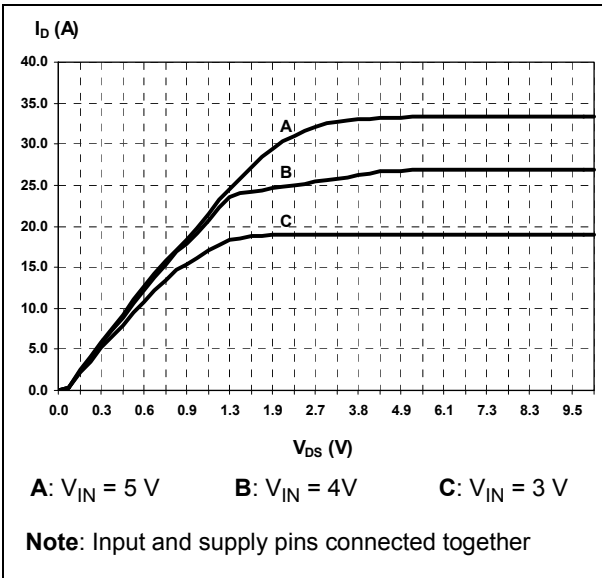


Figure 13. Normalized on-resistance vs. temperature

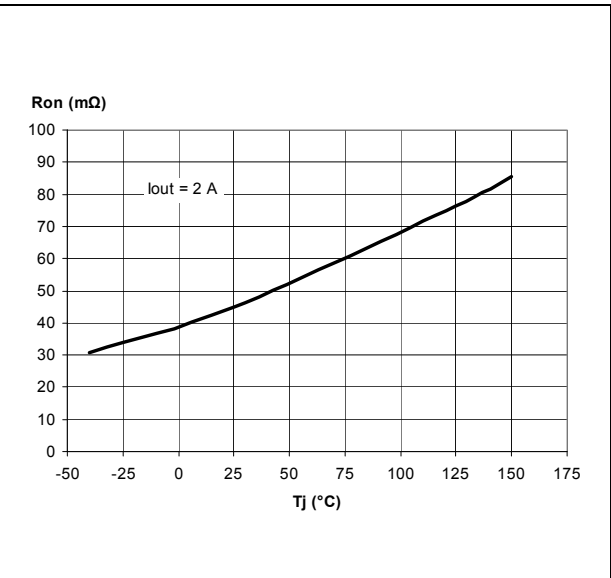


Figure 14. Normalized input threshold vs. temperature

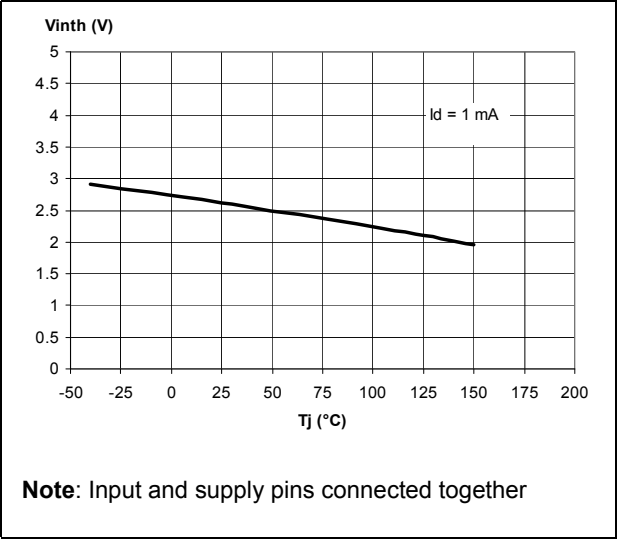


Table 15. Truth table⁽¹⁾

Conditions	INPUT	DRAIN	STATUS
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Overtemperature	L	H	H
	H	H	L
Undervoltage	L	H	X
	H	H	X
Output voltage < V_{OL}	L	L	L
	H	L	H

1. Valid for VNL5050S5-E option

Figure 15. Switching characteristics

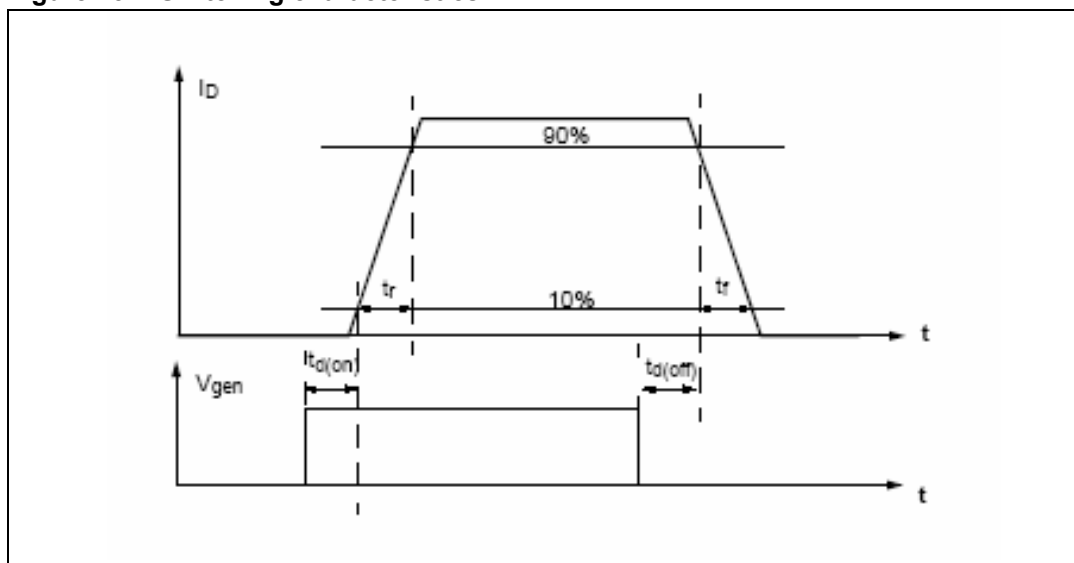


Figure 16. VNL5050N3-E application schematic

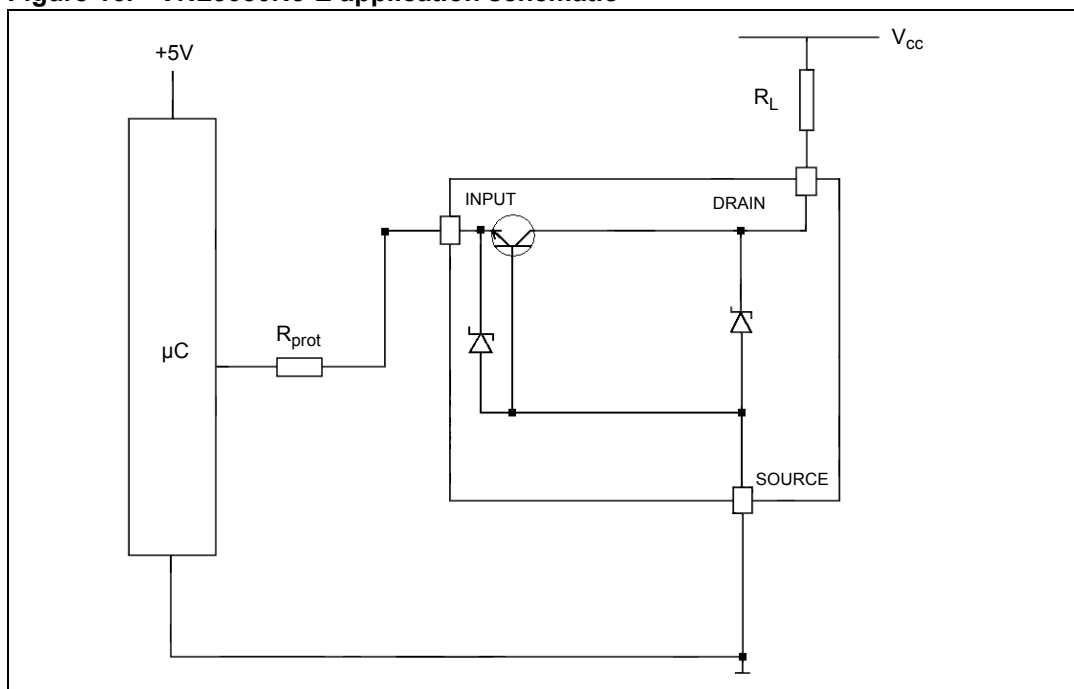
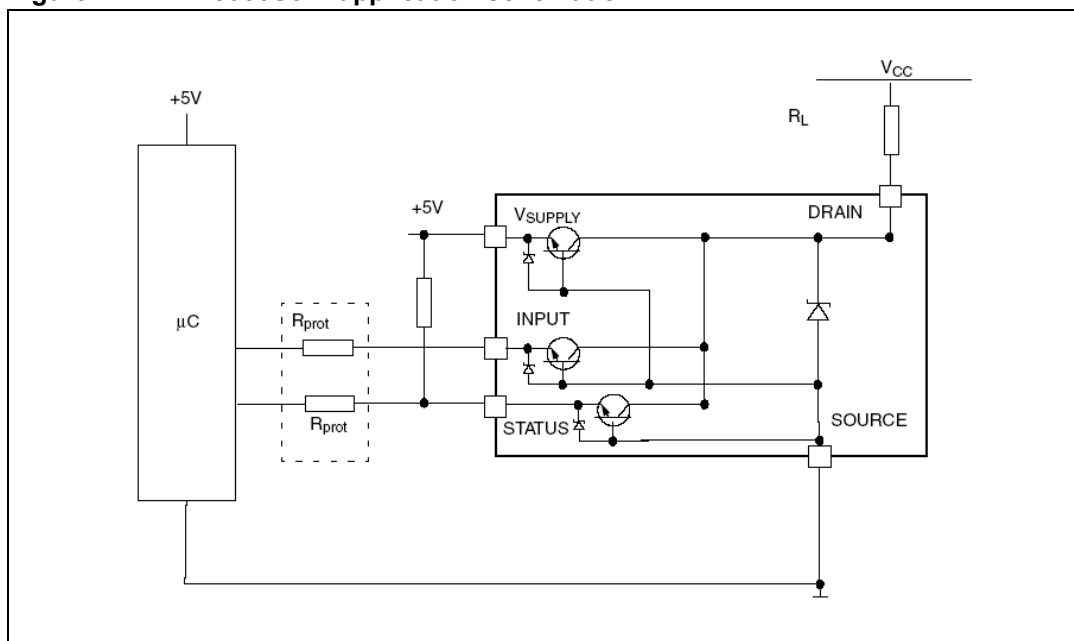


Figure 17. VNL5050S5-E application schematic



3.2 MCU I/O protection

ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up^(a). The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 1

$$\frac{0.7}{I_{\text{latchup}}} \leq R_{\text{prot}} \leq \frac{(V_{\text{OH} \mu\text{C}} - V_{\text{IH}})}{I_{\text{IH max}}}$$

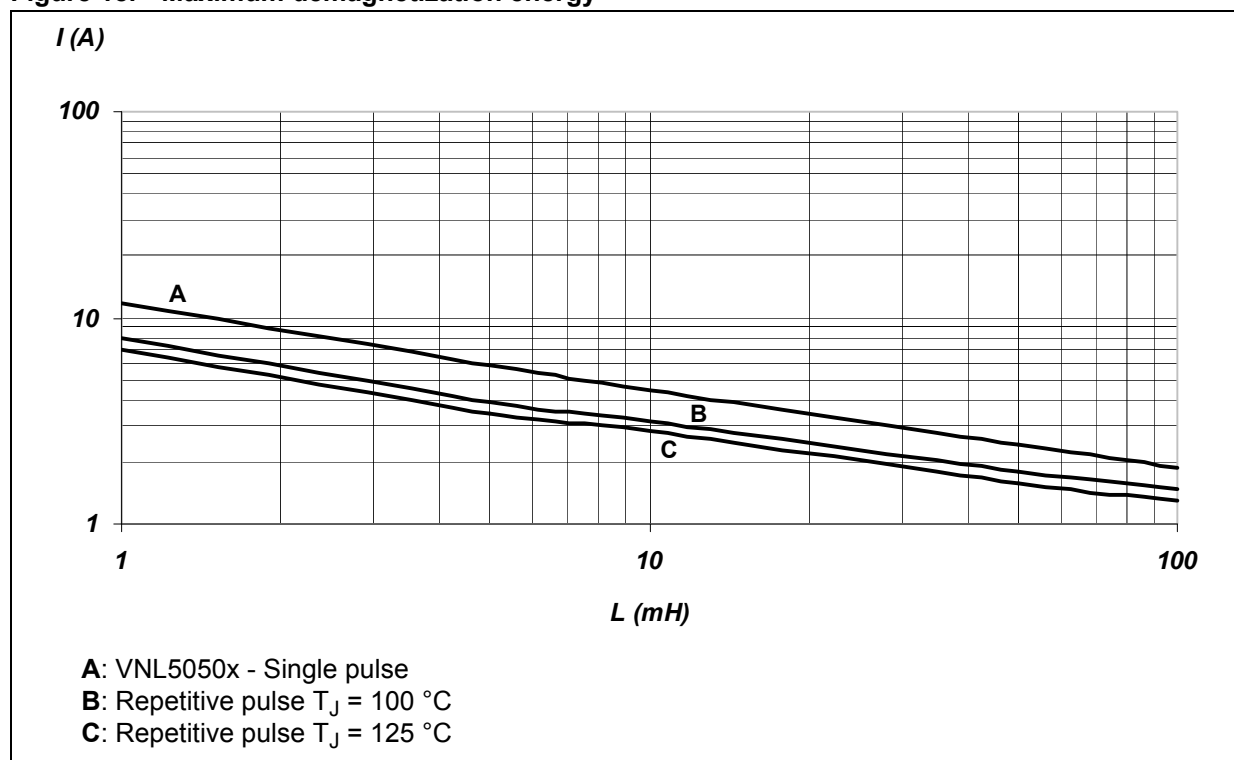
Let:

- ? $I_{\text{latchup}} \geq 20 \text{ mA}$
- ? $V_{\text{OH} \mu\text{C}} \geq 4.5 \text{ V}$
- ? $35 \Omega \leq R_{\text{prot}} \leq 100 \text{ K}\Omega$

Then, the recommended value is $R_{\text{prot}} = 10 \text{ K}\Omega$

[Figure 18](#) shows the turn-off current drawn during the demagnetization.

Figure 18. Maximum demagnetization energy⁽¹⁾



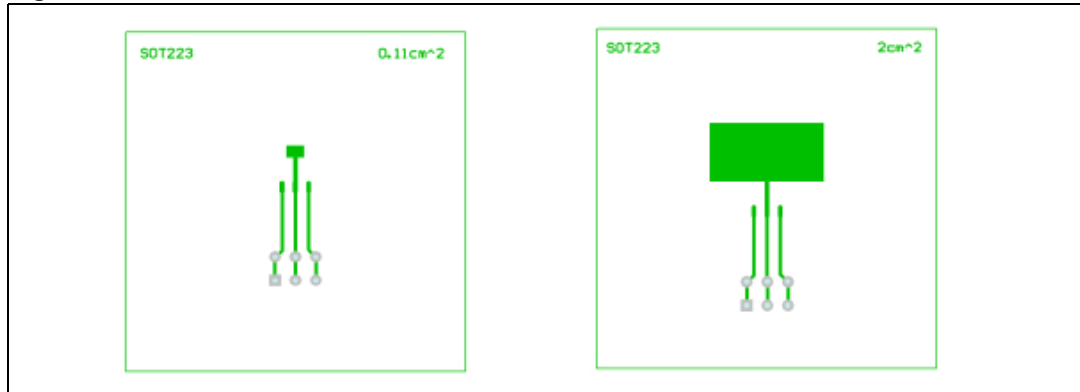
1. The voltage supply is $V_{\text{CC}} = 13.5 \text{ V}$

a. In case of negative transient on the drain pin

4 Package and PC board thermal data

4.1 SOT-223 thermal data

Figure 19. SOT-223 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 30 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, copper areas: from minimum pad lay-out to 0.8 cm²).

Figure 20. $R_{thj-amb}$ vs. PCB copper area in open box free air condition

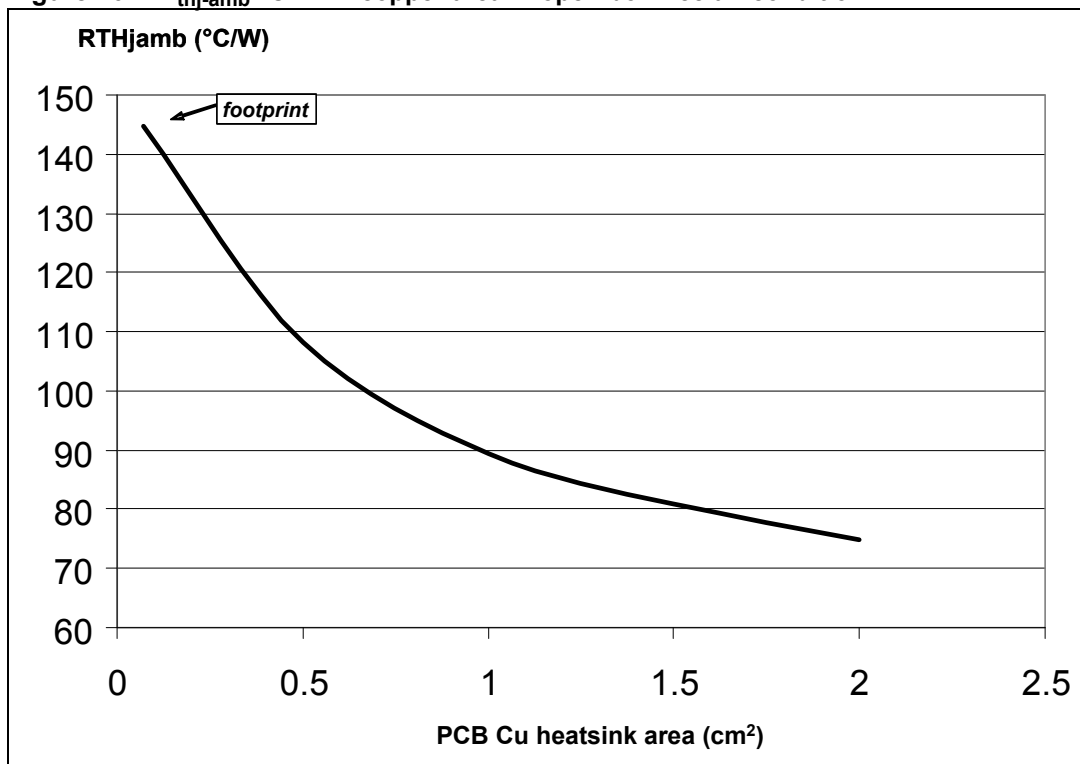
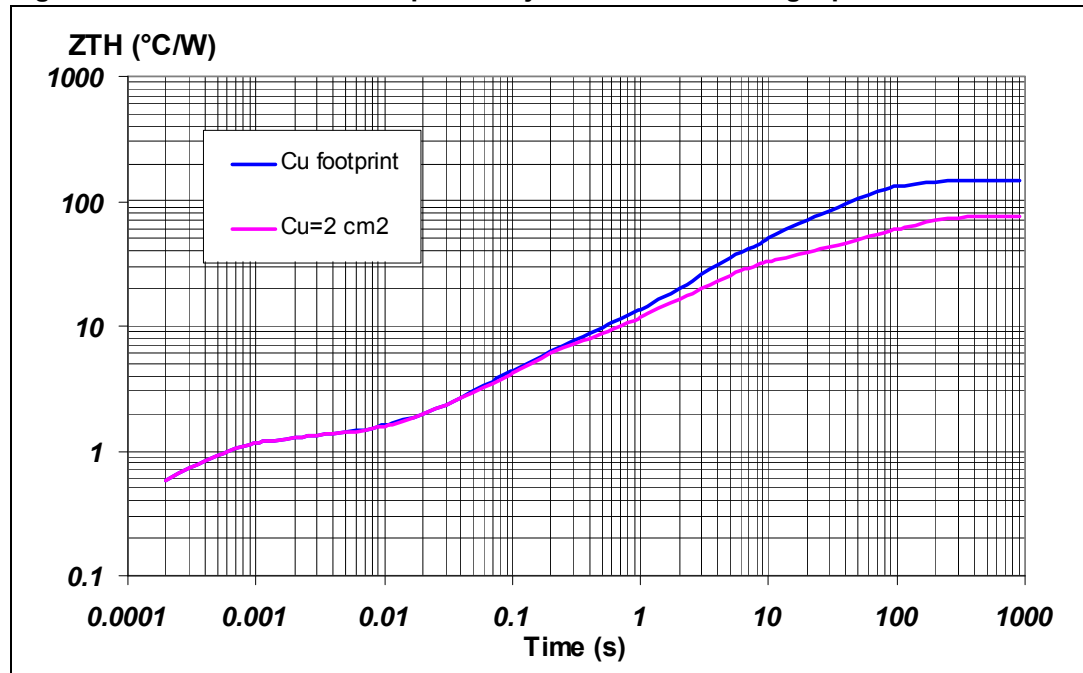


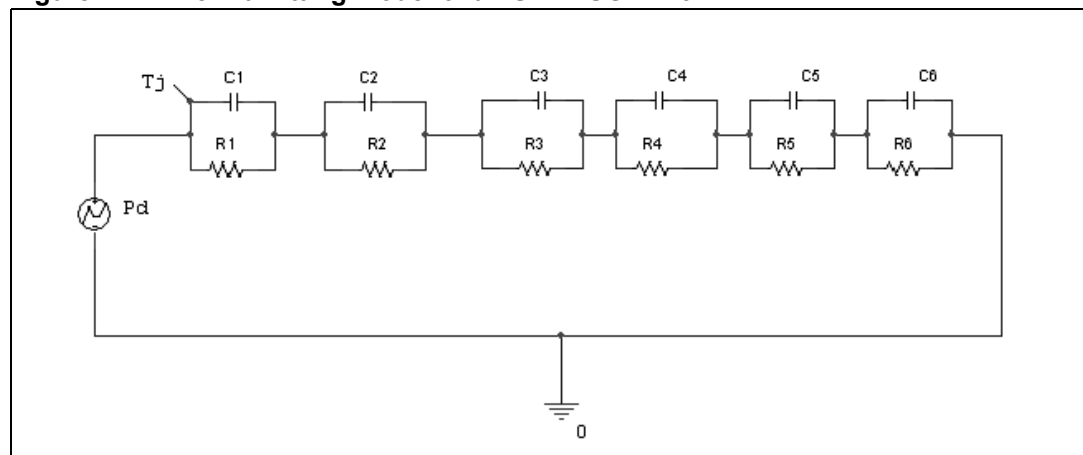
Figure 21. SOT-223 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 22. Thermal fitting model of a LSD in SOT-223⁽¹⁾

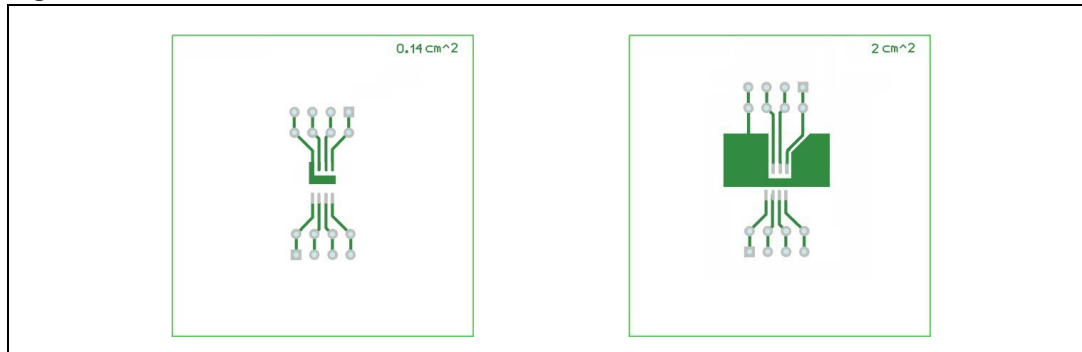
1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. Thermal parameters

Area/island (cm ²)	Footprint	2
R1 (°C/W)	0.4	
R2 (°C/W)	0.8	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	115	45
C1 (W.s/°C)	0.00006	
C2 (W.s/°C)	0.0005	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.16	
C5 (W.s/°C)	1000	
C6 (W.s/°C)	0.4	2

4.2 SO-8 thermal data

Figure 23. SO-8 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m (front and back side), Copper areas: from minimum pad lay-out to 2 cm²).

Figure 24. $R_{thj-amb}$ vs. PCB copper area in open box free air condition

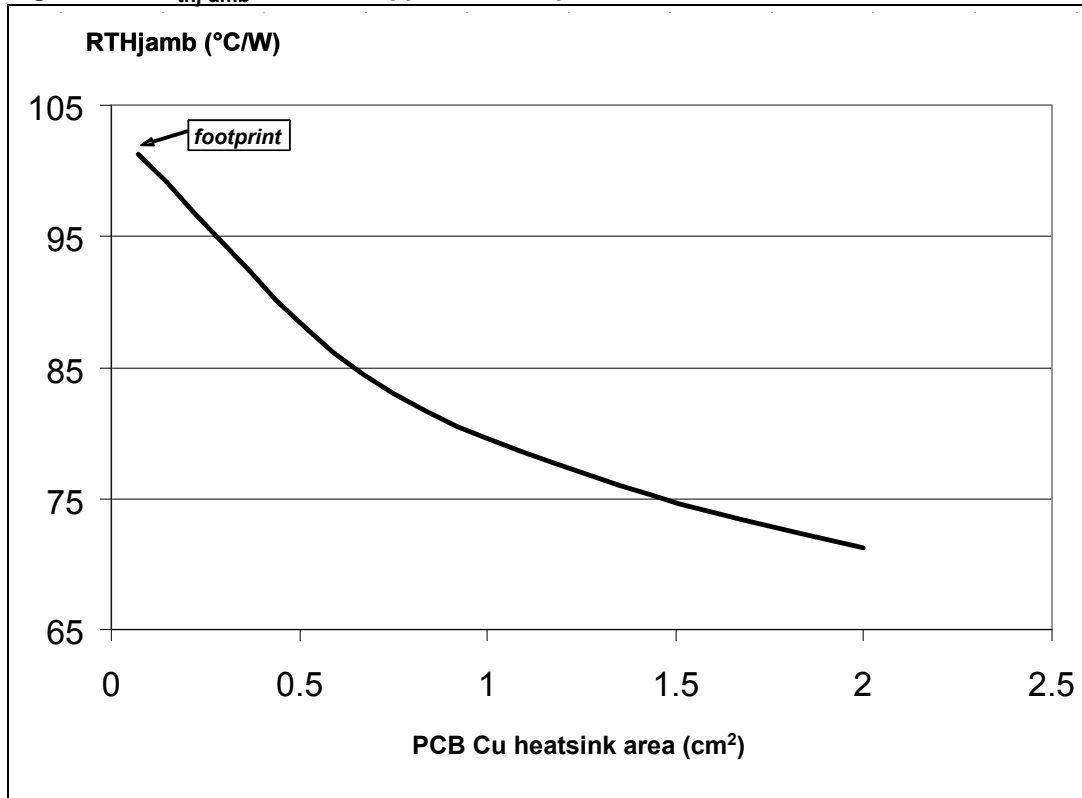
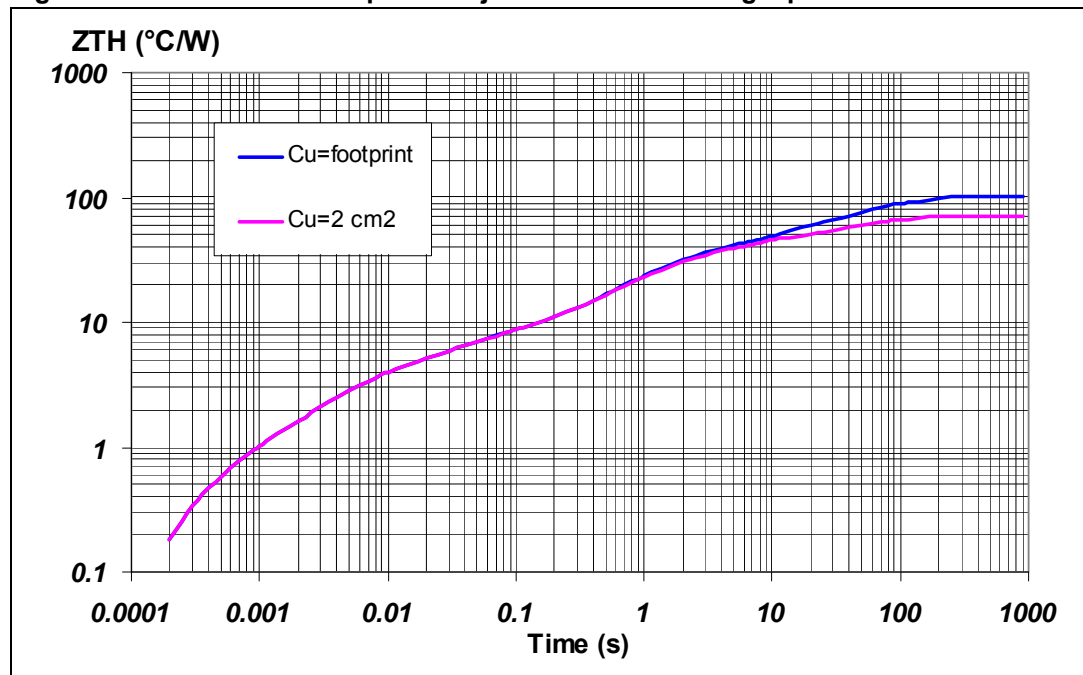
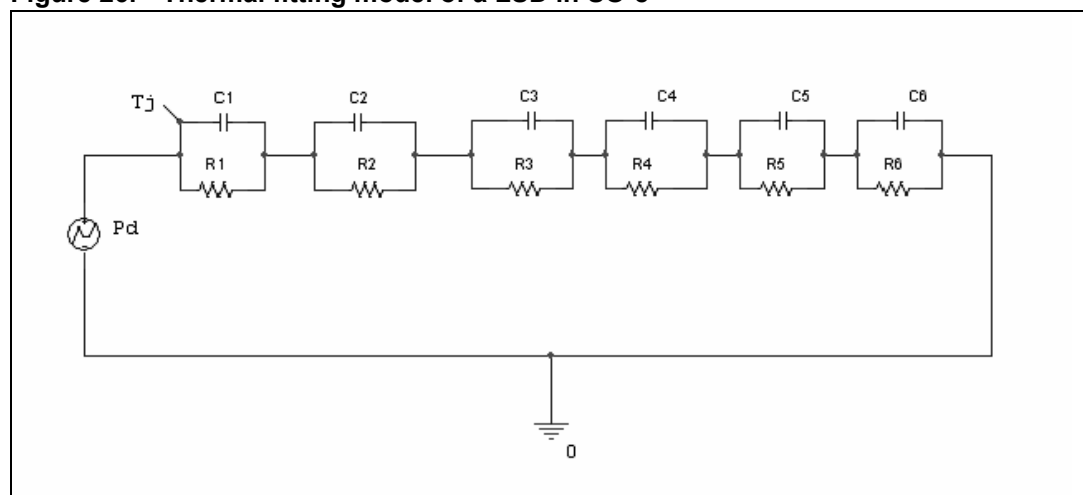


Figure 25. SO-8 thermal impedance junction ambient single pulse**Equation 3: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 26. Thermal fitting model of a LSD in SO-8⁽¹⁾

1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. Thermal parameters

Area/island (cm ²)	Footprint	2
R1 (°C/W)	0.4	
R2 (°C/W)	2.4	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.00008	
C2 (W.s/°C)	0.0016	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SOT-223 mechanical data

Figure 27. SOT-223 package dimensions

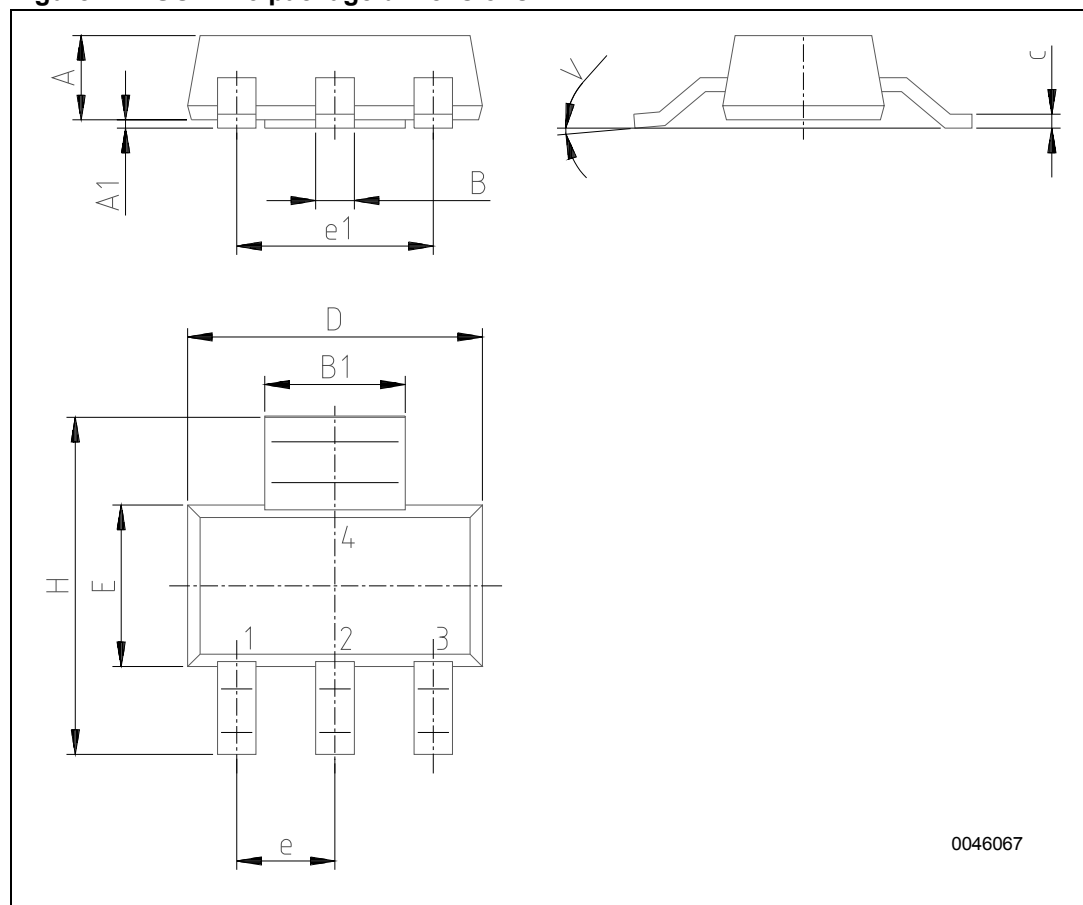


Table 18. SOT-223 mechanical data

DIM.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.8			0.071
B	0.6	0.7	0.85	0.024	0.027	0.033
B1	2.9	3	3.15	0.114	0.118	0.124
c	0.24	0.26	0.35	0.009	0.01	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
e		2.3			0.09	
e1		4.6			0.181	
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.276	0.287
V	10 (max)					
A1	0.02		0.1	0.0008		0.004

5.3 SO-8 mechanical data

Figure 28. SO-8 package dimensions

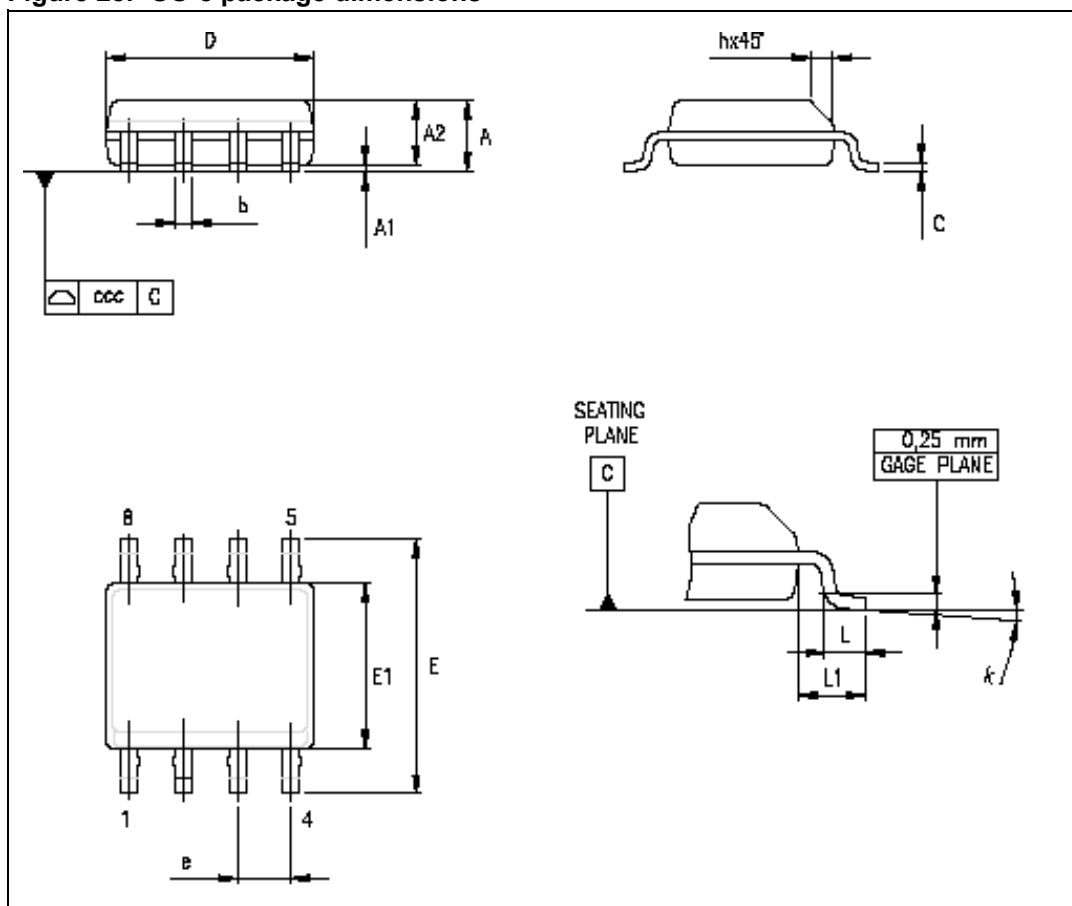


Table 19. SO-8 mechanical data

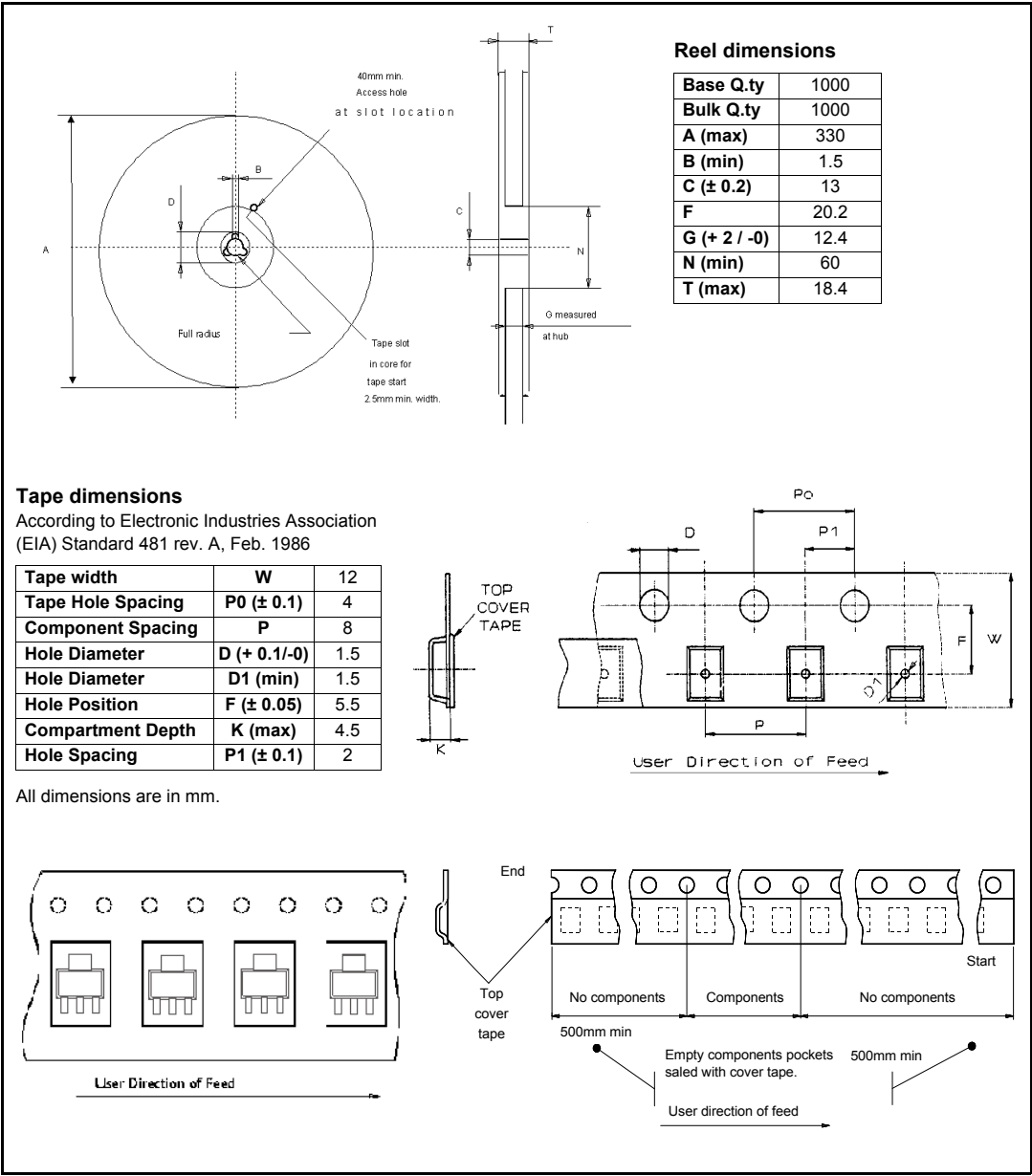
Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.4 SOT-223 packing information

The devices can be packed in tube or tape and reel shipments (see the [Table 1: Devices summary on page 1](#)).

Figure 29. SOT-223 tape and reel shipment (suffix “TR”)



5.5 SO-8 packing information

Figure 30. SO-8 tube shipment (no suffix)

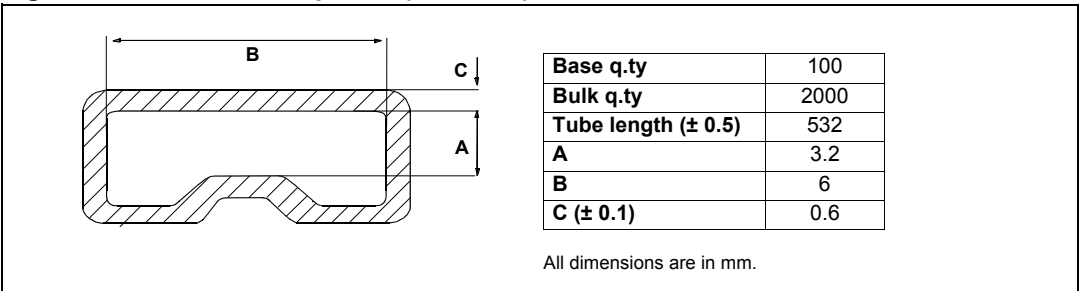
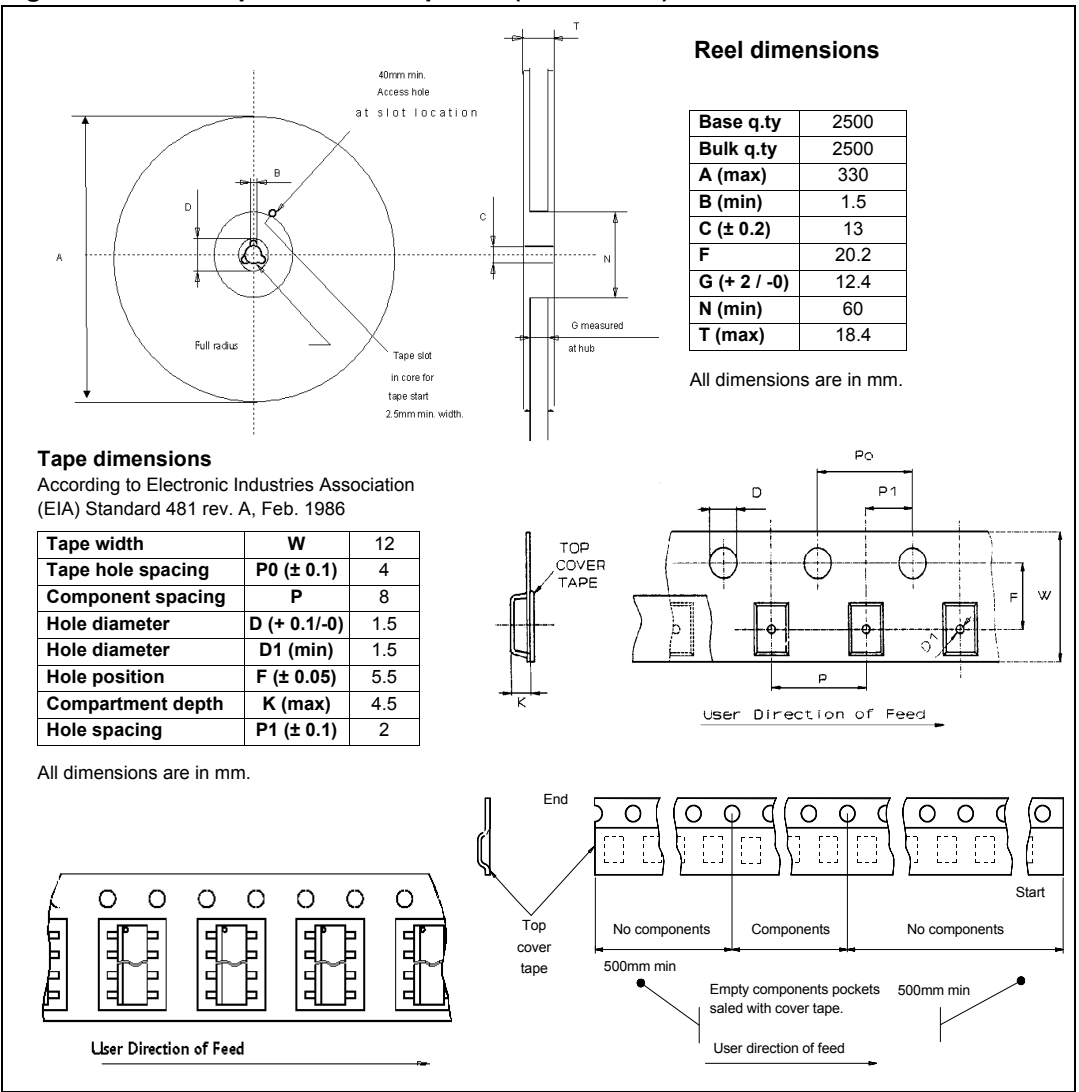


Figure 31. SO-8 tape and reel shipment (suffix “TR”)



6 Revision history

Table 20. Document revision history

Date	Revision	Changes
9-Jan-2008	1	Initial release.
25-Jun-2009	2	Updated corporate template from V2 to V3 Table 3: Suggested connections for unused and n.c. pins – V_{ESD1}: updated parameter and value – V_{ESD2}: changed value Table 4: Absolute maximum ratings – R_{thj-case}: deleted max value for SO-8 – R_{thj-amb}: added max value for both SOT-223 and SO-8 Table 7: Source drain diode – V_{SD}: added typ value Table 8: Input section. – V_{ICL}: added min/max value for I_S = 1 mA – V_{INTH}: added min/max value Table 9: Status pin – V_{STCL}: added max value for I_{STAT} = 1 mA Table 10: Logic input – V_{ICL}: added max value for I_N = 1 mA Table 12: Supply section – I_S: changed unit of measurement for ON-state. – V_{VSL}: added max value for I_{STAT} = 1 mA Table 13: Switching characteristics – t_{d(OFF)}: changed typ value both for SOT-223 and SO-8 – W_{ON}: added typ value for SO-8 – W_{OFF}: added typ value for SO-8 – Added all typ column for SOT-223 Table 14: Protection and diagnostics – I_{limL}: changed typ value – t_{dlimL}: changed typ value – Deleted row T_R valid for VNL5050N3-E option Added Figure 6: Source diode forward characteristics Added Figure 7: Static drain source on-resistance vs. drain current Added Figure 8: Static drain source on-resistance vs. input voltage Added Figure 9: Static drain source on-resistance vs. drain current Added Figure 10: Transfer characteristics Added Figure 11: Output characteristics Added Figure 12: Output characteristics Added Figure 13: Normalized on-resistance vs. temperature Added Chapter 4: Package and PC board thermal data

Table 20. Document revision history (continued)

Date	Revision	Changes
25-Jun-2009	2 (continued)	Deleted table 25: SOT-223 mechanical data & package outline Added Figure 27: SOT-223 package dimensions Added Table 18: SOT-223 mechanical data Deleted table 26: SO-8 mechanical data & package outline Added Figure 28: SO-8 package dimensions Added Table 19: SO-8 mechanical data
19-Aug-2009	3	Updated corporate template from V3 to V3-1 Deleted row for $R_{thj-case}$ in Table 5: Thermal data
20-Nov-2009	4	Changed the document title Took the first line off the bullet list for Features on cover page Table 4: Absolute maximum ratings – E_{AS} : added new row Table 6: Power MOS section – V_{supply} : added new row – R_{ON} : updated test conditions Table 8: Input section. – I_{SS} : updated test conditions – Updated the table footnote Table 13: Switching characteristics – Moved footnote 2 and changed its text – W_{ON} : changed typ value – W_{OFF} : changed typ value Table 14: Protection and diagnostics – I_{limH} : updated test conditions – I_{limL} : updated test conditions – t_{dlimL} : changed typ value Updated Figure 7: Static drain source on-resistance vs. drain current Updated Figure 8: Static drain source on-resistance vs. input voltage Updated Figure 9: Static drain source on-resistance vs. drain current Updated Figure 10: Transfer characteristics Added Figure 11: Transfer characteristics (inside view for $V_{IN} = 2\text{ V}$ to 3 V) Updated Figure 14: Normalized input threshold vs. temperature Added Section 3.2: MCU I/O protection
19-Sep-2013	5	Updated Disclaimer.

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