TSV912H, TSV912AH

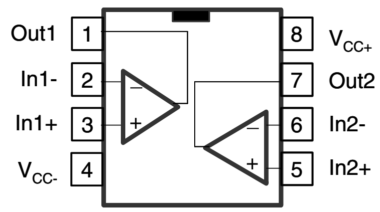
High temperature rail-to-rail input/output 8 MHz operational amplifiers

Features

- Rail-to-rail input and output
- Wide bandwidth
- Low power consumption: 820 µA typ
- Unity gain stability
- High output current: 35 mA
- Operating range from 2.5 to 5.5 V
- Low input bias current, 1 pA typ
- ESD internal protection ≥ 5 kV
- Latch-up immunity

Pin connections
(top view)

SO-8



Applications

- Automotive products

Description

The TSV912H and TSV912AH operational amplifiers offer low voltage operation and rail-to-rail input and output.

The devices feature an excellent speed/power consumption ratio, offering an 8 MHz gain-bandwidth product while consuming only 1.1 mA maximum at 5 V. They are unity gain stable and feature an ultra-low input bias current.

The TSV912H is a high temperature version of the TSV912, and can operate from -40°C to +150°C with unique characteristics. Its main target applications are automotive, but the device is also ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage[1] (V_{CC+} - V_{CC-})	6	V
V_{id}	Differential input voltage [2]	$\pm V_{CC}$	V
V_{in}	Input voltage [3]	V_{CC-} -0.2 to V_{CC+} +0.2	V
I_{in}	Input current [4]	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient[5] [6] SO-8	125	°C/W
R_{thjc}	Thermal resistance junction to case[5] [6] SO-8	40	°C/W
T_j	Maximum junction temperature	160	°C
ESD	HBM: human body model[7]	5	kV
	MM: machine model[8]	400	V
	CDM: charged device model[9]	1500	V
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC}-V_{in} must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
8. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
9. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{CC+} - V_{CC-})	2.5 to 5.5	V
V_{icm}	Common mode input voltage range	V_{CC-} -0.1 to V_{CC+} +0.1	V
T_{oper}	Operating free-air temperature range	-40 to +150	°C

2 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = +2.5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, R_L connected to V_{CC}/2, T = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	TSV912H, T=25°C TSV912H, T_{min} < T < T_{max}		0.1	4.5 7.5	mV
		TSV912AH, T=25°C TSV912AH, T_{min} < T < T_{max}			1.5 3	
DV_{io}/DT	Input offset voltage drift	-40°C < T < +125°C +125°C < T < +150°C		2 20		µV/°C
I_{io}	Input offset current	V_{out} =V_{CC}/2 T=25°C T_{min} < T < T_{max}		1	10(1) 5	pA nA
I_{ib}	Input bias current	V_{out} =V_{CC}/2 T=25°C T_{min} < T < T_{max}		1	10(1) 5	pA nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0V to 2.5V, V_{out} = 1.25V T=25°C T_{min} < T < T_{max}	58 53	75		dB
A_{vd}	Large signal voltage gain	R_L= 10kΩ, V_{out} = 0.5V to 2V T=25°C T_{min} < T < T_{max}	80 70	89		dB
V_{CC}-V_{OH}	High level output voltage	R_L = 10kΩ, T=25°C R_L = 10kΩ, T_{min} < T < T_{max} R_L = 600Ω, T=25°C R_L = 600Ω, T_{min} < T < T_{max}		15 45	40 60 150 250	mV
V_{OL}	Low level output voltage	R_L = 10kΩ, T=25°C R_L = 10kΩ, T_{min} < T < T_{max} R_L = 600Ω, T=25°C R_L = 600Ω, T_{min} < T < T_{max}		15 45	40 60 150 250	mV
I_{out}	I_{sink}	V_{out} = 2.5V T=25°C T_{min} < T < T_{max}	18 14	32		mA
	I_{source}	V_{out} = 0V T=25°C T_{min} < T < T_{max}	18 14	35		
I_{CC}	Supply current (per operator)	No load, V_{out} =V_{CC}/2 T=25°C T_{min} < T < T_{max}		0.78	1.1 1.1	mA
AC performance						
GBP	Gain bandwidth product	R_L= 2kΩ, C_L=100pF, f =100kHz T=25°C T_{min} < T < T_{max}		8 4		MHz

Table 3. Electrical characteristics at V_{CC+} = +2.5 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, R_L connected to $V_{CC}/2$, T = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_u	Unity gain frequency	R_L= 2kΩ, C_L= 100pF		7.2		MHz
ϕm	Phase margin	R_L= 2kΩ, C_L= 100pF		45		Degrees
G_m	Gain margin	R_L= 2kΩ, C_L= 100pF		8		dB
SR	Slew rate	R_L= 2kΩ, C_L=100pF, A_v=1 T=25°C T_{min} < T < T_{max}		4.5 3.5		V/μs
e_n	Equivalent input noise voltage	f= 10kHz		21		$\frac{nV}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion	G=1, f=1kHz, R_L=2kΩ, Bw= 22kHz, V_{icm}=(V_{CC}+1)/2, V_{out}=1.1V_{pp}		0.001		%

1. Guaranteed by design.

Table 4. Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, R_L connected to $V_{CC}/2$, T = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	TSV912H, T=25°C TSV912H, T_{min} < T < T_{max}		0.1	4.5 7.5	mV
		TSV912AH, T=25°C TSV912AH, T_{min} < T < T_{max}			1.5 3	
DV_{io}	Input offset voltage drift	-40°C < T < +125°C +125°C < T < +150°C		2 20		μV/°C
I_{io}	Input offset current	V_{out} =V_{CC}/2 T=25°C T_{min} < T < T_{max}		1	10(1) 5	pA nA
I_{ib}	Input bias current	V_{out} =V_{CC}/2 T=25°C T_{min} < T < T_{max}		1	10(1) 5	pA nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0V to 3.3V, V_{out} = 1.65V T=25°C T_{min} < T < T_{max}	60 55	78		dB
A_{vd}	Large signal voltage gain	R_L=10kΩ, V_{out} = 0.5V to 2.8V T=25°C T_{min} < T < T_{max}	80 70	90		dB
V_{CC}-V_{OH}	High level output voltage	R_L = 10kΩ, T=25°C R_L = 10kΩ, T_{min} < T < T_{max} R_L = 600Ω, T=25°C R_L = 600Ω, T_{min} < T < T_{max}		15 45 	40 60 150 250	mV

Table 4. Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, R_L connected to V_{CC}/2, T = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	R_L = 10kΩ, T=25°C R_L = 10kΩ, T_{min} < T < T_{max} R_L = 600Ω, T=25°C R_L = 600Ω, T_{min} < T < T_{max}		15 45	40 60 150 250	mV
I_{out}	I_{sink}	V_{out} = 3.3V T=25°C T_{min} < T < T_{max}	18 14	32		mA
	I_{source}	V_{out} = 0V T=25°C T_{min} < T < T_{max}	18 14	35		
I_{CC}	Supply current (per operator)	No load, V_{out} =V_{CC}/2 T=25°C T_{min} < T < T_{max}		0.8	1.1 1.1	mA
AC performance						
GBP	Gain bandwidth product	R_L= 2kΩ, C_L= 100pF, f = 100kHz, T=25°C T_{min} < T < T_{max}		8 4.2		MHz
F_u	Unity gain frequency	R_L= 2kΩ, C_L=100pF		7.2		MHz
ϕm	Phase margin	R_L= 2kΩ, C_L=100pF		45		Degrees
G_m	Gain margin	R_L= 2kΩ, C_L=100pF		8		dB
SR	Slew rate	R_L= 2kΩ, C_L= 100pF, A_v=1, T=25°C T_{min} < T < T_{max}		4.5 3.5		V/µs
e_n	Equivalent input noise voltage	f= 10kHz		21		$\frac{nV}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion	G=1, f=1kHz, R_L=2kΩ, BW= 22kHz, V_{icm}=(V_{CC}+1)/2, V_{out} =1.9V_{pp},		0.0007		%

1. Guaranteed by design.

Table 5. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, R_L connected to V_{CC}/2, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	TSV912H, T=25°C TSV912H, $T_{min} < T < T_{max}$		0.1	4.5 7.5	mV
		TSV912AH, T=25°C TSV912AH, $T_{min} < T < T_{max}$			1.5 3	
DV_{io}	Input offset voltage drift	-40°C < T < +125°C +125°C < T < +150°C		2 20		µV/°C
I_{io}	Input offset current	V_{out} =V_{CC}/2 T=25°C $T_{min} < T < T_{max}$		1	10[1] 5	pA nA
I_{ib}	Input bias current	V_{out} =V_{CC}/2 T=25°C $T_{min} < T < T_{max}$		1	10[1] 5	pA nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0V to 5V, V_{out} = 2.5V T=25°C $T_{min} < T < T_{max}$	62 58	82		dB
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 2.5 to 5V T=25°C $T_{min} < T < T_{max}$	70 65	86		dB
A_{vd}	Large signal voltage gain	R_L=10kΩ, V_{out}= 0.5V to 4.5V T=25°C $T_{min} < T < T_{max}$	80 70	91		dB
V_{CC}-V_{OH}	High level output voltage	R_L = 10kΩ, T=25°C R_L = 10kΩ, $T_{min} < T < T_{max}$ R_L = 600Ω, T=25°C R_L = 600Ω, $T_{min} < T < T_{max}$		15 45	40 60 150 250	mV
V_{OL}	Low level output voltage	R_L = 10kΩ, T=25°C R_L = 10kΩ, $T_{min} < T < T_{max}$ R_L = 600Ω, T=25°C R_L = 600Ω, $T_{min} < T < T_{max}$		15 45	40 60 150 250	mV
I_{out}	I_{sink}	V_{out} = 5V T=25°C $T_{min} < T_{op} < T_{max}$	18 14	32		mA
	I_{source}	V_{out} = 0V T=25°C $T_{min} < T_{op} < T_{max}$	18 14	35		
I_{CC}	Supply current (per operator)	No load, V_{out}= 2.5V T=25°C $T_{min} < T_{op} < T_{max}$		0.82	1.1 1.1	mA

Table 5. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L= 2kΩ, C_L= 100pF, f = 100kHz T=25°C $T_{min} < T_{op} < T_{max}$		8 4.5		MHz
F_u	Unity gain frequency	R_L = 2kΩ, C_L=100pF		7.5		MHz
ϕm	Phase margin	R_L = 2kΩ, C_L=100pF		45		Degrees
G_m	Gain margin	R_L = 2kΩ, C_L=100pF		8		dB
SR	Slew rate	R_L= 2kΩ, C_L= 100pF, A_V = 1 T=25°C $T_{min} < T_{op} < T_{max}$		4.5 3.5		V/μs
e_n	Equivalent input noise voltage	f=1kHz f=10kHz		27 21		$\frac{nV}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion	G=1, f=1kHz, R_L=2kΩ, Bw= 22kHz, $V_{icm}=(V_{CC}+1)/2$, V_{out} =3.6V_{pp}		0.0004		%

1. Guaranteed by design.

Figure 1. Input offset voltage distribution at T = 25° C

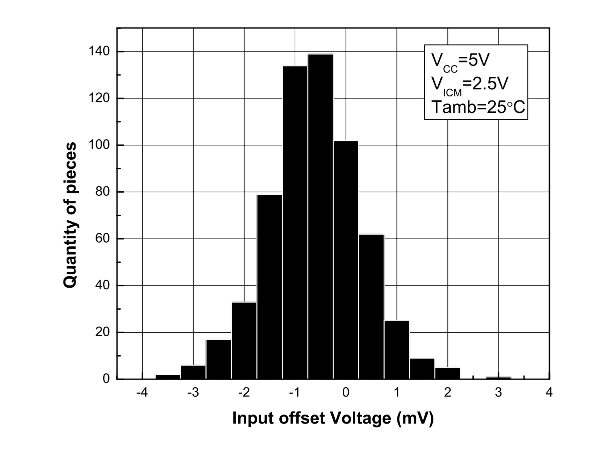


Figure 2. Input offset voltage distribution at T = 150° C

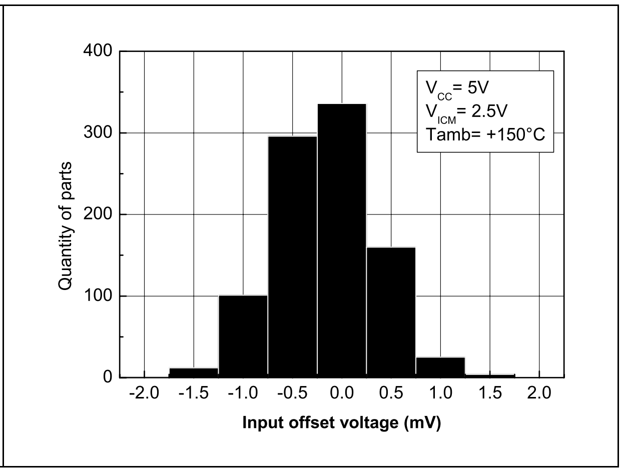


Figure 3. Supply current vs. input common-mode voltage at V_{CC} = 2.5 V

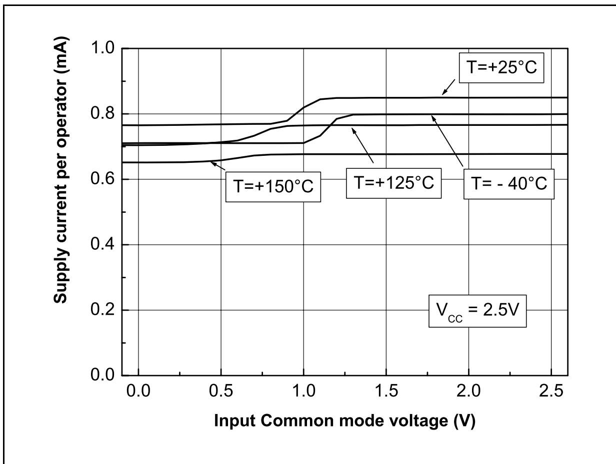


Figure 4. Supply current vs. input common-mode voltage at V_{CC} = 5 V

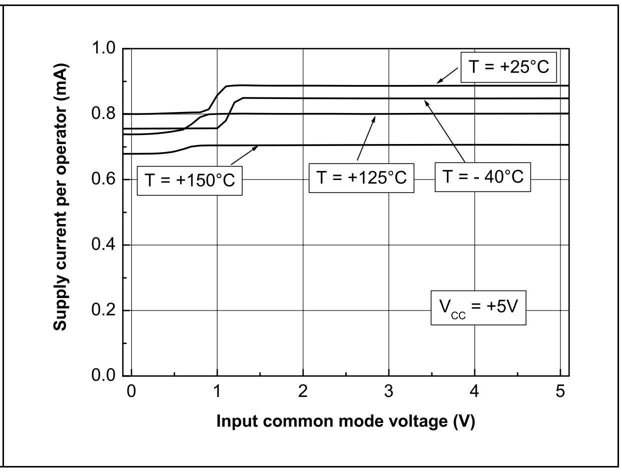


Figure 5. Output current vs. output voltage at V_{CC} = 2.5 V

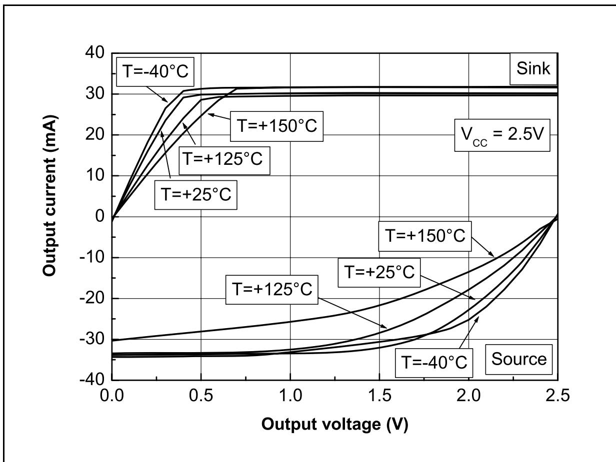


Figure 6. Output current vs. output voltage at V_{CC} = 5 V

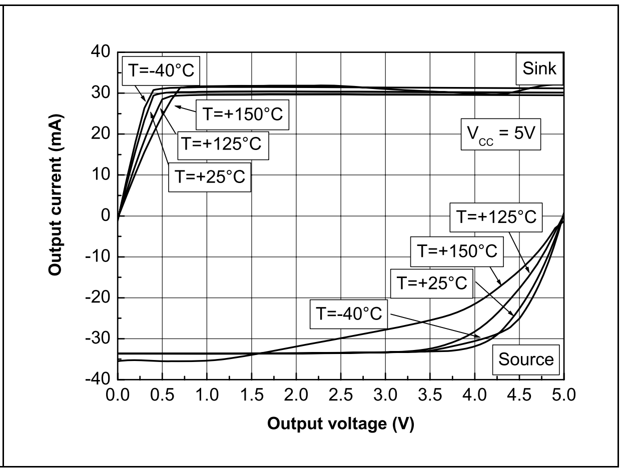


Figure 7. Voltage gain and phase vs frequency at V_{CC} = 2.5 V and V_{icm} = 0.5 V

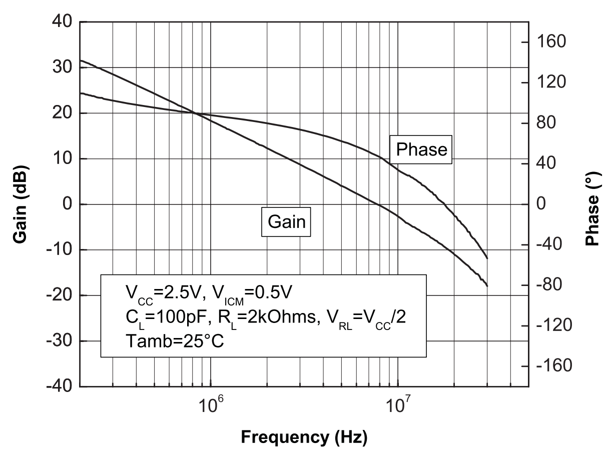


Figure 8. Voltage gain and phase vs frequency at V_{CC} = 5.5V and V_{icm} = 0.5 V

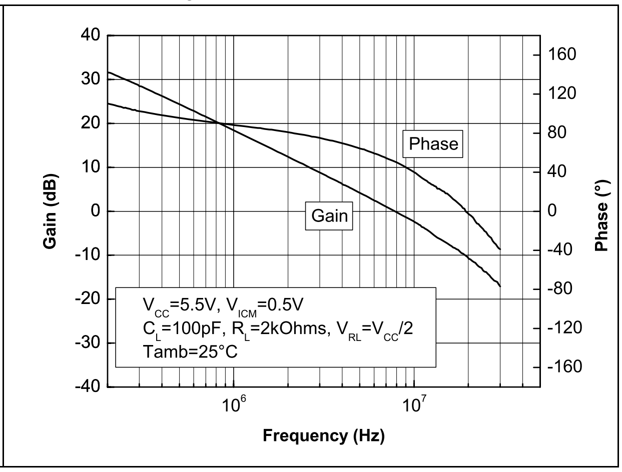


Figure 9. Phase margin vs. capacitive load

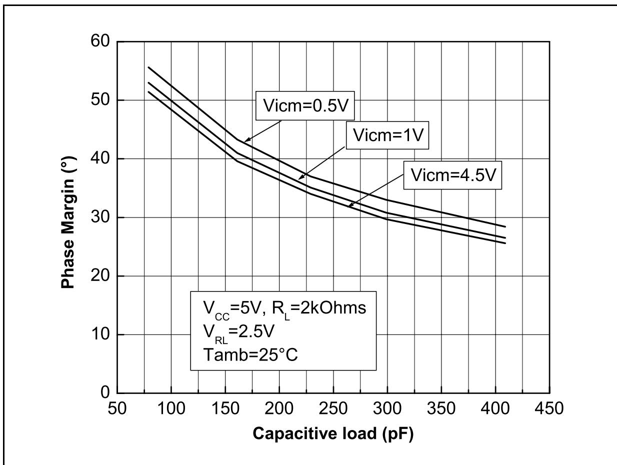


Figure 10. Phase margin vs. output current

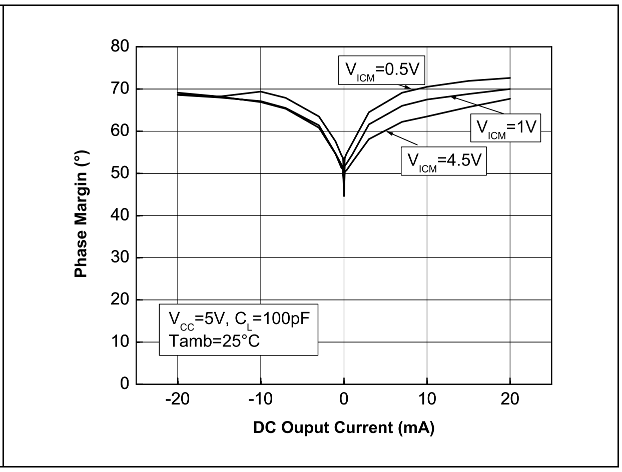


Figure 11. Positive slew rate

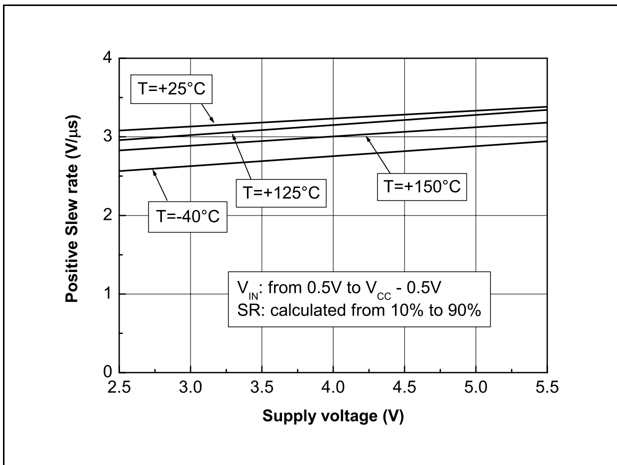


Figure 12. Negative slew rate

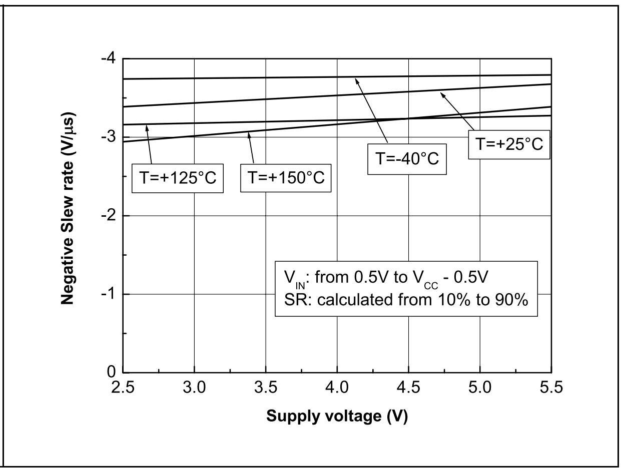


Figure 13. Distortion + noise vs. frequency

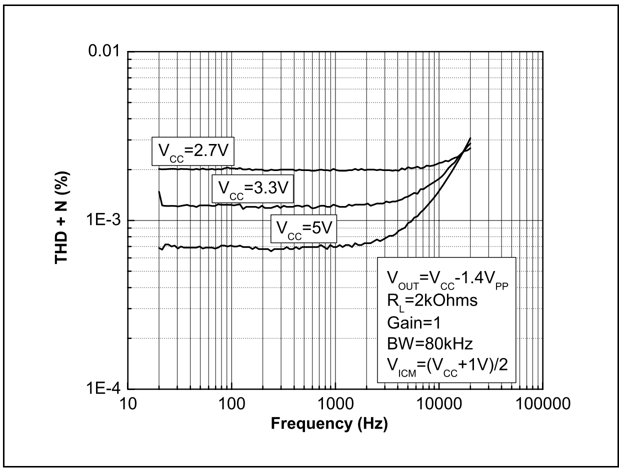


Figure 14. Distortion + noise vs. output voltage

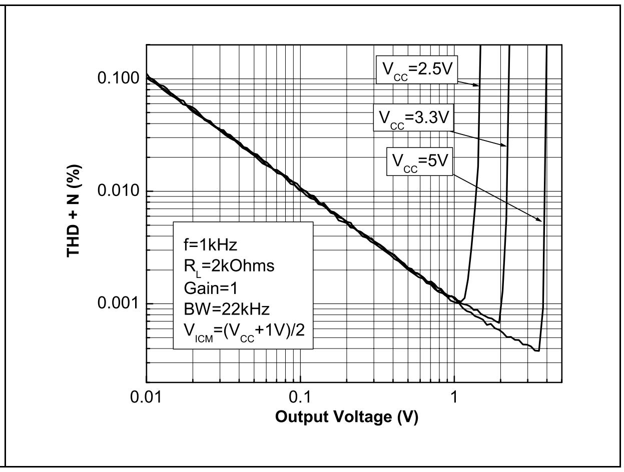


Figure 15. Noise vs. frequency

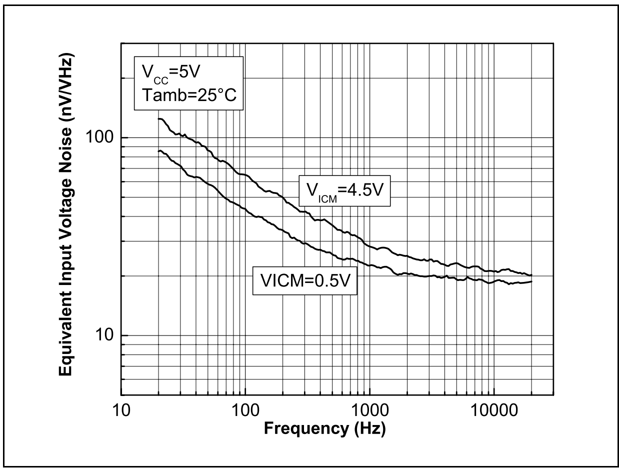


Figure 16. Phase margin vs. capacitive load and serial resistor

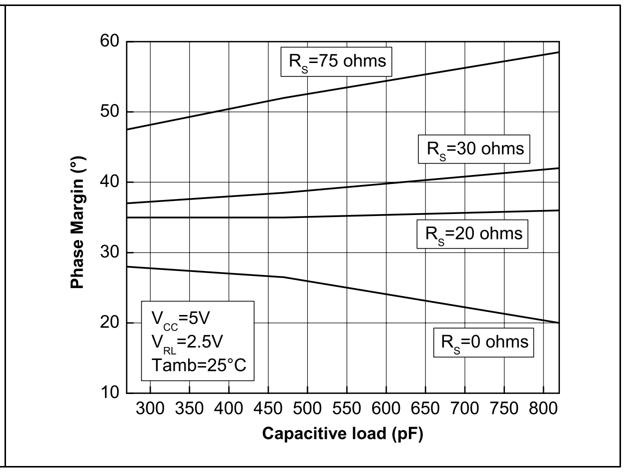
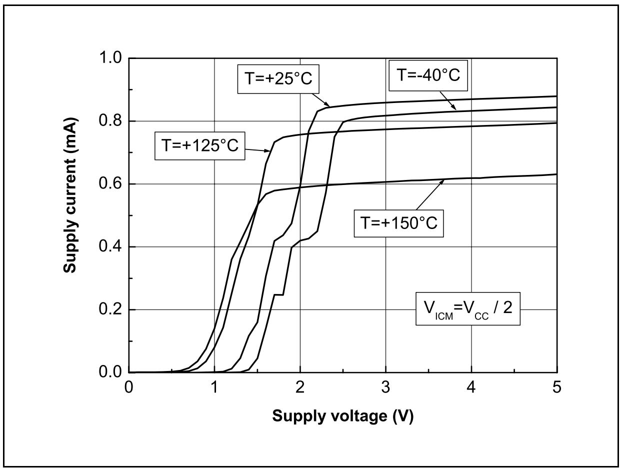


Figure 17. Supply current vs. supply voltage



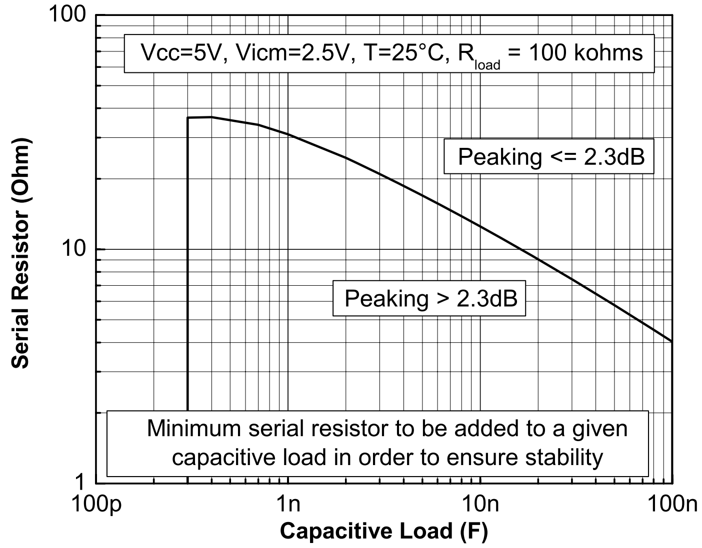
3 Application information

3.1 Driving resistive and capacitive loads

These products are low-voltage, low-power operational amplifiers optimized to drive rather large resistive loads above 2 kΩ

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding a small in-series resistor at the output can improve the stability of the devices (see *Figure 18* for recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

Figure 18. In-series resistor vs. capacitive load



3.2 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 SO-8 package information

Figure 19. SO-8 package mechanical drawing

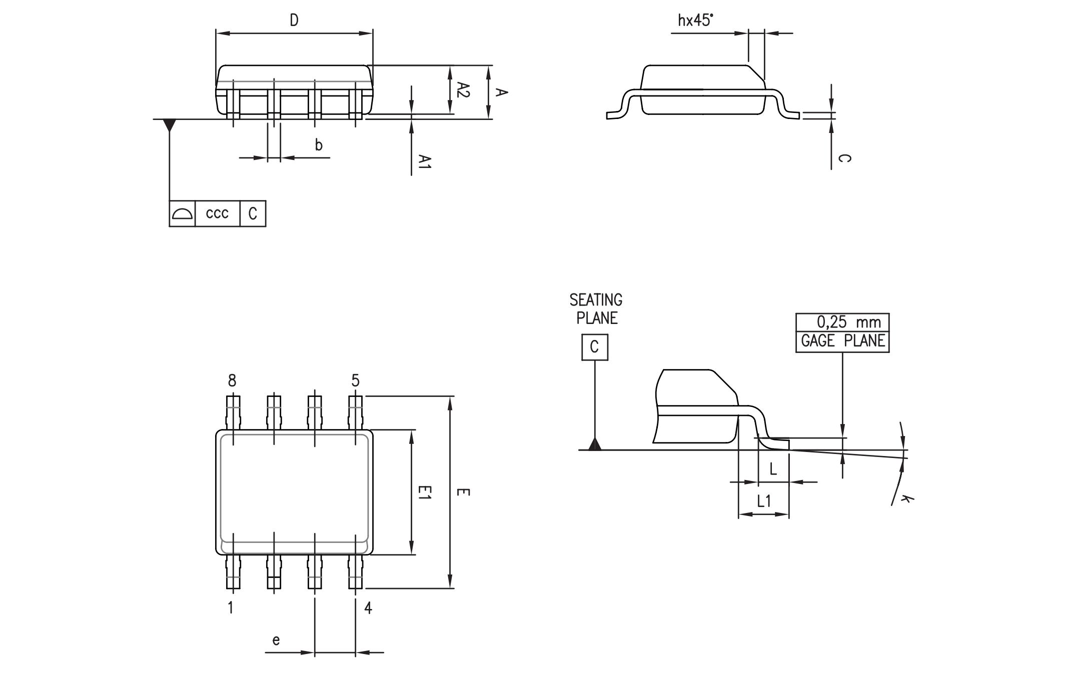


Table 6. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

5 Ordering information

Table 7. Order codes

Order code	Temperature range	Package	Packing	Marking
TSV912HYDT(1)	-40°C to +150°C	SO-8(2) (automotive grade level)	Tape & reel	V912HY
TSV912AHYDT(1)				V912AHY

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.
2. SO8 package is Moisture Sensitivity Level 1 as per Jedec J-STD-020-C.

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
08-Jul-2010	1	Initial release.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

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