



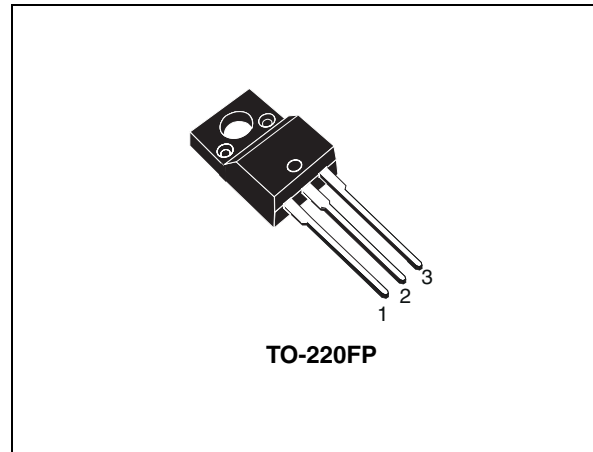
STF12NK65Z

N-channel 650 V, 0.57 Ω , 10 A, TO-220FP
Zener-protected SuperMESH™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D	P _W
STF12NK65Z	650 V	< 0.7 Ω	10 A	35 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Very good manufacturing repeatability



Application

Switching applications

Description

This N-channel SuperMESH™ Power MOSFET is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram

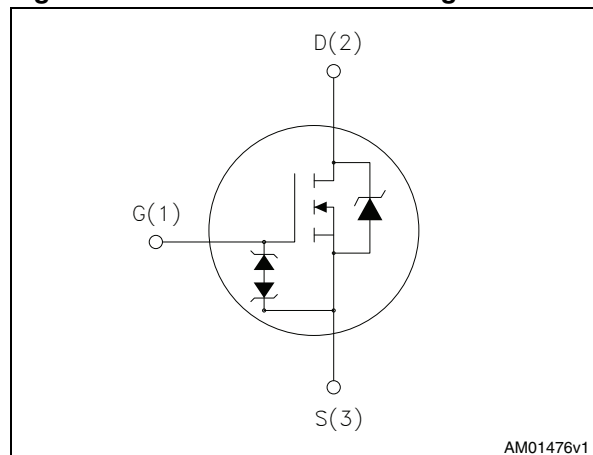


Table 1. Device summary

Order code	Marking	Package	Packaging
STF12NK65Z	12NK65Z	TO-220FP	Tube

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 8

4 **Package mechanical data** 9

5 **Revision history** 11



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	650	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	10	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	6.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	35	W
	Derating factor	1.2	W/ $^{\circ}\text{C}$
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)	2500	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Max operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 10\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.6	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^{\circ}\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	10	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^{\circ}\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	225	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$, $T_C = 125^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.57	0.7	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 5\text{ A}$	-	9.5	-	S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1837	-	pF
C_{oss}	Output capacitance			208		pF
C_{rss}	Reverse transfer capacitance			48.8		pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	122	-	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14)	-	25	-	ns
t_r	Rise time			14		ns
$t_{d(off)}$	Turn-off delay time			55		ns
t_f	Fall time			11.5		ns
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 10\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	62.6	-	nC
Q_{gs}	Gate-source charge			9.6		nC
Q_{gd}	Gate-drain charge			36		nC
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1	-	Ω

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		38	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 10\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16)	-	436		ns
Q_{rr}	Reverse Recovery Charge			3.4		μC
I_{RRM}	Reverse Recovery Current			15.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	518		ns
Q_{rr}	Reverse recovery charge			4.1		μC
I_{RRM}	Reverse recovery current			15.9		A

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30		-	V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

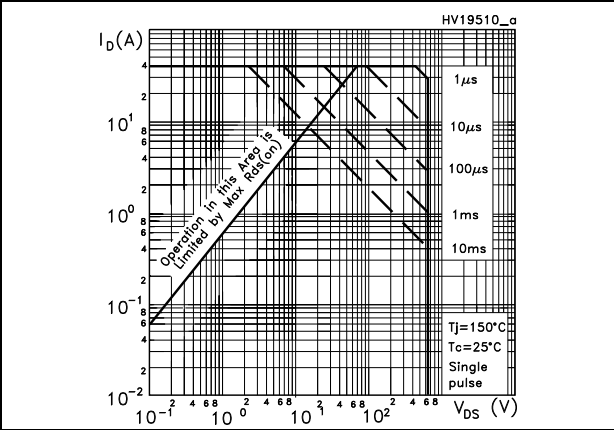


Figure 3. Thermal impedance

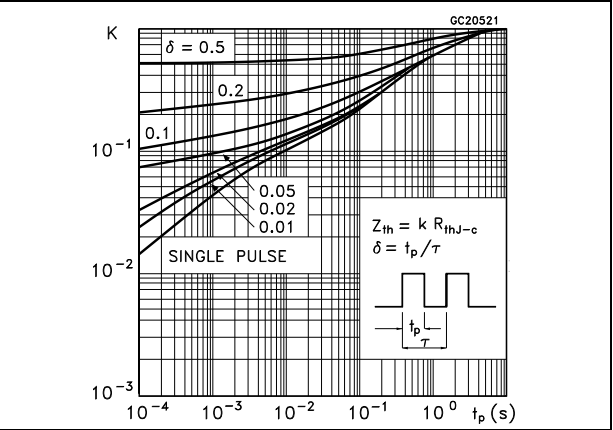


Figure 4. Output characteristics

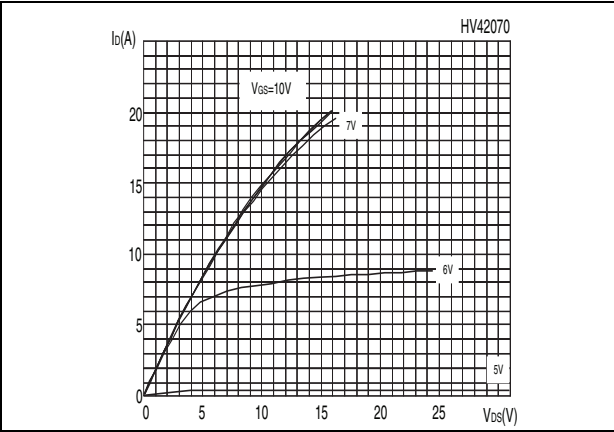


Figure 5. Transfer characteristics

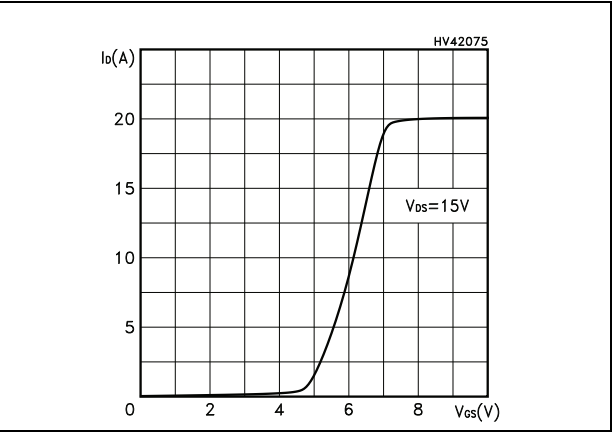


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

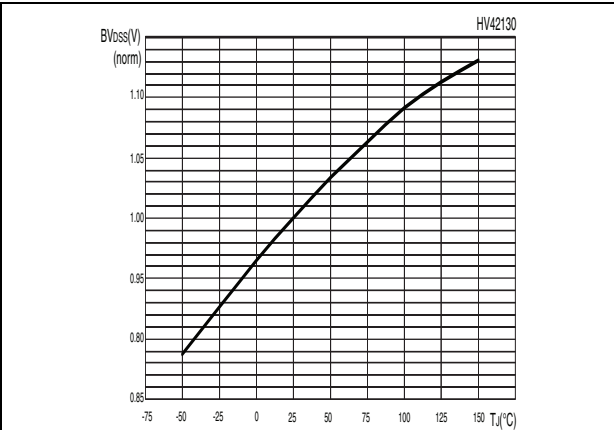


Figure 7. Static drain-source on resistance

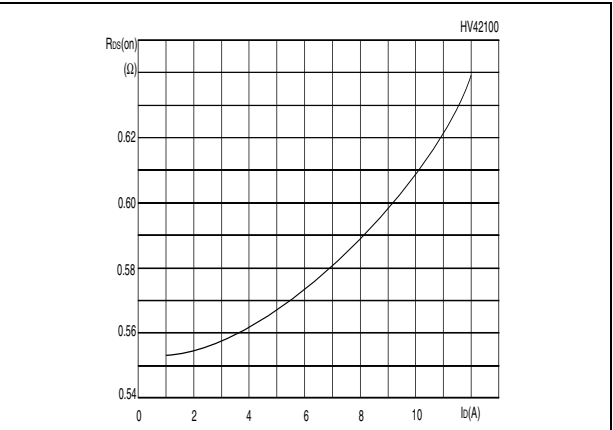


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

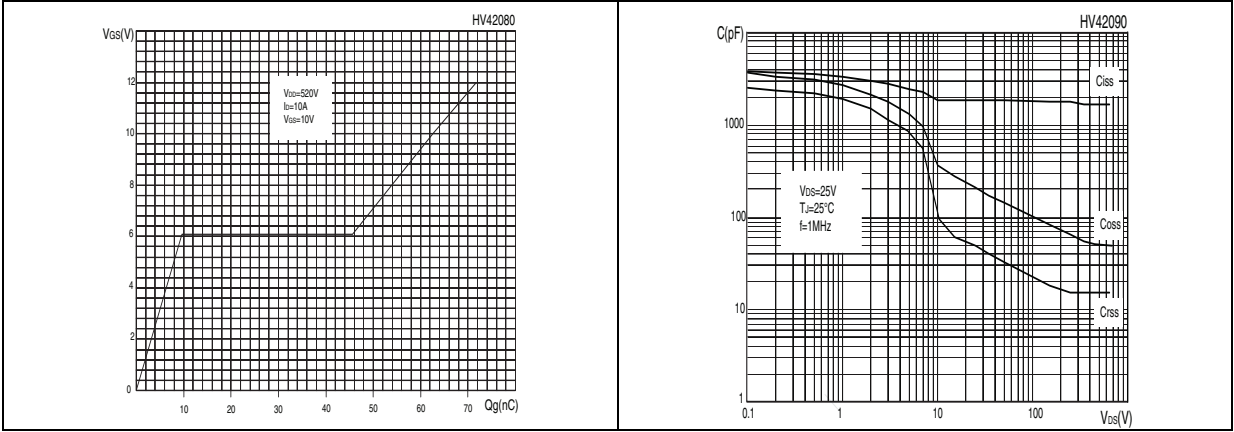


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

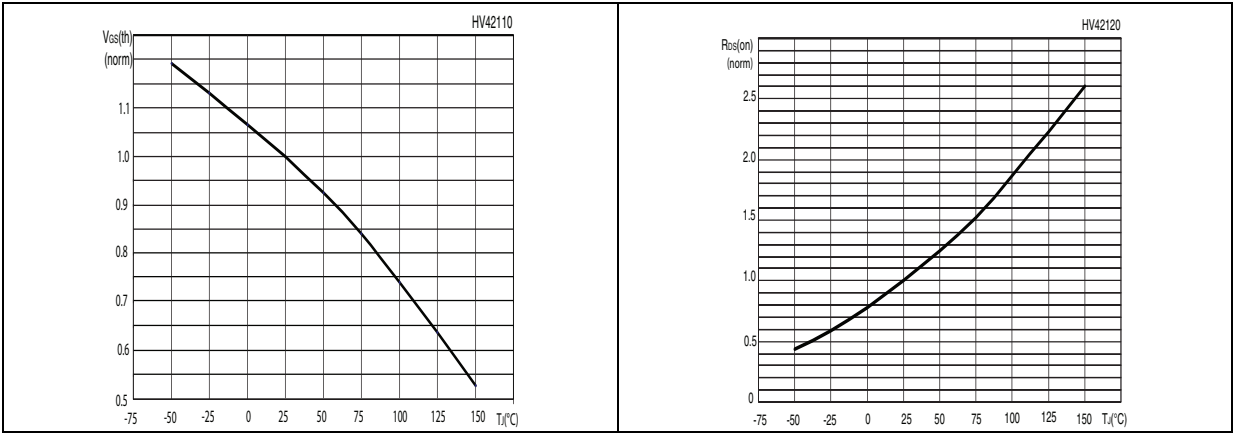
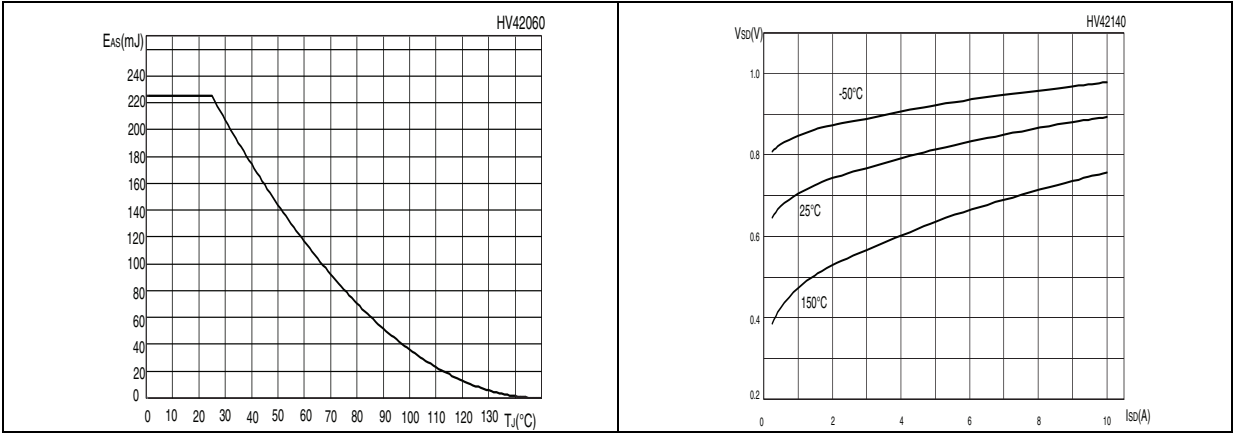


Figure 12. Maximum avalanche energy vs temperature Figure 13. Source-drain diode forward characteristic



3 Test circuits

Figure 14. Switching times test circuit for resistive load

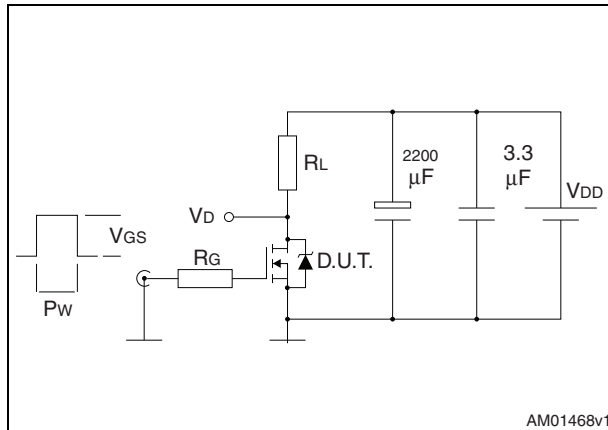


Figure 15. Gate charge test circuit

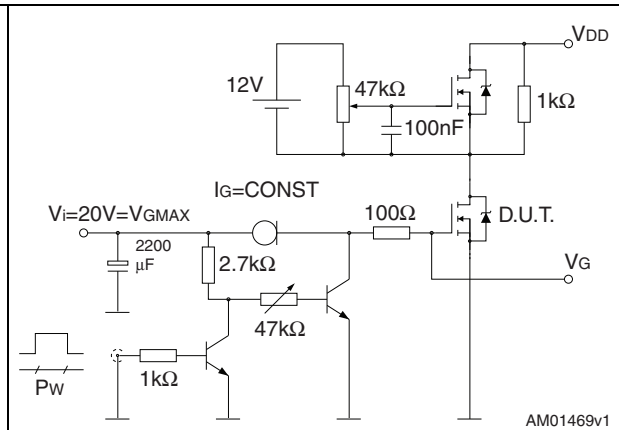


Figure 16. Test circuit for inductive load switching and diode recovery times

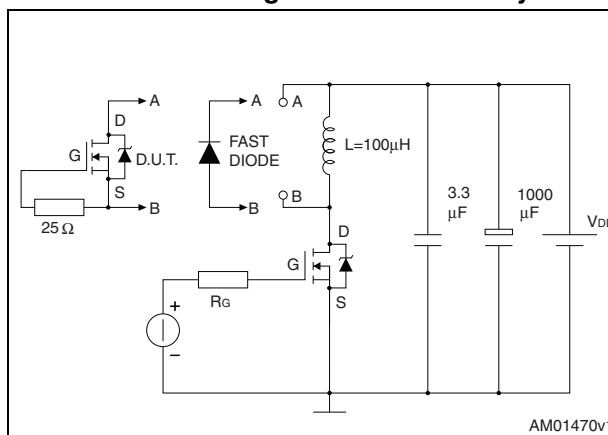


Figure 17. Unclamped inductive load test circuit

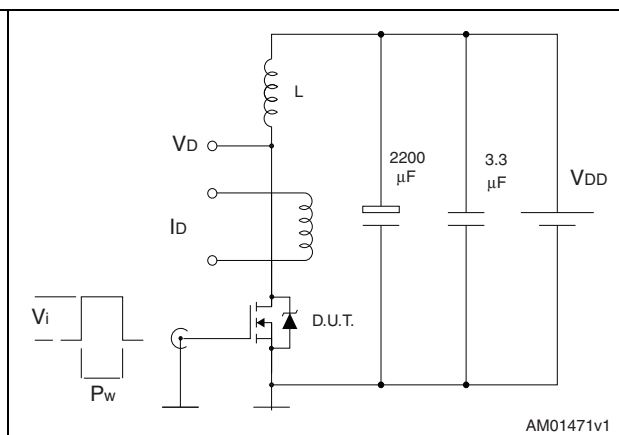


Figure 18. Unclamped inductive waveform

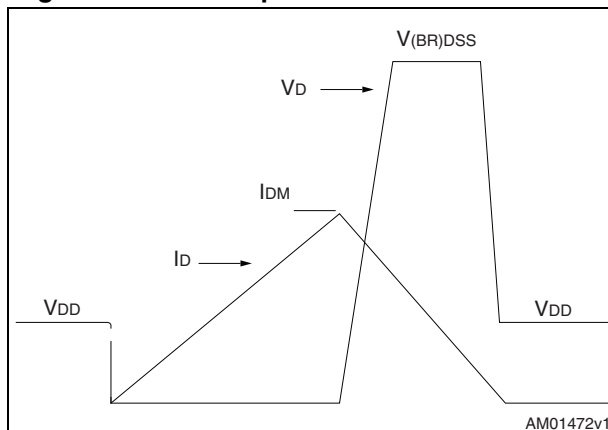
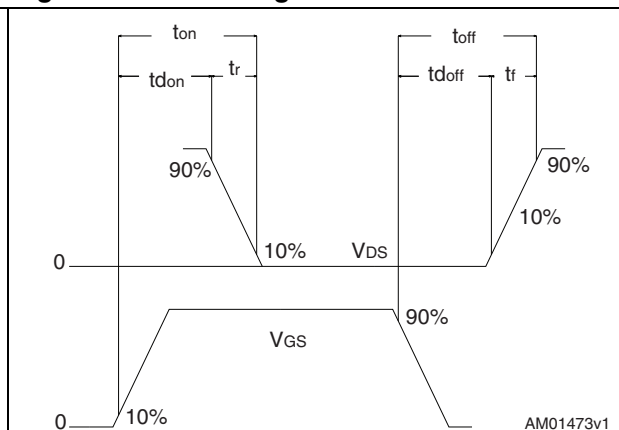


Figure 19. Switching time waveform



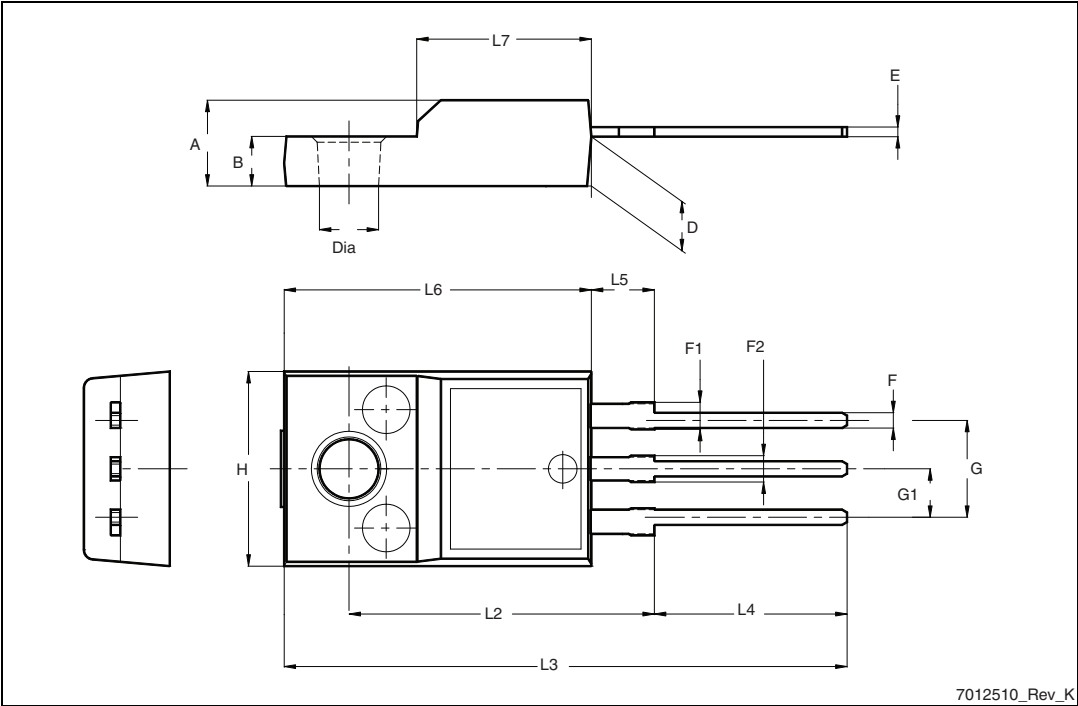
4 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 20. TO-220FP drawing



7012510_Rev_K

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Oct-2010	1	Initial release

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