CDB53L30

Evaluation Board for the CS53L30

Features

- Analog or digital Inputs
  - Analog microphone or line inputs via TRS 1/8” jacks
  - Digital microphone inputs via stake headers
- Two CS53L30 devices support up to eight channels of phase-aligned audio
- Onboard master clock generator
- S/PDIF transmitter interface via RCA and optical jacks
- External digital I/O via stake headers
  - Serial audio port I/O
  - Control signal I/O
  - External I²C™ control port I/O
- Flexible power-supply configuration
  - USB or external power supply
- FlexGUI software control
  - Windows® compatible
  - Predefined and user-configurable scripts

Description

The CDB53L30 board is a dedicated platform for testing and evaluating the CS53L30, a low-power, quad-channel microphone ADC with TDM output.

To allow comprehensive testing of CS53L30 features and performance, extensive software-configurable options are available on the CDB53L30.

Software options, such as register settings for the CS53L30, are configured with the FlexGUI software, which communicates with the CDB53L30 via USB from a Windows®-compatible computer. In addition, digital I/O headers on the CDB53L30 allow external control signals (from a host processor, for example) to configure and interface with the CS53L30 directly without the use of FlexGUI.

The CDB53L30 also serves as the component and layout reference for the CS53L30.

Ordering information

CDB53L30	Evaluation Board

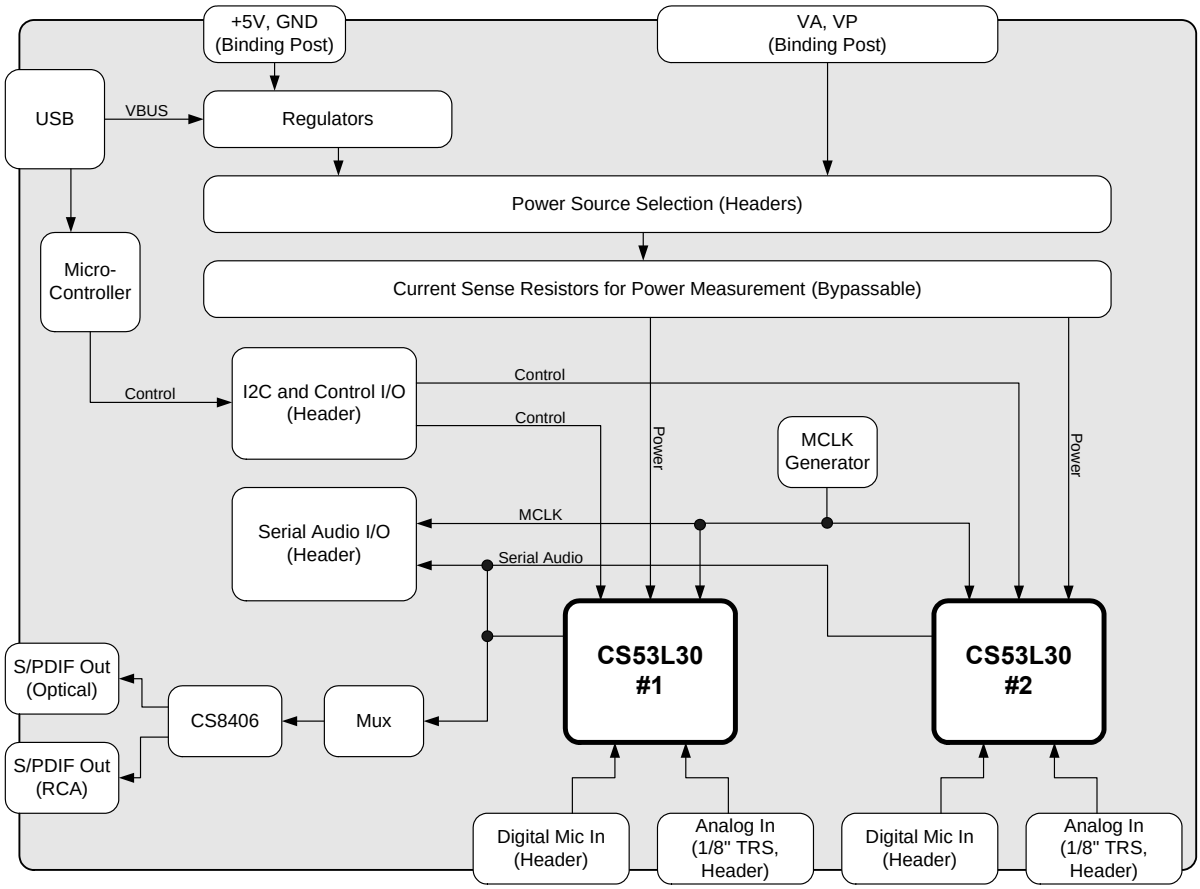


Table of Contents

1 The CDB53L30 System Overview

The CDB53L30 evaluation board is a convenient platform for evaluating the CS53L30 low-power, quad-channel microphone ADC with TDM output. It supports multiple power supply and signal I/O configurations, including the option to connect directly to the CS53L30 from an external system such as a host processor (while bypassing the onboard control circuitry). The CDB53L30 has two CS53L30 devices, providing the ability to evaluate the multichip synchronization protocol. To evaluate the synchronization protocol using four devices, two CDB53L30s can be linked using the SYNC I/O header. The CDB53L30 also serves as the component and layout reference for the CS53L30.

The following subsections describe the features of the CDB53L30 evaluation board in detail.

1.1 Power Supply Circuitry

The CDB53L30 requires a +5-V power source, supplied either by a +5-V external DC power supply connected to the +5V_EXT and GND binding posts, or by the VBUS connection from a powered USB port. The +5-V source is selectable via jumper pin block J31.

Low-dropout regulators (LDOs) step down the +5-V supply to provide clean and stable +3.3-, +3.6-, and +1.8-V rails to all the onboard circuitry and the CS53L30. Jumper pin block J2 selects the VA power supply source for the CS53L30 supply pins (either the VA_EXT binding post or the onboard +1.8-V LDO). Jumper pin block J13 selects the VP power supply source for the CS53L30 supply pins (either the VP_EXT binding post or the onboard +3.6-V LDO).

1.2 Analog Inputs

The CDB53L30 has eight analog input connectors, four per CS53L30 device. The four 1/8” TRS jacks labeled “1.AIN1," “1.AIN2," “1.AIN3," and “1.AIN4” are connected to analog inputs 1–4, respectively, of device #1. The four 1/8” TRS jacks labeled “2.AIN1," “2.AIN2," “2.AIN3," and “2.AIN4” are connected to analog inputs 1–4, respectively, of device #2.

For fully differential input sources, no jumper should be placed at the position marked “IN–” at the Sleeve/AIN– jumper pin block (J36 on channel 1.AIN1). For single-ended or pseudodifferential input sources, AIN– should be shunted to ground by placing a jumper at the “IN–” position (Pins 1 and 2).

In addition to the 1/8” TRS jacks, the input source may also be connected directly to the input header (J6 on channel 1.AIN1). The AIN+ and AIN– pins are connected directly to the “tip” and “ring” conductors of the 1/8” TRS jack, respectively.

By factory default, the sleeve conductor of the TRS cable is shunted to ground by the jumper at the position labeled “Sleeve”. When using a fully differential input source, it may be desirable for noise reasons to float the sleeve connection by removing the “Sleeve” jumper. In some cases, this can reduce noise induced by ground loops.

For microphone applications, the CS53L30 microphone bias signals are available at the input headers. Bias can also be connected to the AIN+ inputs through 1.8-kΩ series bias resistors according to the instructions below:

1. For two-pin microphones (bias connected to AIN+ through a bias resistor): the “Bias to AIN+” jumper should be shunted and the “Rbias SHORT” jumper should be open.
2. For three-pin microphones (bias not connected to AIN+): the “Bias to AIN+” jumper should be open and the “Rbias SHORT” jumper should be shunted.

DC blocking capacitors are located between the AIN+/AIN– input connectors and the CS53L30 IN± input pins. These caps are 0.1 μF, providing a typical –3-dB corner frequency of 31.8 Hz when the microphone preamplifier is bypassed (50 kΩ input impedance) or 1.6 Hz when the the preamplifier is enabled (1-MΩ input impedance).

1.3 Digital Mic Inputs

The CS53L30 can be configured to accept digital microphone inputs on channels 1 and 3. The digital microphone signals should be connected directly to the input header (J6 on input 1.AIN1) as described in Table 1-1.

Table 1-1. Digital Microphone Connections to the Input Header

Header Pin	Direction	Description
1.SCLK1	Output	Digital mic 1 serial clock from CS53L30 #1
1.SCLK2	Output	Digital mic 2 serial clock from CS53L30 #1
2.SCLK1	Output	Digital mic 1 serial clock from CS53L30 #2
2.SCLK2	Output	Digital mic 2 serial clock from CS53L30 #2
1.DATA1	Input	Digital mic 1 data to CS53L30 #1
1.DATA2	Input	Digital mic 2 data to CS53L30 #1
2.DATA1	Input	Digital mic 1 data to CS53L30 #2
2.DATA2	Input	Digital mic 2 data to CS53L30 #2
1.BIAS1	Output	Mic bias 1 from CS53L30 #1 (To supply bias directly to the pin with no series bias resistor, the “Rbias SHORT” pin jumper should be shunted)
1.BIAS3	Output	Mic bias 3 from CS53L30 #1 (To supply bias directly to the pin with no series bias resistor, the “Rbias SHORT” pin jumper should be shunted)
2.BIAS1	Output	Mic bias 1 from CS53L30 #2 (To supply bias directly to the pin with no series bias resistor, the “Rbias SHORT” pin jumper should be shunted)
2.BIAS3	Output	Mic bias 3 from CS53L30 #2 (To supply bias directly to the pin with no series bias resistor, the “Rbias SHORT” pin jumper should be shunted)

1.4 Serial Audio I/O

Header J29 provides an interface for the I²S and TDM serial audio clocks and data. The header signals are described in Table 1-2. MCLK routing is controlled by the settings on the “Board Config” tab in the FlexGUI. The direction of the LRCK/FSYNC and SCLK pins is configured by the “Serial Header Direction” control on the “Board Config” tab. When configured as Master, LRCK/FSYNC and SCLK are outputs from the CDB53L30. When configured as Slave, LRCK/FSYNC and SCLK are inputs to the CDB53L30. The logic level for all serial I/O is +1.8 V.

Table 1-2. Serial Header Signal Descriptions

Header Pin	Direction	Description
MCLK IN	Input	Master clock input
MCLK OUT	Output	Master clock output
SCLK	Input/Output	I²S or TDM bit clock
LRCK/FSYNC	Input/Output	I²S left/right clock or TDM frame sync
1.ASP1_SDOUT	Output	ASP1_SDOUT I²S or TDM data from CS53L30 #1; In I²S mode, left channel corresponds to 1.AIN1, right channel corresponds to 1.AIN2. In TDM mode, channel slot location is configurable.
1.ASP2_SDOUT	Output	ASP2_SDOUT I²S data from CS53L30 #1; Left channel corresponds to 1.AIN3, right channel corresponds to 1.AIN4.
2.ASP1_SDOUT	Output	ASP1_SDOUT I²S or TDM data from CS53L30 #2; In I²S mode, left channel corresponds to 2.AIN1, right channel corresponds to 2.AIN2. In TDM mode, channel slot location is configurable.
2.ASP2_SDOUT	Output	ASP2_SDOUT I²S data from CS53L30 #2; Left channel corresponds to 2.AIN3, right channel corresponds to 2.AIN4.

1.5 S/PDIF Transmitter

The CS8406 S/PDIF transmitter on the CDB53L30 provides a two-channel digital output simultaneously to both the RCA coaxial connector (J35) and the optical output connector (OPT2). To use the S/PDIF transmitter, the CS53L30 must be configured for I²S mode, and the CS53L30 MCLK/LRCK ratio must correspond to one of the four ratios supported by the CS8406: 128x, 256x, 384x, or 512x. Only one SDOUT signal may be chosen for output at any time. The CS8406 clock ratio and desired SDOUT signal are selected on the “Board Config” tab of the FlexGUI.

1.6 Master Clock

The CDB53L30 includes a fixed-frequency crystal oscillator and CS2300 programmable PLL, facilitating the generation of an onboard MCLK. The MCLK frequency is configured on the “Board Config” tab of the FlexGUI.

The Serial Audio I/O header J29 provides a MCLK input pin and MCLK output pin. The MCLK IN pin can be used to provide an externally generated MCLK to the board. The MCLK OUT pin provides either a buffered version of the onboard generated MCLK or a buffered version of the MCLK IN signal. By providing a buffered version of the MCLK IN signal, the MCLK OUT pin may be used for daisy chaining an additional CDB53L30. This is useful when the external clock source does not have sufficient output drive capability to support multiple parallel loads. To enable the various MCLK routing options, use the MCLK buffer control drop-down boxes in the “Board Config” tab in the FlexGUI.

1.7 Synchronization I/O

For applications requiring more than two CS53L30 devices, two CDB53L30 boards may be linked using the Sync I/O header J33. This will allow up to four CS53L30 devices to be synchronized using the multichip synchronization protocol. The direction of the sync signal is configured using jumper pin block J37. For more information on enabling the synchronization protocol, see the CS53L30 data sheet.

1.8 Control Port Interface

The Cirrus Logic FlexGUI software application (downloadable from http://www.cirrus.com/msasoftware) provides users an easy and intuitive way to configure the CDB53L30. A Windows®-compatible PC with USB connectivity is required to run FlexGUI.

The CDB53L30’s onboard microcontroller handles the USB communication with FlexGUI and the I^2C control port interface of the CS53L30. The control port interface and the control I/O signals ($\overline{\text{INT}}$, $\overline{\text{RST}}$, and MUTE) are routed through jumper pin block J4. When the pin columns marked “FlexGUI CNTL” are shunted, the microcontroller handles all communication between the FlexGUI application and the CS53L30. To interface to an external system, the shunts on J4 should be removed and the external signals should be connected to the pin columns marked “EXT SYS” (note the GND pins on the right hand side of the header).

The $\overline{\text{INT}}$, $\overline{\text{RST}}$, and MUTE control signals for the two CS53L30 devices may be ganged together using the “CONTROL SHORTS” jumper pin block J34. This allows both devices to share a single set of control signals. To enable ganging of a control, apply a shunt to the desired signal on J34. When ganging a control, remove one of the associated FlexGUI control jumpers from J4 to prevent contention between the two ganged control signals from the microcontroller.

1.9 Layout Reference

The CDB53L30 utilizes a six-layer PCB that allows for optimal trace and power routing to the CS53L30 devices and surrounding circuitry. Local decoupling capacitors for the CS53L30 are placed as close as possible to the device. The CDB53L30 uses a topside-only component placement without compromise to placement of critical components, but a double-sided placement is also be feasible. Ground fill is used extensively on the component layer to isolate critical nets where possible.

2 Quick-Start Guide

This section describes a basic setup procedure for the CDB53L30. After completing the steps in Fig. 2-1, the CDB53L30 will be configured to accept eight single-ended or differential analog line inputs and will output four two-channel I²S streams at a sample rate of 48 kHz.

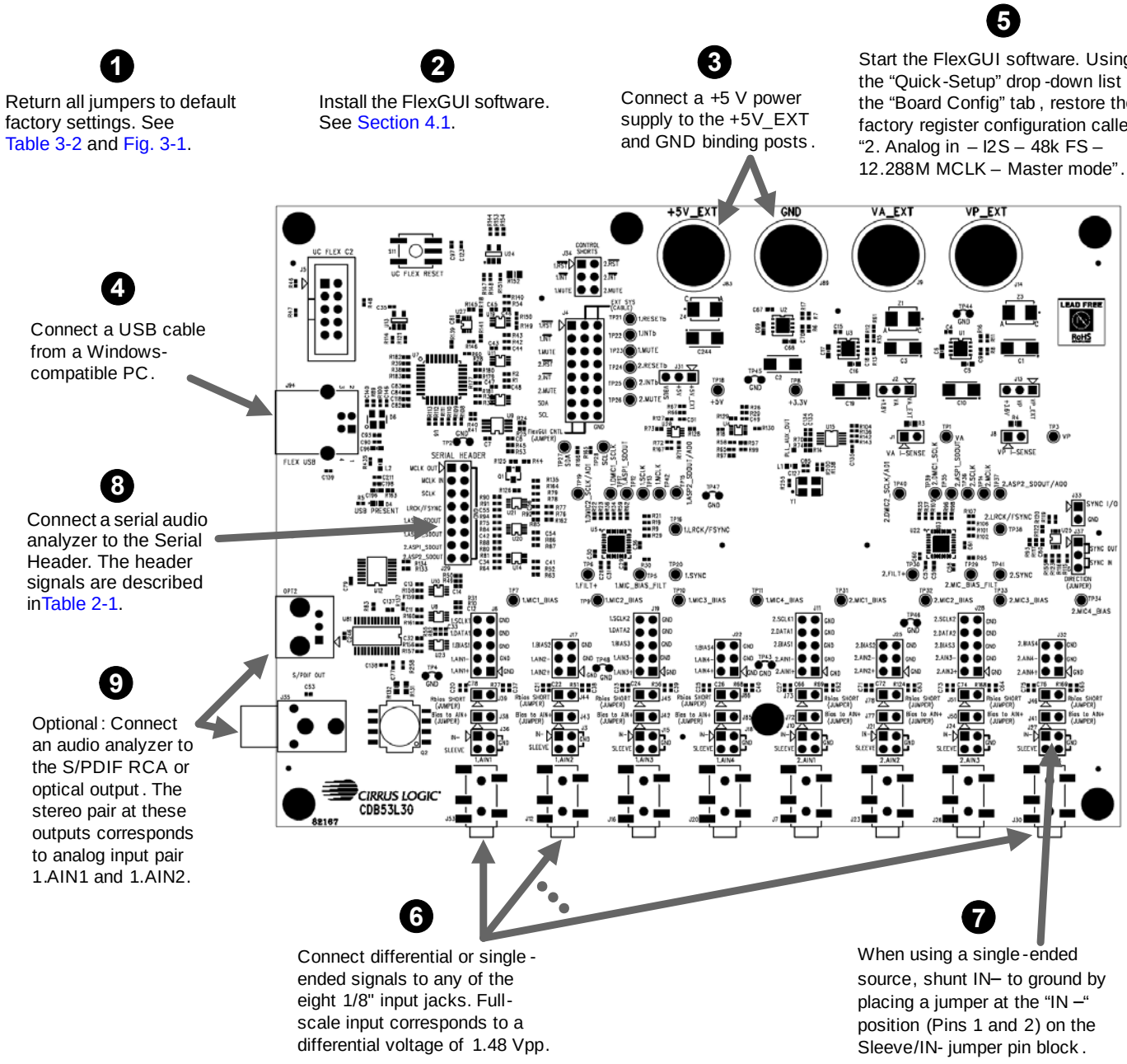


Figure 2-1. CDB53L30 Factory Default Jumper Settings

Table 2-1. Quick-Start Serial Header Signal Descriptions

Header Pin	Direction	Frequency	Description
MCLK IN	N/A	N/A	Not used
MCLK OUT	Output	12.288 MHz	Master clock
SCLK	Output	3.072 MHz	I²S bit clock
LRCK/FSYNC	Output	48 kHz	I²S left/right clock
1.ASP1_SDOUT	Output	N/A	ASP1_SDOUT I²S data from CS53L30 #1; Left channel corresponds to 1.AIN1, right channel corresponds to 1.AIN2

Table 2-1. Quick-Start Serial Header Signal Descriptions *(Cont.)*

Header Pin	Direction	Frequency	Description
1.ASP2_SDOUT	Output	N/A	ASP2_SDOUT I²S data from CS53L30 #1; Left channel corresponds to 1.AIN3, right channel corresponds to 1.AIN4
2.ASP1_SDOUT	Output	N/A	ASP1_SDOUT I²S data from CS53L30 #2; Left channel corresponds to 2.AIN1, right channel corresponds to 2.AIN2
2.ASP2_SDOUT	Output	N/A	ASP2_SDOUT I²S data from CS53L30 #2; Left channel corresponds to 2.AIN3, right channel corresponds to 2.AIN4

3 System Connections and Jumper Settings

All power and signal I/O connections are listed in Table 3-1. Jumper settings are described in Table 3-2. LED indicator states are described in Table 3-3. Factory default jumper settings are shown in Fig. 3-1.

Table 3-1. External System Connections

Reference Designator	Connection	Input/Output	Description
J83	+5V_EXT	Input	+5-V external power supply
J89	GND	Input	Board ground
J9	VA_EXT	Input	CS53L30 VA external supply
J14	VP_EXT	Input	CS53L30 VP external supply
J5	UC FLEX C2	Input	Microcontroller programming header
J94	USB	Input/Output	USB connection
J29	SERIAL HEADER	Input/Output	CS53L30 Audio Serial Port (MCLK IN, MCLK OUT, LRCK/FSYNC, SCLK, ASP1_SDOUT, ASP2_SDOUT)
J4	CONTROL HEADER	Input/Output	CS53L30 control port connections (SDA, SCL, $\overline{INT}$, $\overline{RST}$, MUTE) • By default, shunts connect the columns marked “FlexGUI CNTL (JUMPER)”. This connects the onboard microcontroller to the control port of the CS53L30. • To use external control signals, remove shunts and connect the external controls to the columns marked “EXT SYS (CABLE)”. Notice the ground connections on Column 3.
J35	S/PDIF OUT	Output	Coaxial S/PDIF digital output
OPT2	S/PDIF OUT	Output	Optical S/PDIF digital output
J53	1.AIN1	Input	Analog mic/line TRS input 1 for CS53L30 #1
J12	1.AIN2	Input	Analog mic/line TRS input 2 for CS53L30 #1
J16	1.AIN3	Input	Analog mic/line TRS input 3 for CS53L30 #1
J20	1.AIN4	Input	Analog mic/line TRS input 4 for CS53L30 #1
J7	2.AIN1	Input	Analog mic/line TRS input 1 for CS53L30 #2
J23	2.AIN2	Input	Analog mic/line TRS input 2 for CS53L30 #2
J26	2.AIN3	Input	Analog mic/line TRS input 3 for CS53L30 #2
J30	2.AIN4	Input	Analog mic/line TRS input 4 for CS53L30 #2
J6	Input header	Input	Analog input 1 and digital mic interface 1 for CS53L30 #1
J17	Input header	Input	Analog input 2 for CS53L30 #1
J19	Input header	Input	Analog input 3 and digital mic interface 2 for CS53L30 #1
J22	Input header	Input	Analog input 4 for CS53L30 #1
J11	Input header	Input	Analog input 1 and digital mic interface 1 for CS53L30 #2
J25	Input header	Input	Analog input 2 for CS53L30 #2
J28	Input header	Input	Analog input 3 and digital mic interface 2 for CS53L30 #2
J32	Input header	Input	Analog input 4 for CS53L30 #2
J33	SYNC I/O	Input/Output	Synchronization Input/Output for additional CDB53L30

Table 3-2. CDB53L30 Jumper Settings

Jumper Pin Block	Connection	Purpose	Position	Function Selected
J31	+5 V	Select +5 V main supply	+5V_EXT [1] VBUS	+5-V supply source from J83 +5-V supply source from USB VBUS
J2	VA	Select CS53L30 VA supply source	VA EXT +1.8 V [1]	CS53L30 VA supply from J9 CS53L30 VA supply from +1.8 V derived from LDO
J13	VP	Select CS53L30 VP supply source	VP_EXT +3.6 V [1]	CDB53L30 VP supply from J14 CDB53L30 VP supply from +3.6 V derived from LDO

Table 3-2. CDB53L30 Jumper Settings *(Cont.)*

Jumper Pin Block	Connection	Purpose	Position	Function Selected
J34	CONTROL SHORTS	Gang control signals of CS53L30 #1 and CS53L30 #2	Shunted Open [1]	Control signals are tied. Control signals are independent.
J39, J44, J45, J86, J73, J78, J51, J46	Rbias SHORT	Shunt across the 1.8 kΩ bias resistor	Shunted Open [1]	1.8-kΩ bias resistor is shunted (for three-wire mic connection). 1.8-kΩ bias resistor is not shunted (for two-wire mic connection).
J38, J43, J42, J85, J72, J77, J50, J41	Bias to AIN+	Connect mic bias to noninverting input	Shunted Open [1]	Mic bias tied to AIN+. Mic bias not tied to AIN+.
J36, J3, J15, J18, J10, J21, J24, J27	IN– to GND	Connect inverting input to ground	Shunted Open [1]	IN– tied to ground (for pseudodifferential input). IN– not tied to ground (for true differential input).
J36, J3, J15, J18, J10, J21, J24, J27	SLEEVE to GND	Connect TRS sleeve conductor to ground	Shunted [1] Open	Sleeve tied to ground. Sleeve floating.
J37	SYNC DIRECTION	Configure direction of synchronization signal	SYNC IN SYNC OUT[1]	Sync signal is input (from another CDB53L30). Sync signal is output (to another CDB53L30).
J1	VA I-SENSE	CS53L30 VA current measurement	Shunted [1] Open	1-Ω current measurement resistor is shorted. 1-Ω current measurement resistor is in series with CS53L30 VA, allowing direct measurement of VA supply current at J1.
J8	VP I-SENSE	CS53L30 VP current measurement	Shunted [1] Open	1-Ω current measurement resistor is shorted. 1-Ω current measurement resistor is in series with CS53L30 VP, allowing direct measurement of VP supply current at J8.

1. Indicates default factory settings.

Table 3-3. LED Indicators

LED	Indication	Status	Function
D4	USB present	On Off	Indicates there is a USB connection to the CDB53L30. Indicates there is not a USB connection to the CDB53L30.

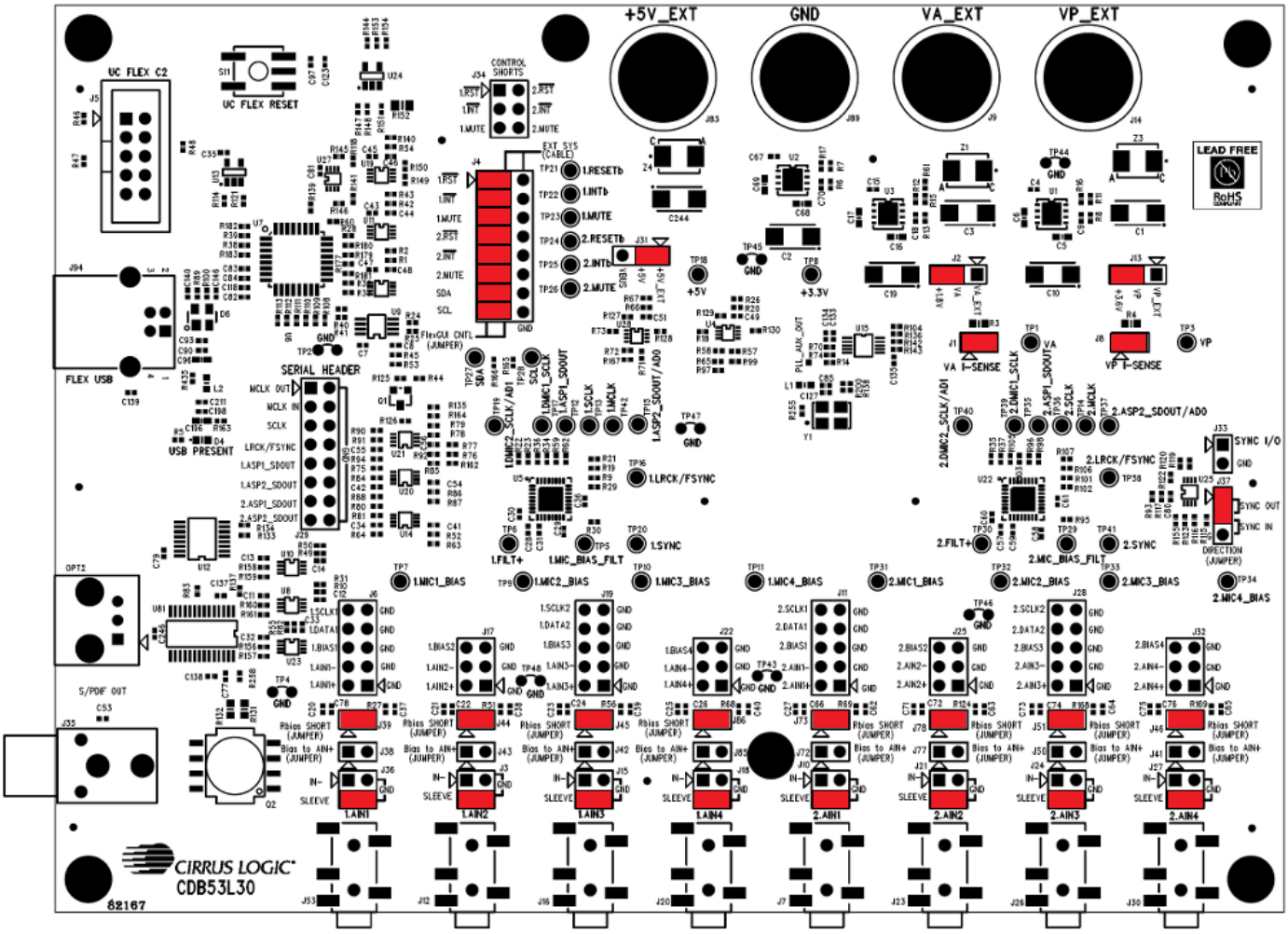


Figure 3-1. CDB53L30 Factory Default Jumper Settings

4 Software Control Using FlexGUI

The Cirrus Logic FlexGUI application is a graphical user interface that allows users to easily configure software modifiable options on the CDB53L30, such as the register settings of the CS53L30 and the CS8046 S/PDIF transmitter.

4.1 Installation and First-Time Setup

To set up FlexGUI for use with the CDB53L30, follow these steps:

1. Download the latest version of the FlexGUI control software from www.cirrus.com/msasoftware. Follow the installation instructions on the download page.
2. Connect the CDB53L30 to the host PC using a USB cable.
3. Apply power to the CDB53L30.
4. Launch FlexGUI. Once the GUI is launched successfully, all registers are set to their default reset states. To start evaluating the CS53L30 immediately using one of several factory preset configurations, load the predefined register settings using the Quick Setup drop-down box on the “Board Config” tab.

4.2 Working with Register Settings

Register settings can be restored automatically using factory or user-defined script files. Registers can be modified using the high-level interface controls, or they may be edited directly in the Register Maps tab of the FlexGUI.

4.2.1 Modifying Individual Register Settings

There are two ways to modify individual register settings:

- Using the high-level graphical interface, which features intuitive GUI elements such as sliders, check boxes, and drop-down menus. See Section 4.3 for details on using the high-level interface.
- Using the low-level Register Maps tab, which displays the entire user configurable register space for each device on the CDB53L30 in table form. The Register Maps tab allows the user to modify entire registers or individual register bits. See Section 4.4 for details on the register map.

4.2.2 Save or Restore Register Settings

FlexGUI allows saving the current state of all register settings to a file, which can easily be restored later.

Figure 4-1. Save Register Settings

Figure 4-2. Restore Register Settings

To save the current register settings, click on the File menu, then click “Save Board Registers” (Fig. 4-1). Enter a suitable file name and click “Save.”

To restore predefined/saved register settings, click on the File menu, then click “Restore Board Registers” (Fig. 4-2). Choose the desired register setting and click “Open.”

To restore one of several standard configurations predefined at the factory, use the Quick Setup drop-down box on the "Board Config" tab, or use the *Restore Board Registers...* command to load any of the configurations starting with "FACTORY--" in the file name. The file names are meant to be self-explanatory. For example, the script called "FACTORY--analog_48k_12.288M_master_I2S_dual.fgs" configures the board as I²S master with a 48k sample rate and 12.288 MHz MCLK, using analog input type.

The factory scripts are written with special consideration to proper sequencing of device settings, for example, enabling a device's power down mode before changing its MCLK settings. Register settings saved using the method described in this section DO NOT include sequencing and may result in unexpected behavior when restored in the FlexGUI.

4.3 Using the FlexGUI Tabs

The FlexGUI features a series of tabs which represent the high- and low-level controls, grouped together according to function. Fig. 4-3 shows the tabs in the FlexGUI interface.

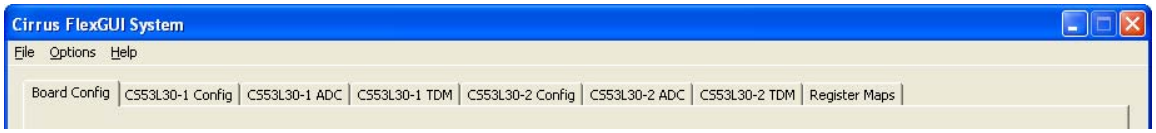


Figure 4-3. FlexGUI Tabs

- **Board Config**—Board controls for configuring the MCLK source, S/PDIF transmitter, serial header, and CS53L30 mute signals
- **CS53L30-1 Config, CS53L30-2 Config**—Controls for configuring the overall operation of the CS53L30
- **CS53L30-1 ADC, CS53L30-2 ADC**—Controls for configuring ADC functionality of the CS53L30 (volume, noise gate, high-pass filter, etc.)
- **CS53L30-1 TDM, CS53L30-2 TDM**—Controls for configuring TDM mode of the CS53L30
- **Register Maps**—Allows direct register access to all the devices on the CDB53L30

The subsequent sections, Section 4.3.1 through Section 4.3.4, describe each tab in detail.

4.3.1 Board Config Tab

The “Board Config” tab contains the controls for configuring the MCLK source, S/PDIF transmitter, serial header, and CS53L30 mute signals. The individual functions of this tab are described below.

- **Quick Setup**—Drop-down box for selecting a factory preset register configuration.
- **MCLK**—Settings for onboard MCLK frequency and MCLK routing.
- **S/PDIF Transmitter**—Settings for the CS8406 S/PDIF transmitter. See Section 1.5 for more information.
- **Mute Control**—Configures the state of the microcontroller I/O pins which drive the CS53L30 MUTE inputs. To enable these controls, jumper pin block J4 must have the corresponding “FlexGUI CNTL” jumpers placed.
- **Serial Header Direction**—Configures the SCLK and LRCK/FSYNC signal direction for the serial audio header, J29. When configured as Master, SCLK and LRCK/FSYNC are outputs from the CDB53L30. When configured as Slave, SCLK and LRCK/FSYNC are inputs to the CDB53L30.
- **Device and Revision I.D.**—Displays the CS53L30 revision information.
- **Refresh**—Reads all registers in all devices and updates the values in the FlexGUI.
- **Reset CS53L30-1**—Sends a reset pulse to CS53L30 #1.
- **Reset CS53L30-2**—Sends a reset pulse to CS53L30 #2.

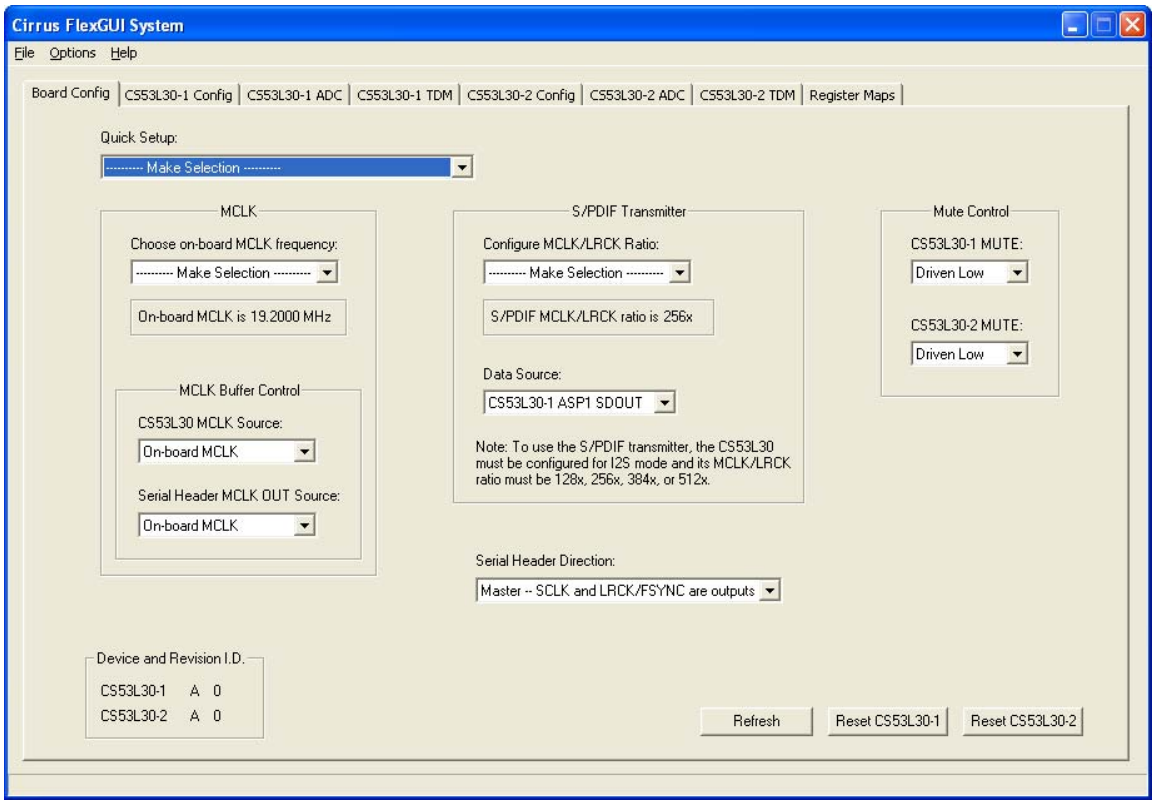


Figure 4-4. The “Board Config” Tab

4.3.2 CS53L30 Config Tab

The “CS53L30-1 Config” and “CS53L30-2 Config” tabs contain the controls for configuring the CS53L30 power down state, serial port settings, DMIC, mic bias, input pin bias, MUTE pin power down behavior, and multichip synchronization.

- **Power**—Configures the power down controls and supply settings.
- **MCLK**—Controls for MCLK configuration.
- **ASP**—Settings for Audio Serial Port configuration.
- **DMIC**—Settings for digital mic configuration.
- **Multichip Sync**—Enables the multichip synchronization protocol (see the CS53L30 data sheet for details on using the sync protocol).
- **Mic Bias**—Power down and output voltage controls for the mic bias outputs.
- **MUTE**—Configures the polarity of the MUTE input pin and the associated power down states which are active while MUTE is asserted.
- **Input Pin Bias**—Configures the bias for each input pin.
- **Refresh**—Reads all registers in all devices and updates the values in the FlexGUI.
- **Reset CS53L30-1**—Sends a reset pulse to CS53L30 #1.
- **Reset CS53L30-2**—Sends a reset pulse to CS53L30 #2.

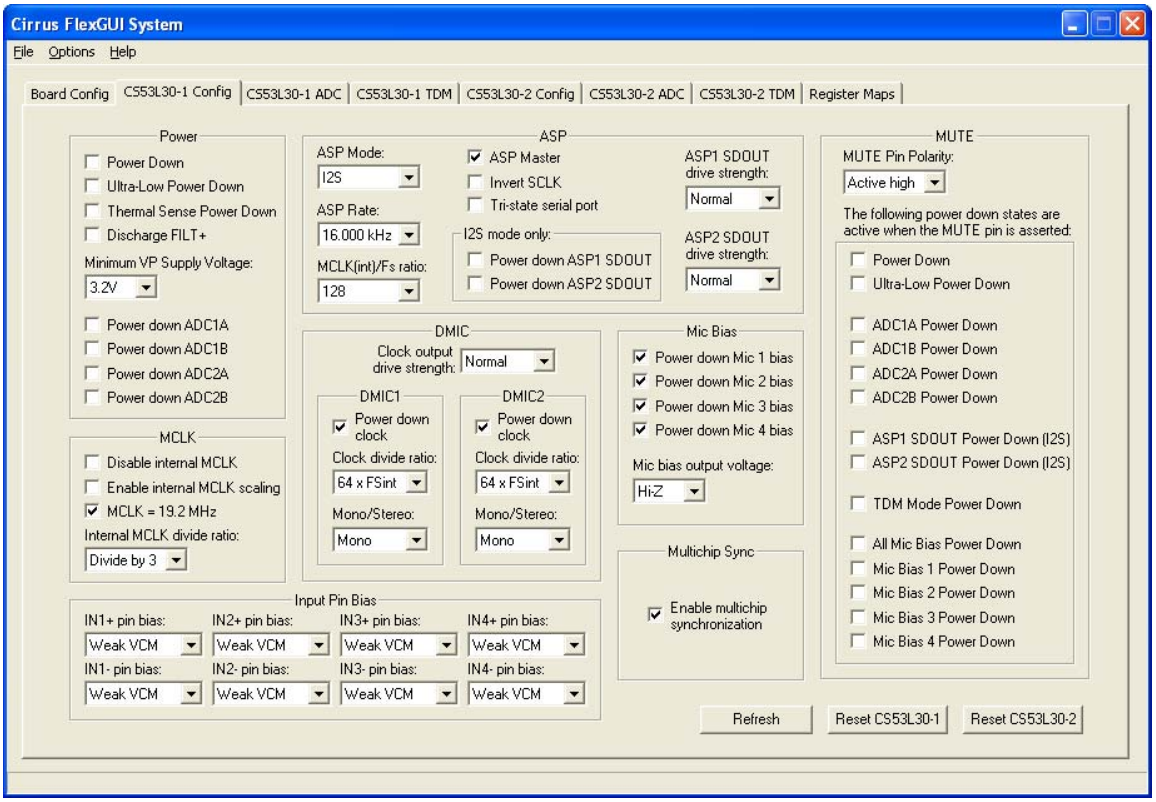


Figure 4-5. The “CS53L30 Config” Tab

4.3.3 CS53L30 ADC Tab

The “CS53L30-1 ADC” and “CS53L30-12 ADC” tabs contain the controls for the ADC settings, including notch filter enable, high-pass filter configuration, noise gating, volume controls, and input type. The controls on the left correspond to ADC1, and the controls on the right correspond to ADC2.

- **Disable digital notch filter**—Disables the digital notch filter (applies to both channels of the ADC).
- **High-Pass Filter**—Controls for the high-pass filter (applies to both channels of the ADC).
- **Noise Gate**—Controls for the noise gate.
- **Channel volume controls**—Controls for mic preamp gain, PGA volume, digital volume, +20 dB digital boost, and signal inversion (Channel A and Channel B have independent controls).
- **Input channel type**—Configures the CS53L30 for either analog or digital inputs (applies to all input channels).
- **Enable soft ramp on all digital volume changes**—Enables an incremental ramp on all digital volume changes (applies to all input channels).
- **Refresh**—Reads all registers in all devices and updates the values in the FlexGUI.
- **Reset CS53L30-1**—Sends a reset pulse to CS53L30 #1.
- **Reset CS53L30-2**—Sends a reset pulse to CS53L30 #2.

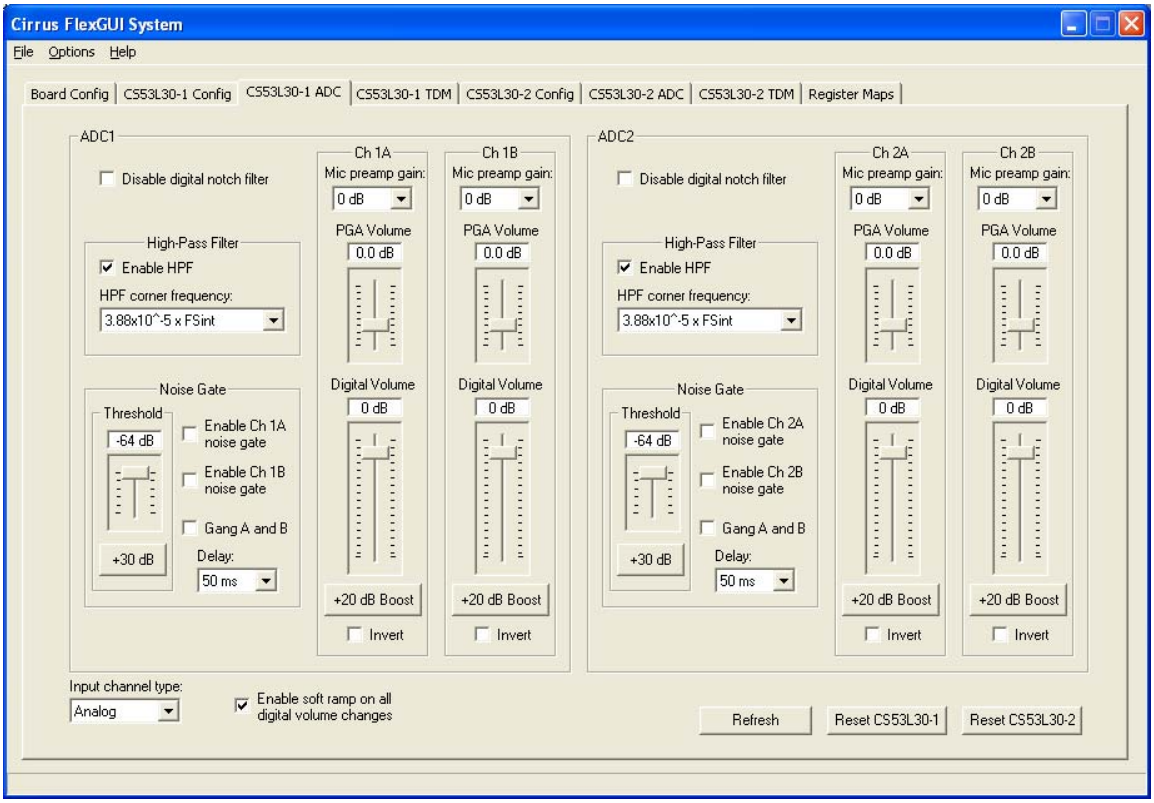


Figure 4-6. The “CS53L30 ADC” Tab

4.3.4 CS53L30 TDM Tab

The “CS53L30-1 TDM” and “CS53L30-2 TDM” tabs contain the controls for configuring the CS53L30 TDM output. These controls apply only when the ASP Mode is configured for TDM on the “CS53L30 Config” tab.

- **Shift TDM frame 1/2 SCLK left—**Configures the start offset of TDM data after a rising edge of LRCK/FSYNC.
- **LRCK Pulse Width**—Configures the LRCK/FSYNC high time in TDM mode. The pulse width can be fixed to 50% duty cycle or configured for any number of SCLK cycles. The high-level GUI allows the user to select between 1 and 8 SCLK cycles as the programmable high time. To configure the CS53L30 for a programmable high time of greater than 8 SCLK cycles, the user should write directly to the LRCK_TPWH field in registers 0x1B and 0x1C in the appropriate CS53L30 register tab.
- **TDM Channel Configuration**—Enables TDM output from each of the four ADC channels and configures the channel’s starting TDM slot location.
- **TDM Slot Enable**—Determines into which of the 48 available TDM time slots the CS53L30 can load data. During time slots which are not enabled, the ASP1_SDOUT output pin is Hi-Z.
- **Refresh**—Reads all registers in all devices and updates the values in the FlexGUI.
- **Reset CS53L30-1**—Sends a reset pulse to CS53L30 #1.
- **Reset CS53L30-2**—Sends a reset pulse to CS53L30 #2.

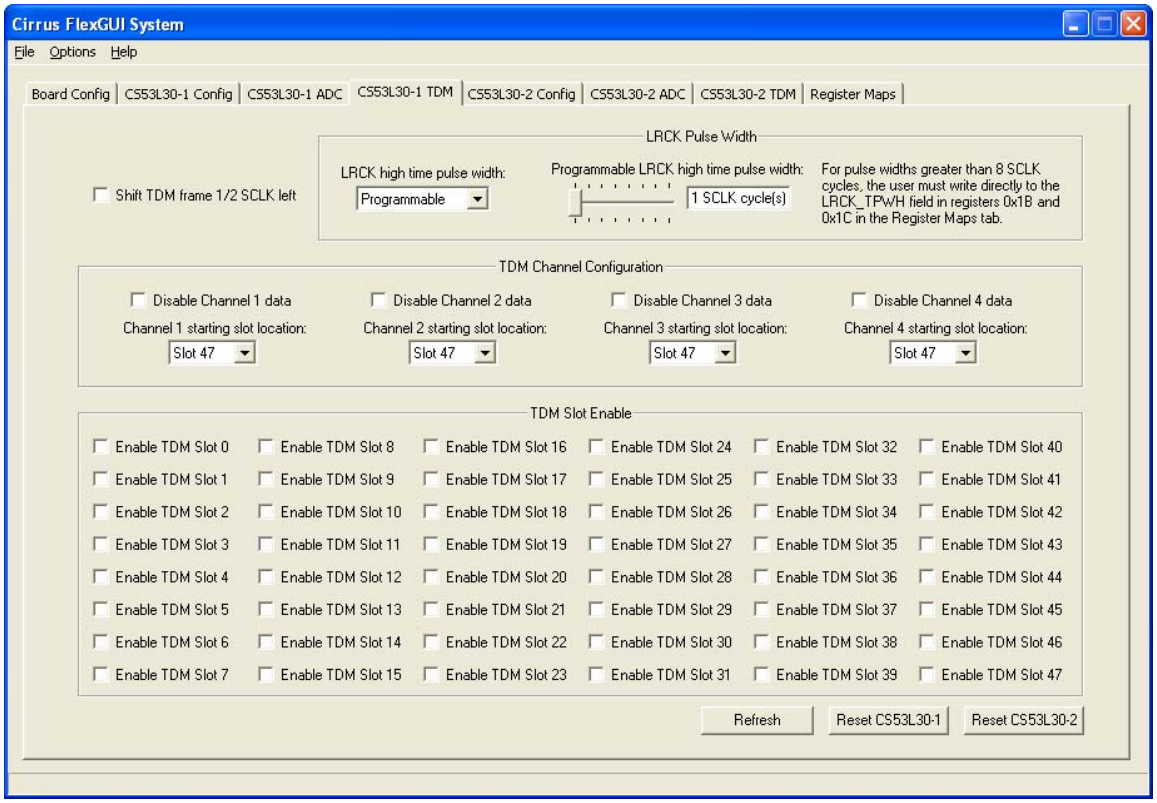


Figure 4-7. The “CS53L30 TDM” Tab

4.4 Register Maps Tab

The “Register Maps” tab shows the entire user configurable register space for all programmable devices on the CDB53L30. It is especially useful for reading/writing a device’s register settings directly, one register at a time. For example, the default value for register 0x10 is 0x2F (Figure 4-8). To modify register 0x10’s value, first navigate to it by locating the cell at the intersection of row “10” and column “00.” Click on the cell and simply type the desired hexadecimal value for that register, then press the return key (Enter) on the keyboard.

To modify one bit of a register at a time, navigate to the desired register cell, click it, then click on the applicable bits shown in the lower part of the register map page to toggle them.

Other useful controls:

- **Reset All**—Sends a reset pulse to all devices on the CDB53L30.
- **Reset Device**—Sends a reset pulse to the device currently in view in the register map.
- **Released Reset**—Holds/releases the device currently in view in the register map in/from reset.
- **Update Register**—Refreshes the current selected register value.
- **Update Device**—Refreshes all register values of the device currently in view in the register map.

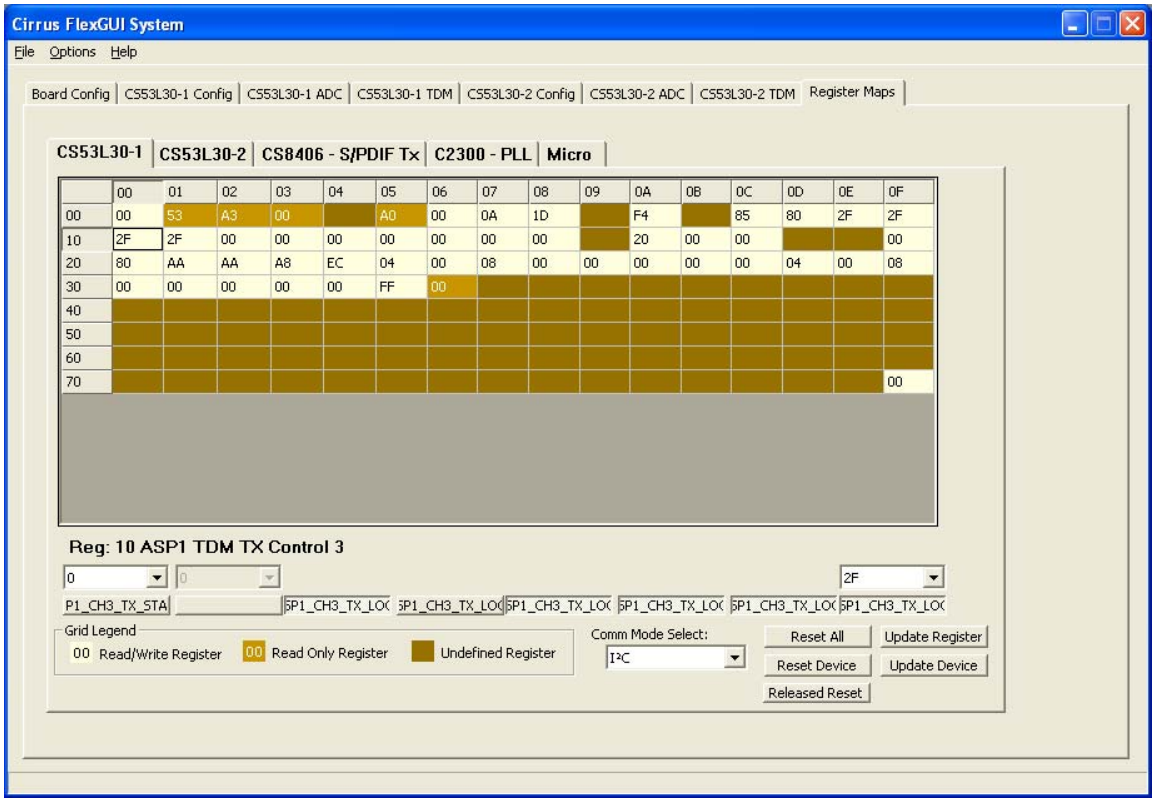


Figure 4-8. The “Register Maps” Tab

5 Performance Plots

Test conditions (unless otherwise specified): FS_{ext} = 48 kHz; $MCLK_{ext}$ = 12.2880 MHz; preamp setting: 0 dB (bypassed); PGA setting: 0 dB; high-pass filter enabled, ADCx_HPF_CF = 00; notch filter disabled; noise gate disabled; MCLK autoscale enabled; VA = 1.8 V, VP = 3.6 V. THD+N measurement bandwidth = 10 Hz to $FS_{ext}/2$, no weighting. Unless otherwise specified, the performance data is representative of all channels on both CS53L30 devices.

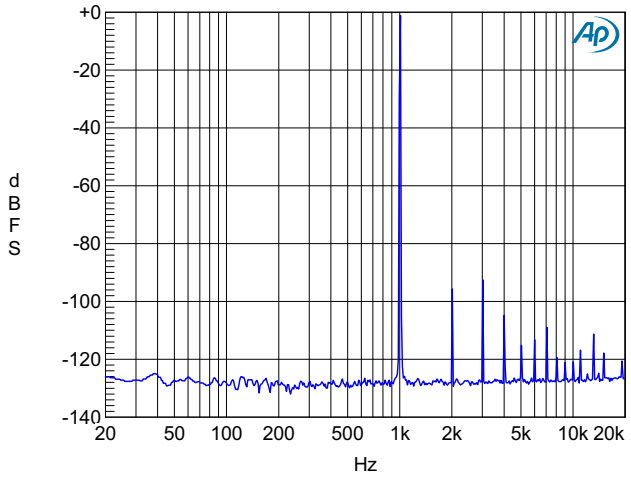


Figure 5-1. Output FFT, Preamp Setting: 0 dB, PGA Setting: 0 dB, 1 kHz, –1 dBFS

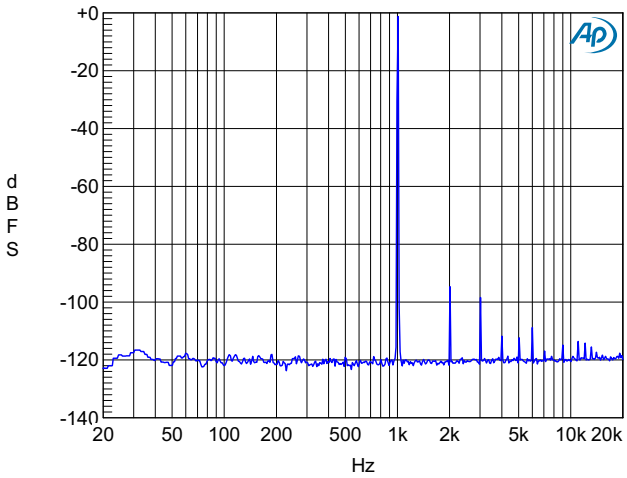


Figure 5-2. Output FFT, Preamp Setting: 0 dB, PGA Setting: +12 dB, 1 kHz, –1 dBFS

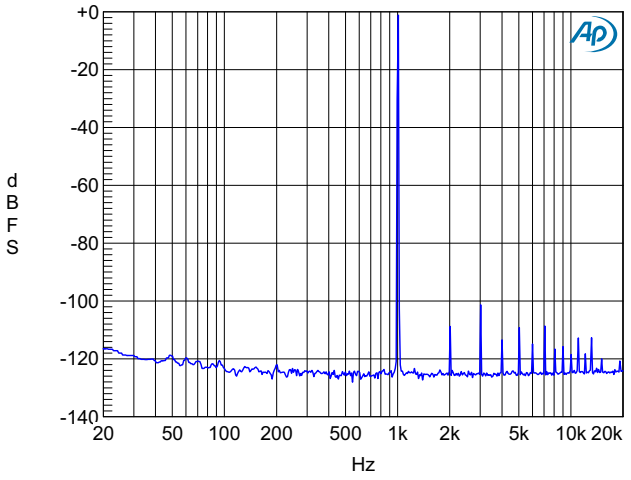


Figure 5-3. Output FFT, Preamp Setting: +10 dB, PGA Setting: 0 dB, 1 kHz, –1 dBFS

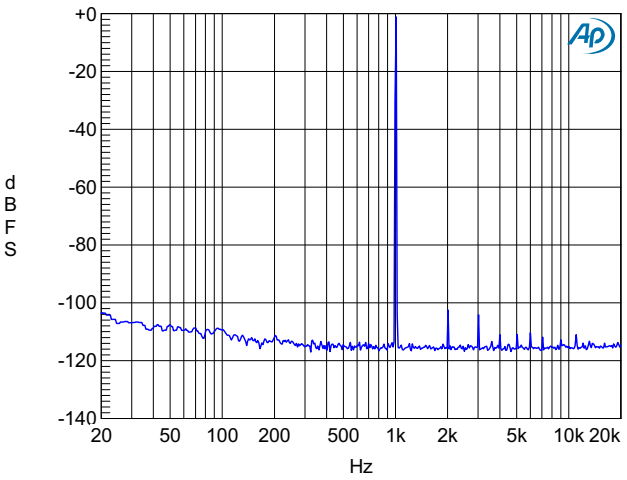


Figure 5-4. Output FFT, Preamp Setting: +10 dB, PGA Setting: +12 dB, 1 kHz, –1 dBFS

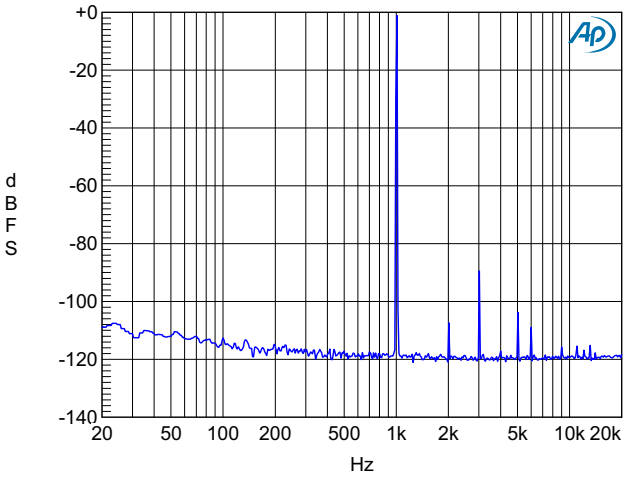


Figure 5-5. Output FFT, Preamp Setting: +20 dB, PGA Setting: 0 dB, 1 kHz, –1 dBFS

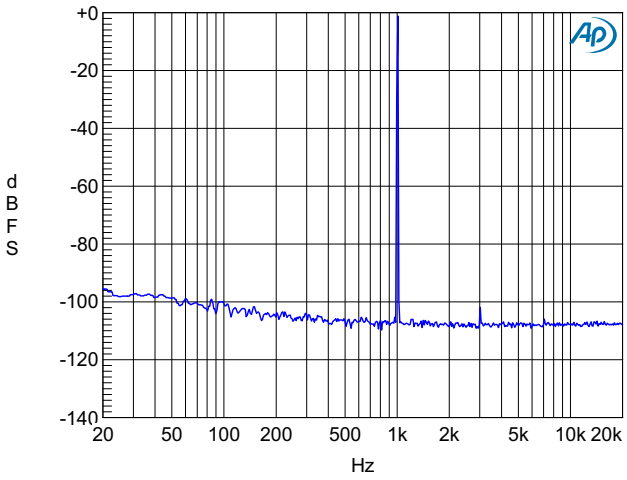


Figure 5-6. Output FFT, Preamp Setting: +20 dB, PGA Setting: +12 dB, 1 kHz, –1 dBFS

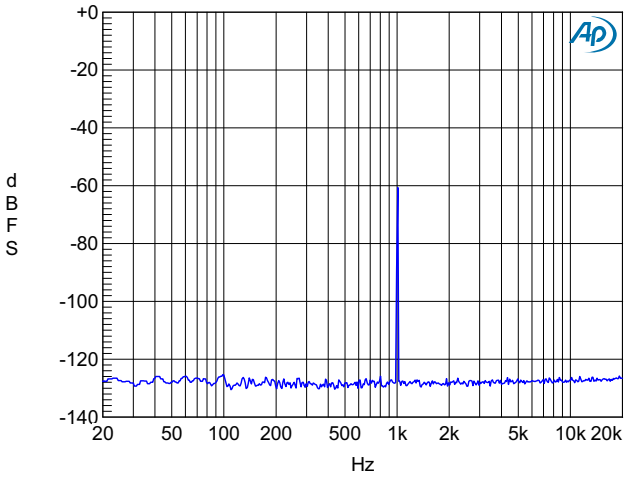


Figure 5-7. Output FFT, 1 kHz, –60 dBFS

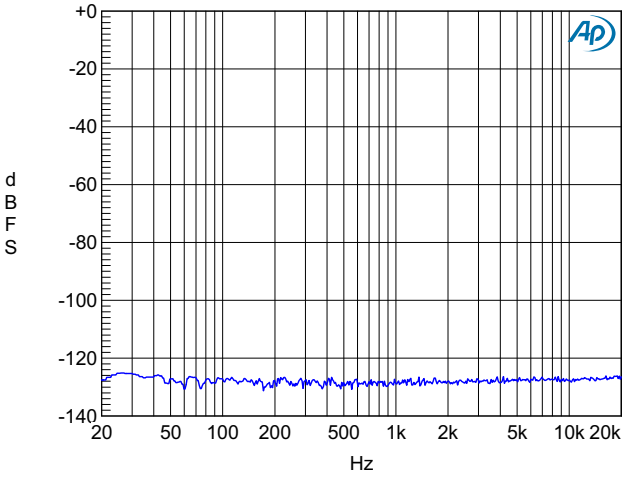


Figure 5-8. Output FFT, No Input

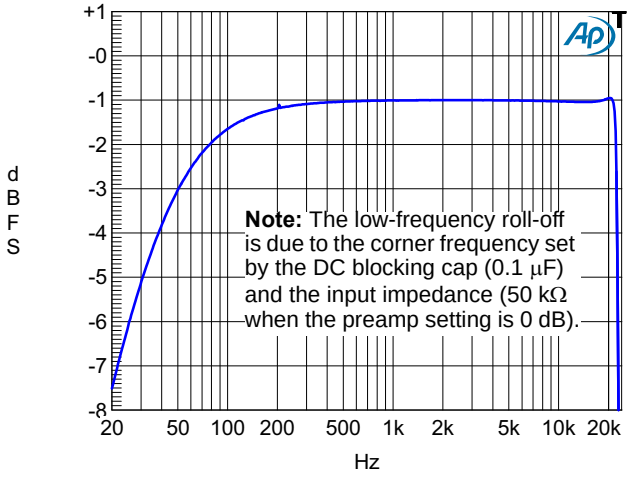


Figure 5-9. Frequency Response, Notch Filter Disabled, Preamp Bypassed (0 dB), –1 dBFS

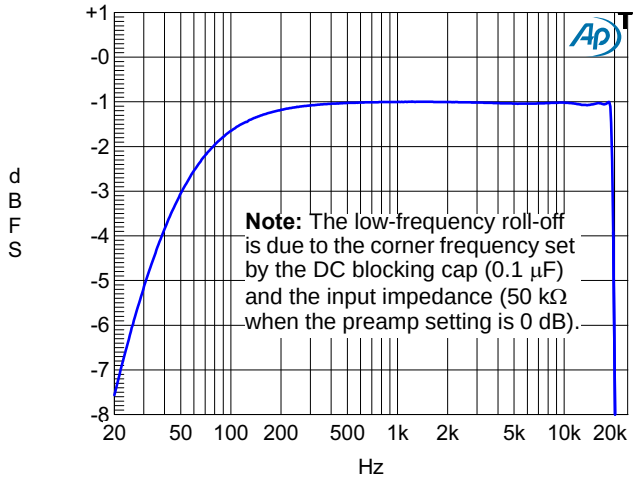


Figure 5-10. Frequency Response, Notch Filter Enabled, Preamp Bypassed (0 dB), –1 dBFS

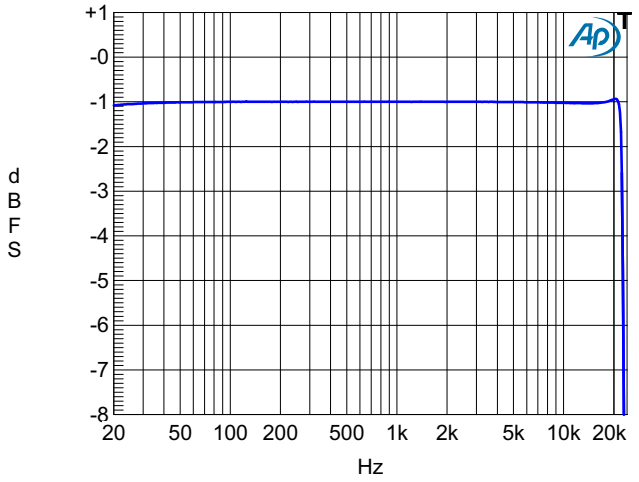


Figure 5-11. Frequency Response, Notch Filter Disabled, Preamp Enabled (+10 dB or +20 dB), –1 dBFS

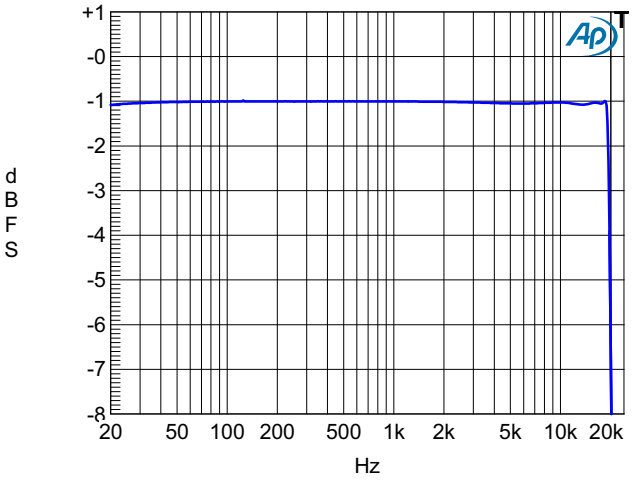


Figure 5-12. Frequency Response, Notch Filter Enabled, Preamp Enabled (+10 dB or +20 dB), –1 dBFS

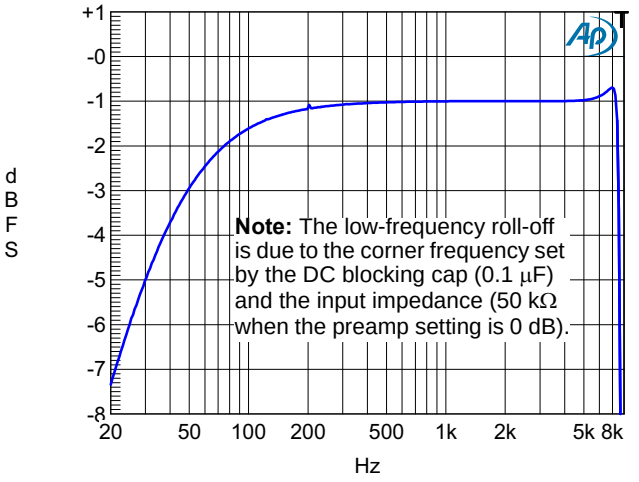


Figure 5-13. Frequency Response, FS_{ext} = 8 kHz, Notch Filter Disabled, Preamp Bypassed (0 dB), –1 dBFS

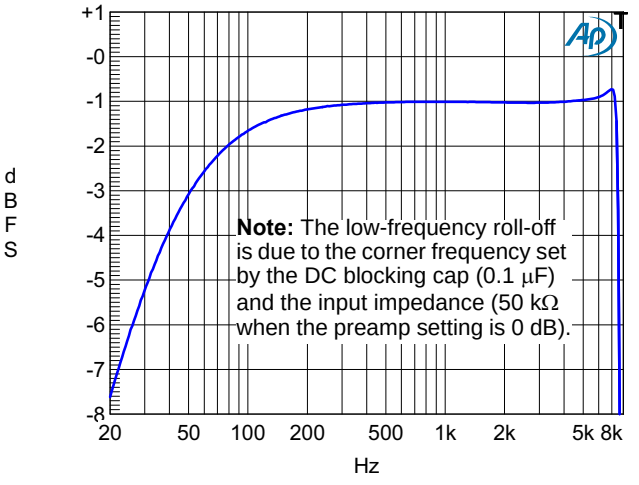


Figure 5-14. Frequency Response, FS_{ext} = 8 kHz, Notch Filter Enabled, Preamp Bypassed (0 dB), –1 dBFS

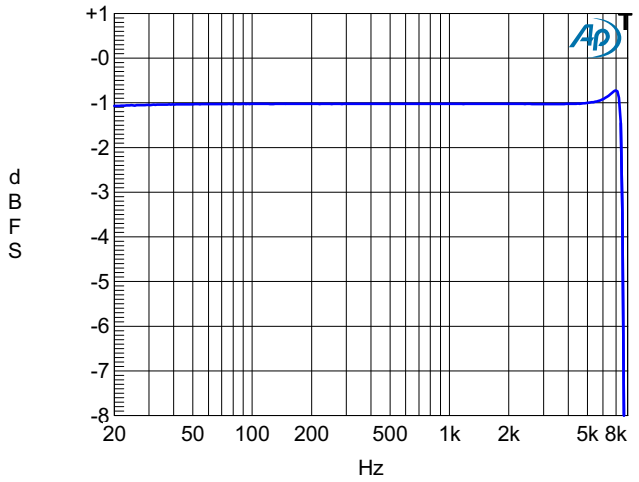


Figure 5-15. Frequency Response, FS_{ext} = 8 kHz, Notch Filter Disabled, Preamp Enabled (+10 dB or +20 dB), –1 dBFS

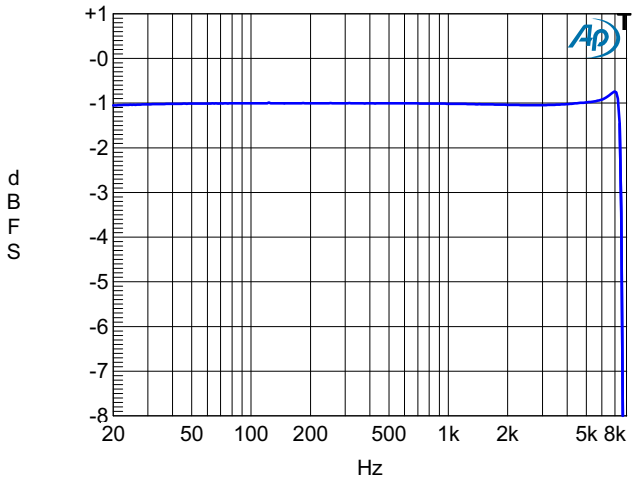


Figure 5-16. Frequency Response, FS_{ext} = 8 kHz, Notch Filter Enabled, Preamp Enabled (+10 dB or +20 dB), –1 dBFS

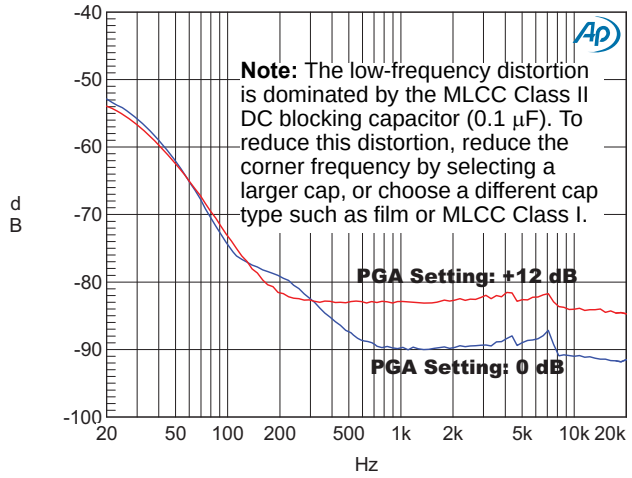


Figure 5-17. THD+N (Relative) vs. Frequency, Preamp Setting: 0 dB, –1 dBFS

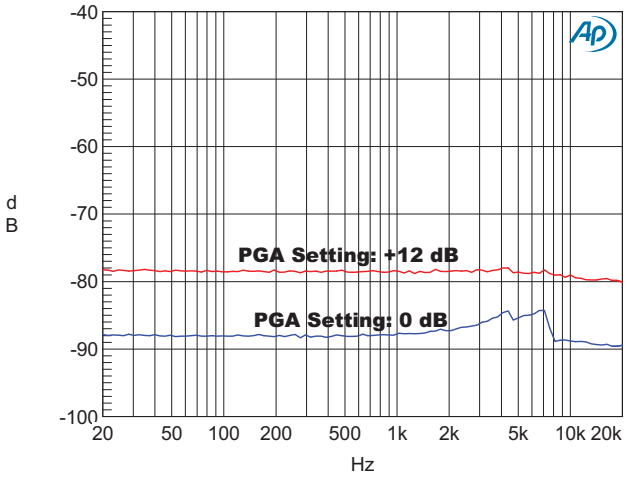


Figure 5-18. THD+N (Relative) vs. Frequency, Preamp Setting: +10 dB, –1 dBFS

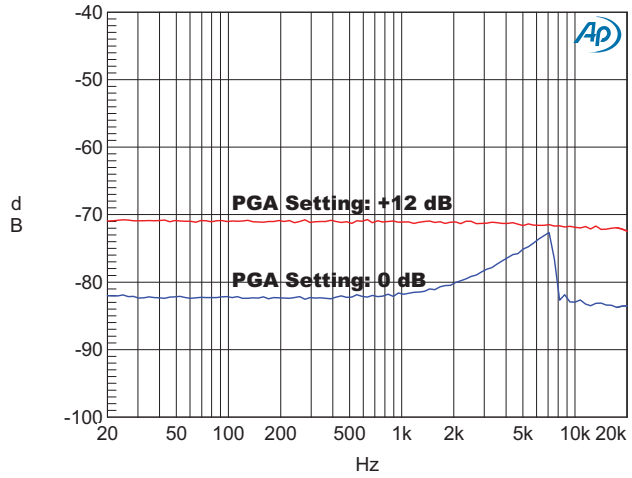


Figure 5-19. THD+N (Relative) vs. Frequency, Preamp Setting: +20 dB, –1 dBFS

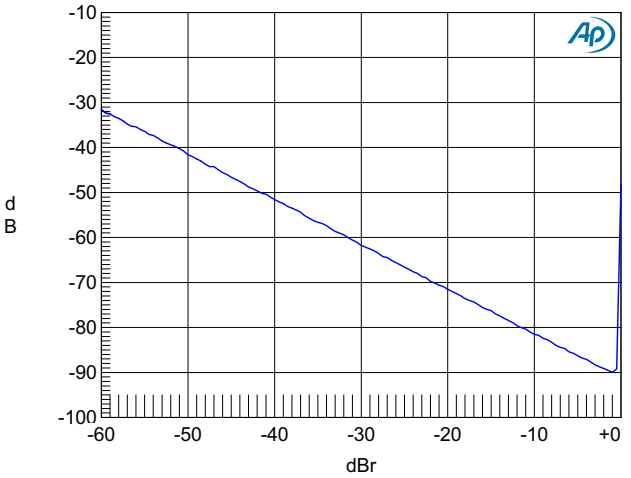


Figure 5-20. THD+N (Relative) vs. Level, Preamp Setting: 0 dB, PGA Setting: 0 dB, 1 kHz

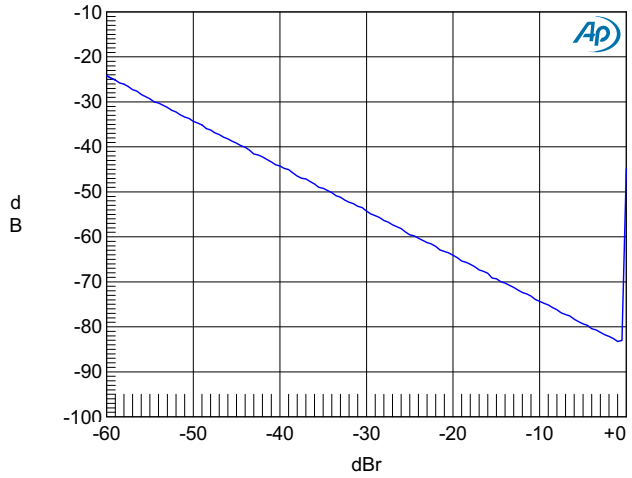


Figure 5-21. THD+N (Relative) vs. Level, Preamp Setting: 0 dB, PGA Setting: +12 dB, 1 kHz

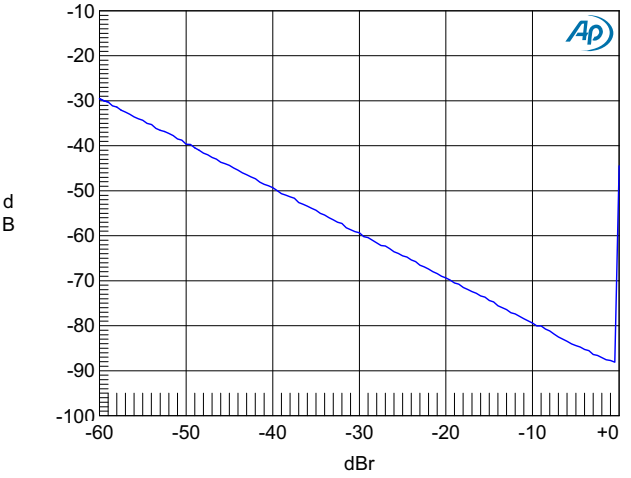


Figure 5-22. THD+N (Relative) vs. Level, Preamp Setting: +10 dB, PGA Setting: 0 dB, 1 kHz

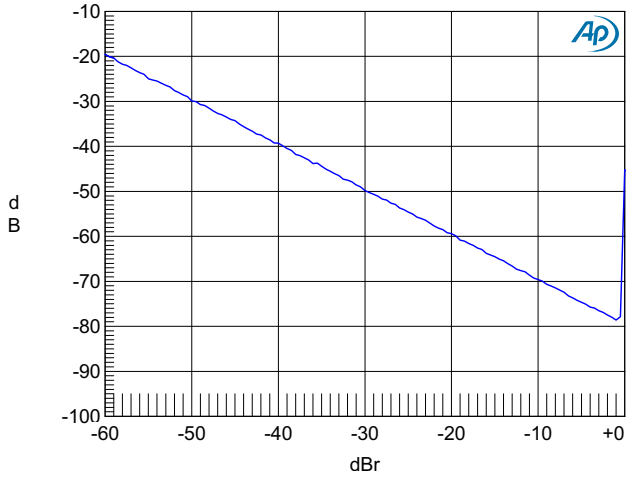


Figure 5-23. THD+N (Relative) vs. Level, Preamp Setting: +10 dB, PGA Setting: +12 dB, 1 kHz

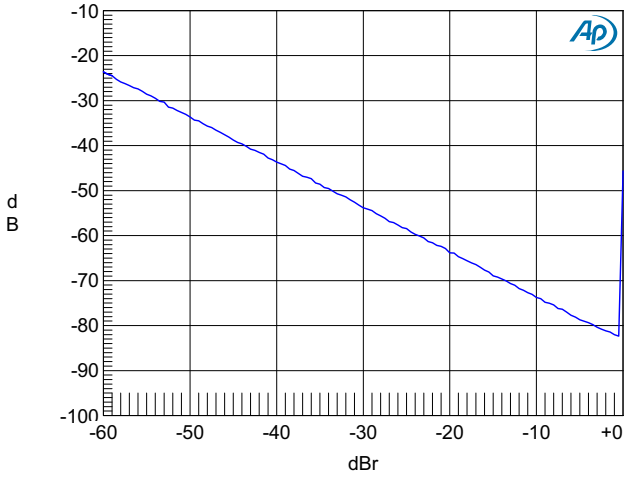


Figure 5-24. THD+N (Relative) vs. Level, Preamp Setting: +20 dB, PGA Setting: 0 dB, 1 kHz

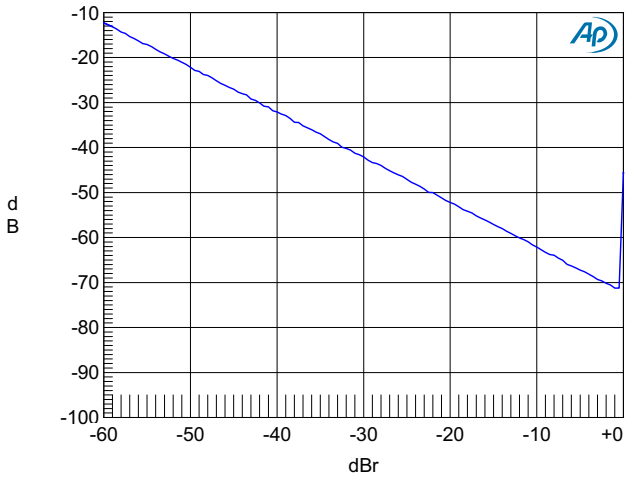


Figure 5-25. THD+N (Relative) vs. Level, Preamp Setting: +20 dB, PGA Setting: +12dB, 1 kHz

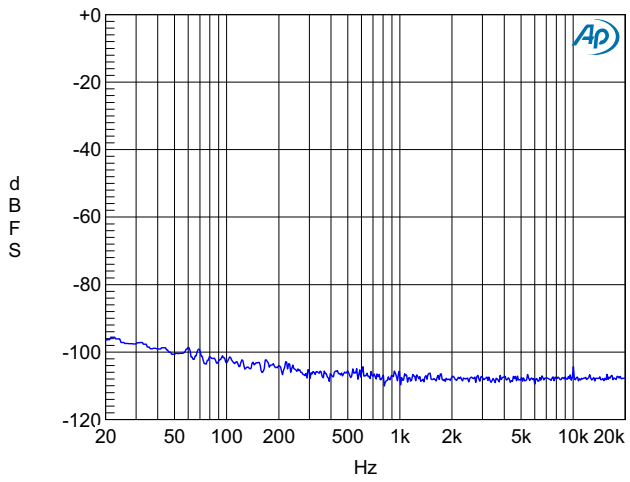


Figure 5-26. FFT, Adjacent Channel Crosstalk at 10 kHz, Preamp Setting: +20 dB, PGA Setting: +12 dB, –1 dBFS

6 Schematics

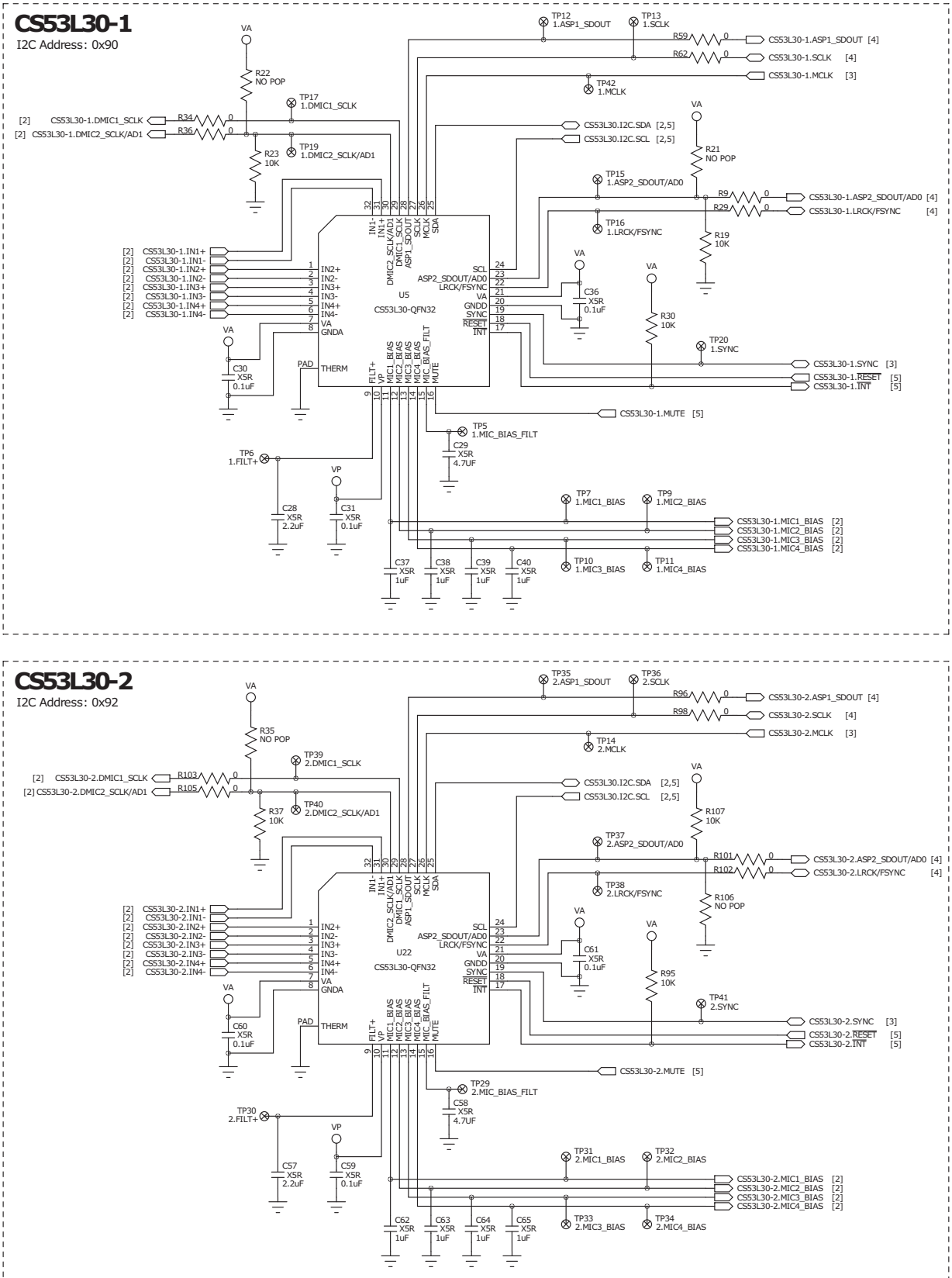
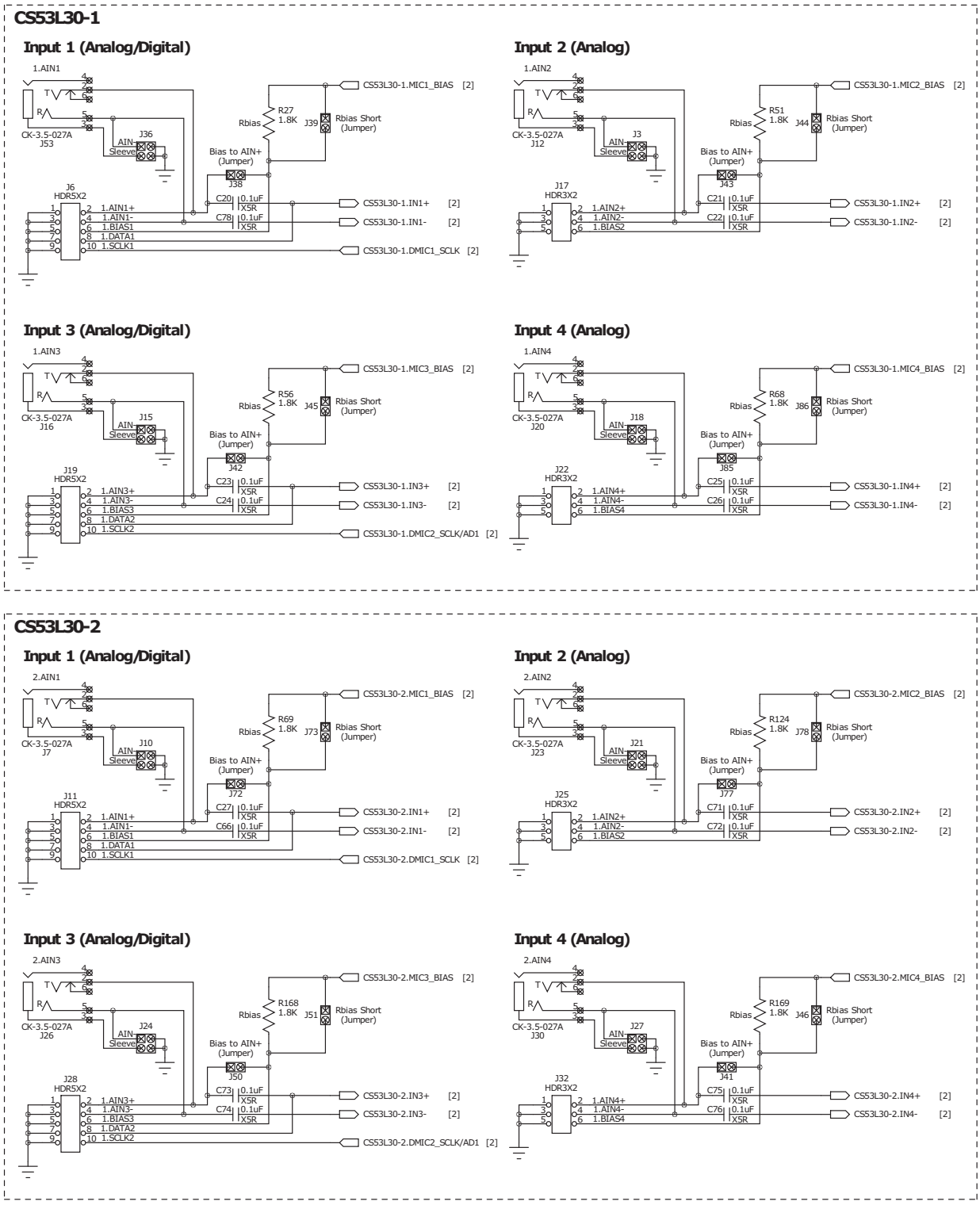


Figure 6-1. CS53L30

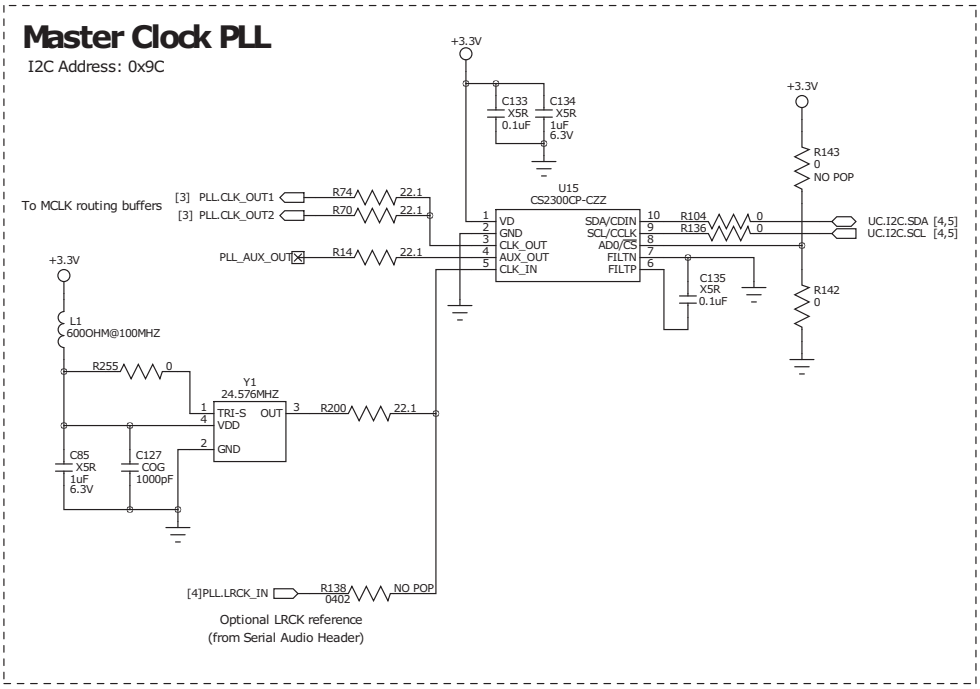


DC Blocking Capacitors

The value of the DC blocking capacitor can be modified according to the desired high-pass corner frequency, determined by the CS53L30 input impedance. Several example calculations are shown in the table below.

Preamp Setting	CS53L30 Input Impedance	DC Blocking Capacitor	High-Pass Corner Freq
Bypass	50k	0.1 uF	31.8 Hz
+10 or +20	1M	0.1 uF	1.6 Hz
+10 or +20	1M	0.01 uF	15.9 Hz

Figure 6-2. Inputs



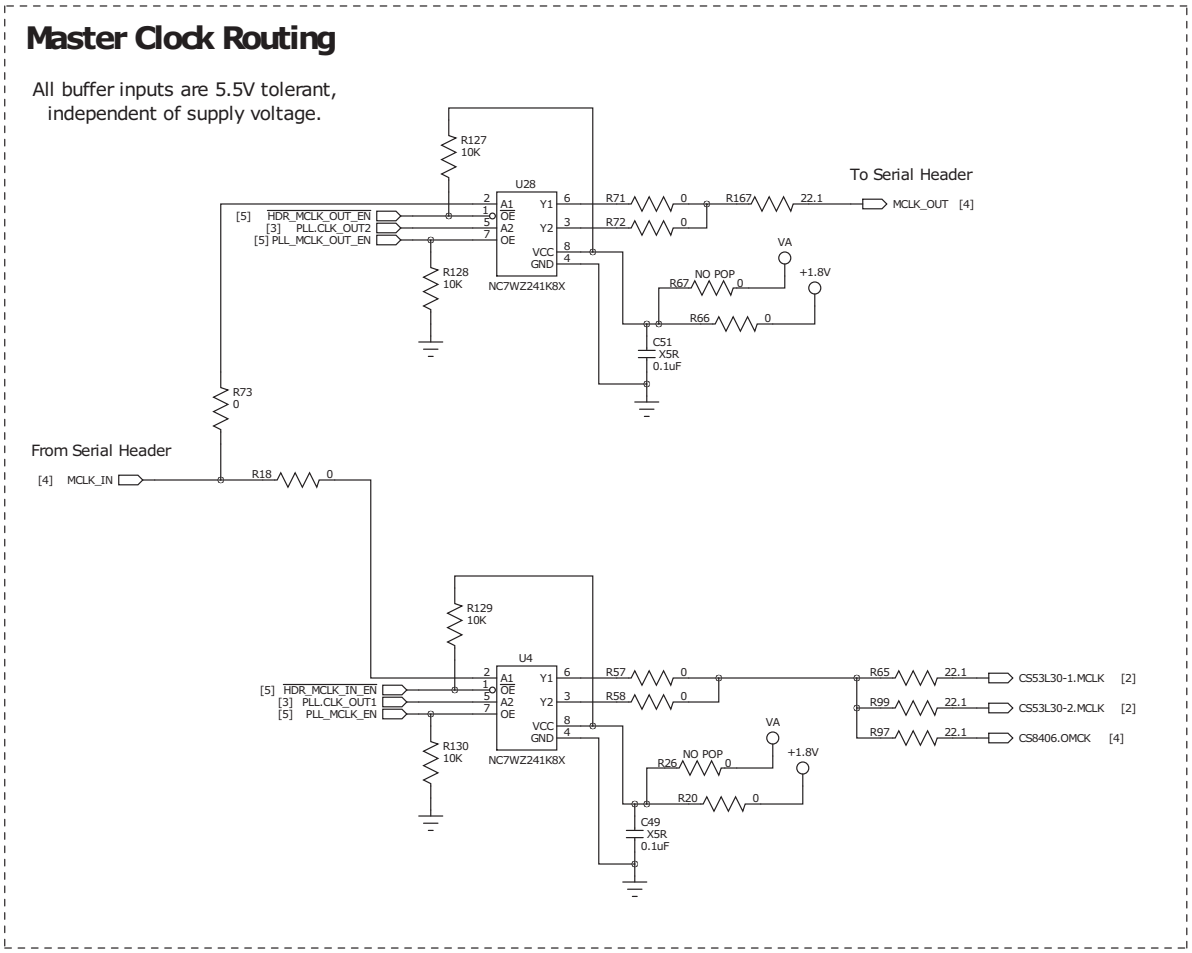
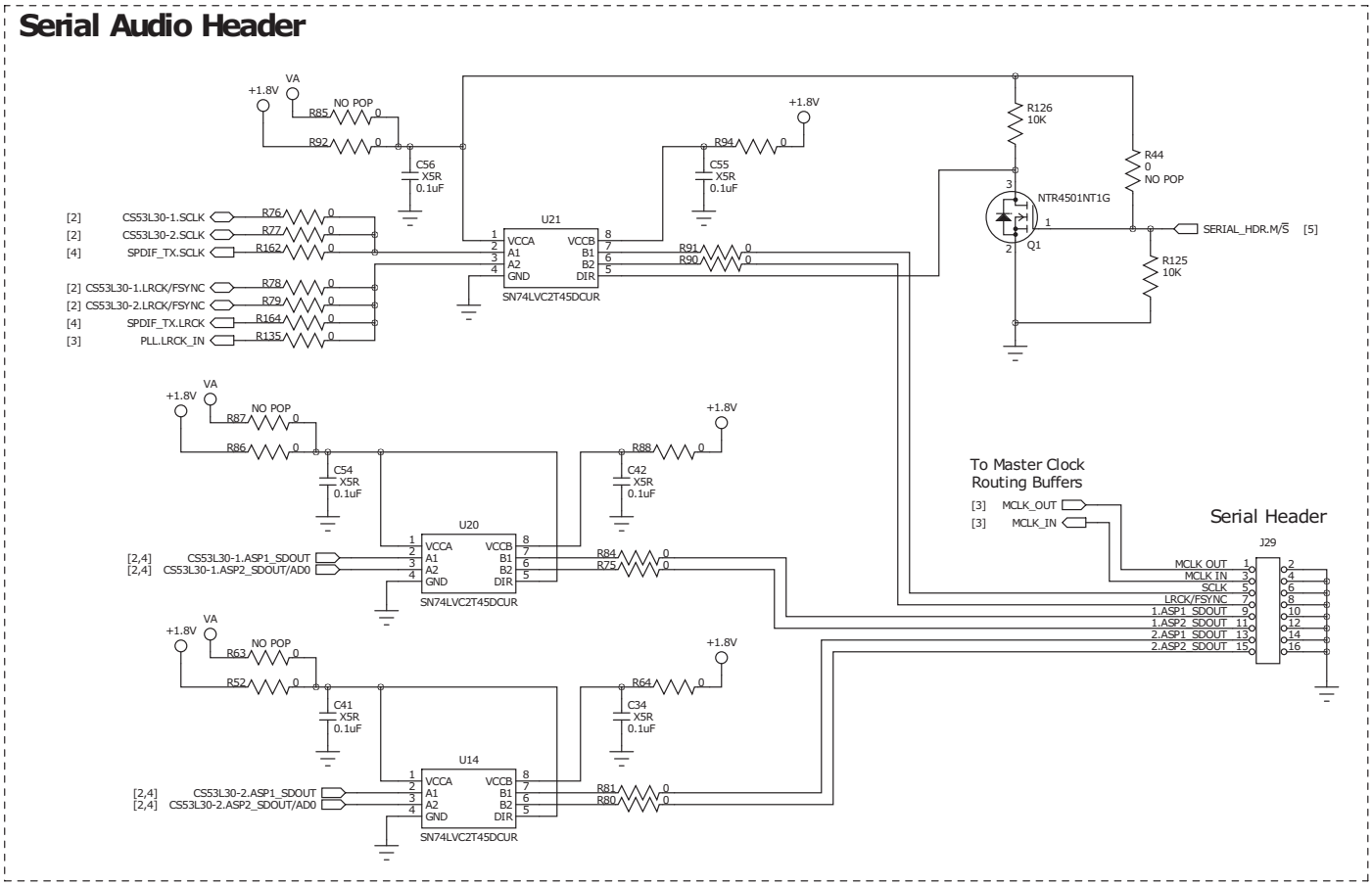


Figure 6-3. Master Clock PLL and Routing Buffers



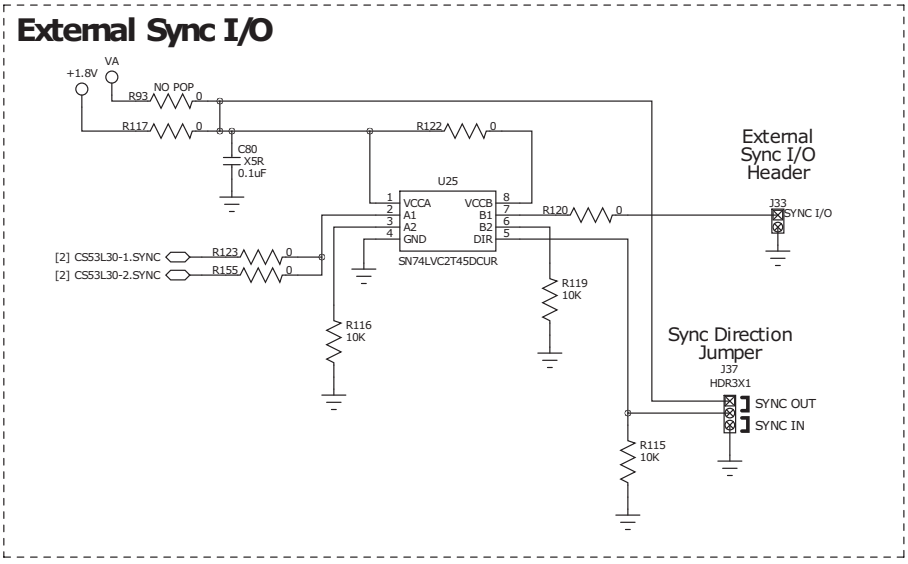


Figure 6-4. Serial Audio Header, Sync I/O

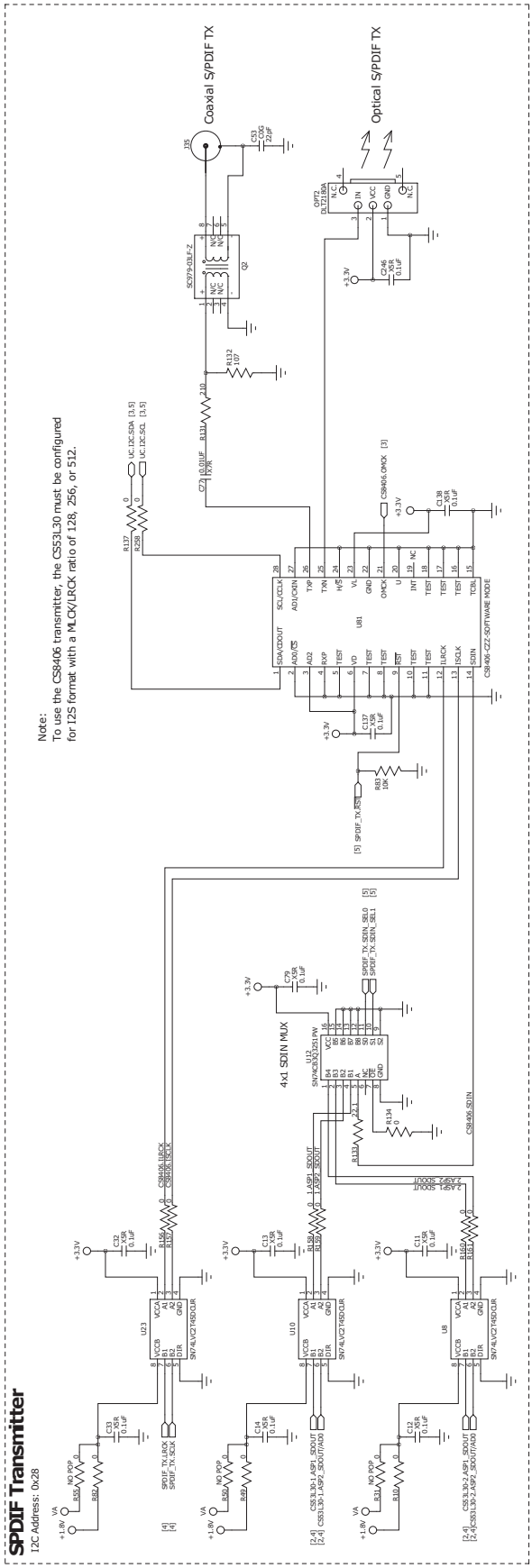


Figure 6-5. S/PDIF Transmitter

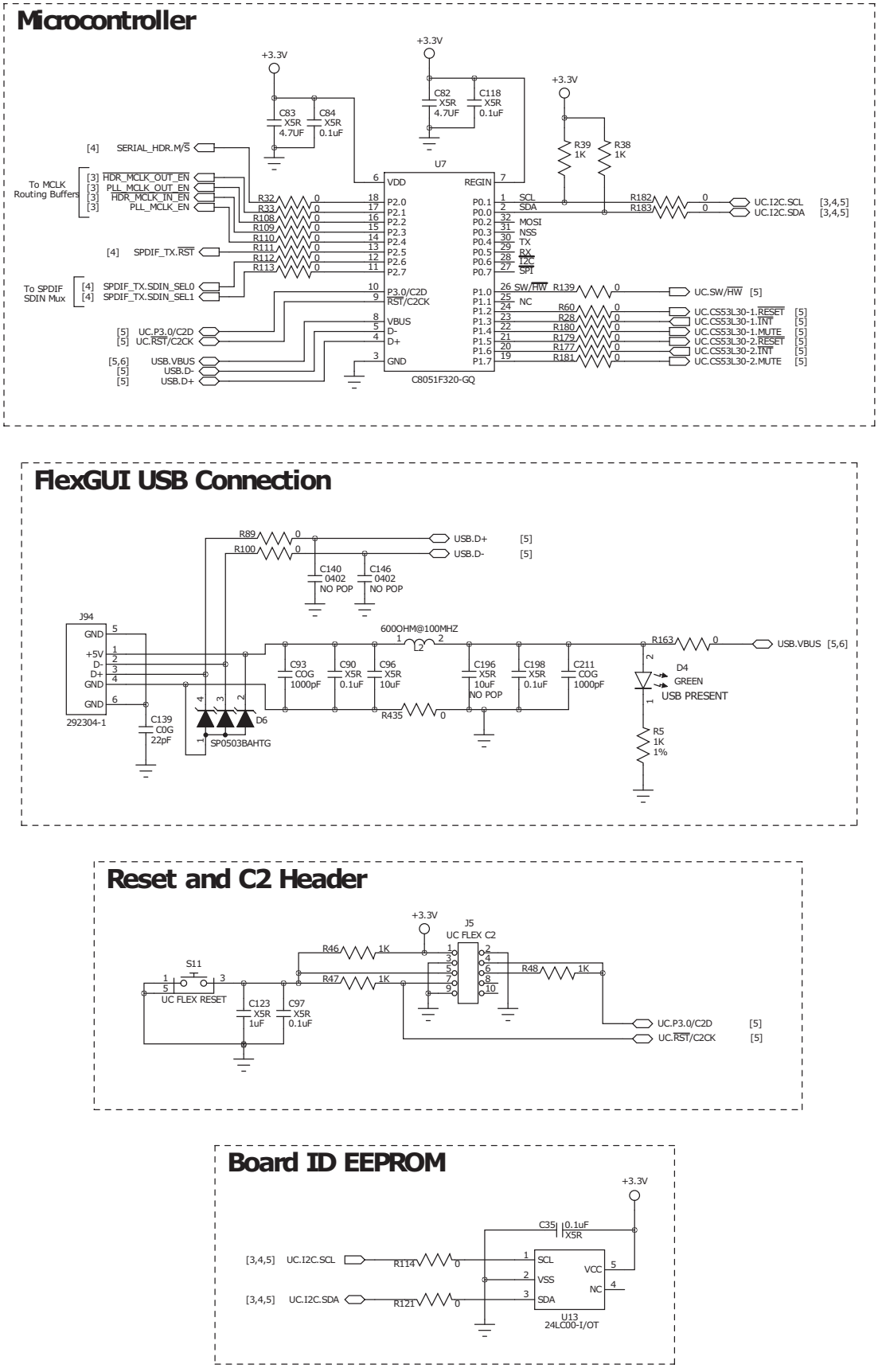


Figure 6-6. Microcontroller

Level Shifters and Control I/O Header

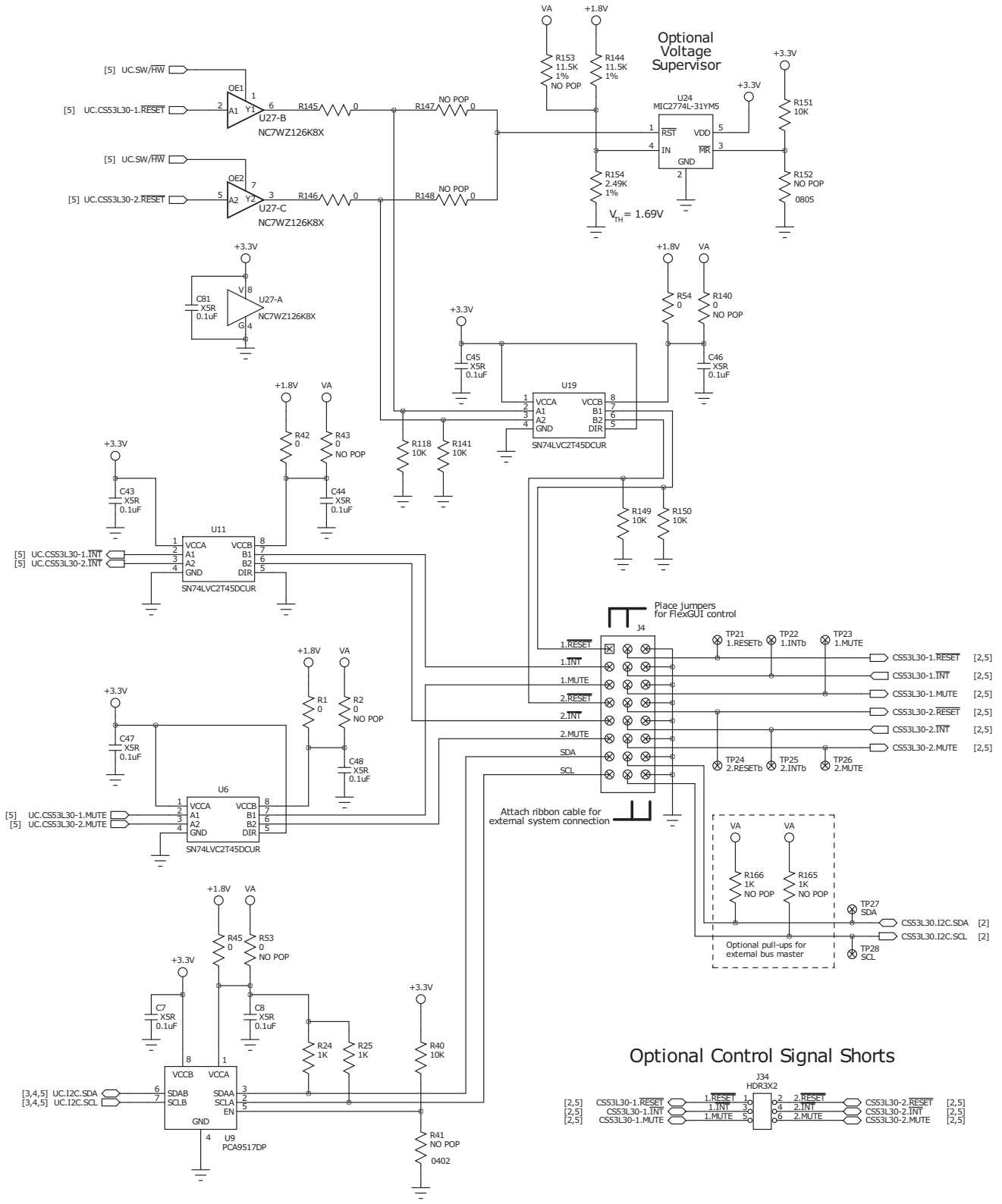
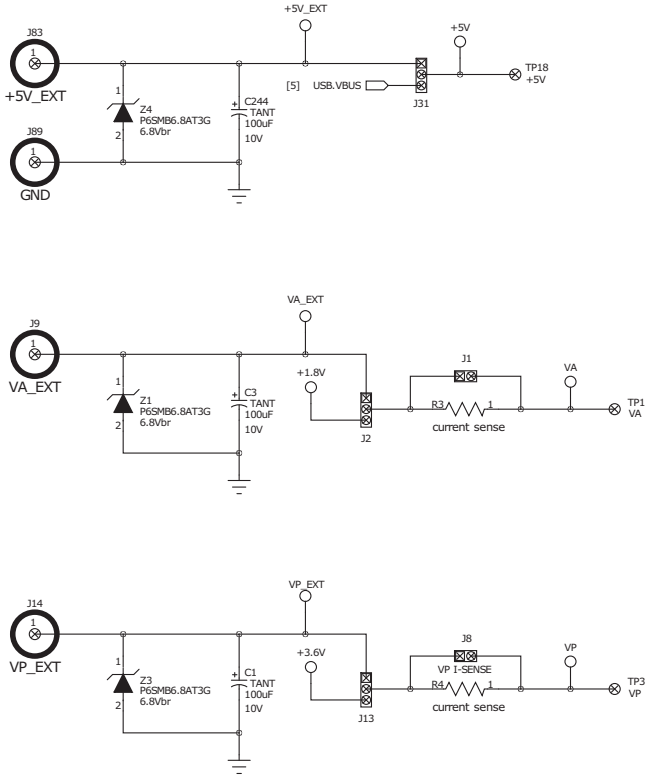
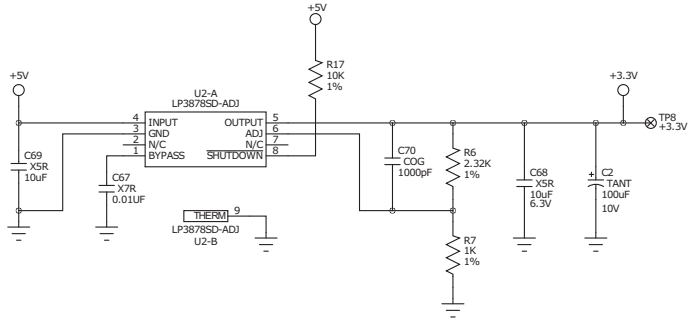


Figure 6-7. Level Shifters, Control I/O Header

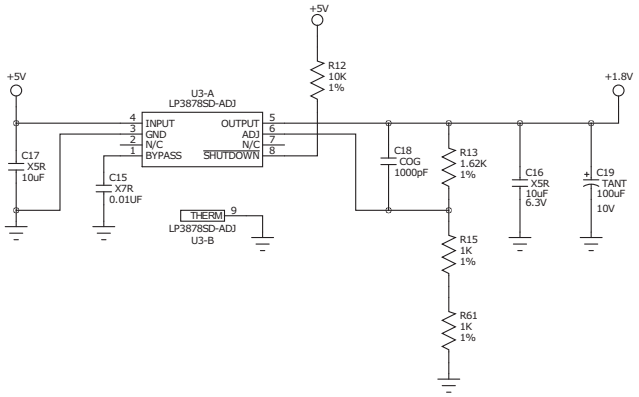
Power Supply Binding Posts



+5.0V to +3.3V LDO: Digital



+5.0V to +1.8V LDO: VA



+5.0V to +3.6V LDO: VP

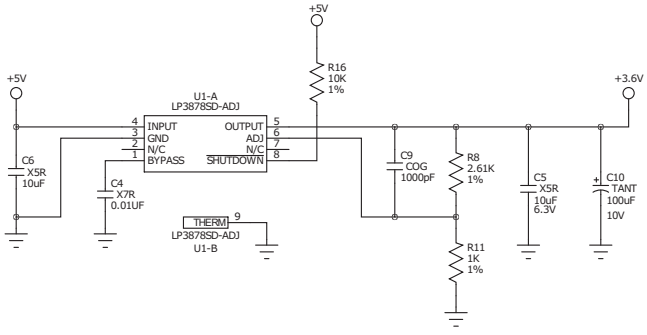


Figure 6-8. Power Supply

7 Layout

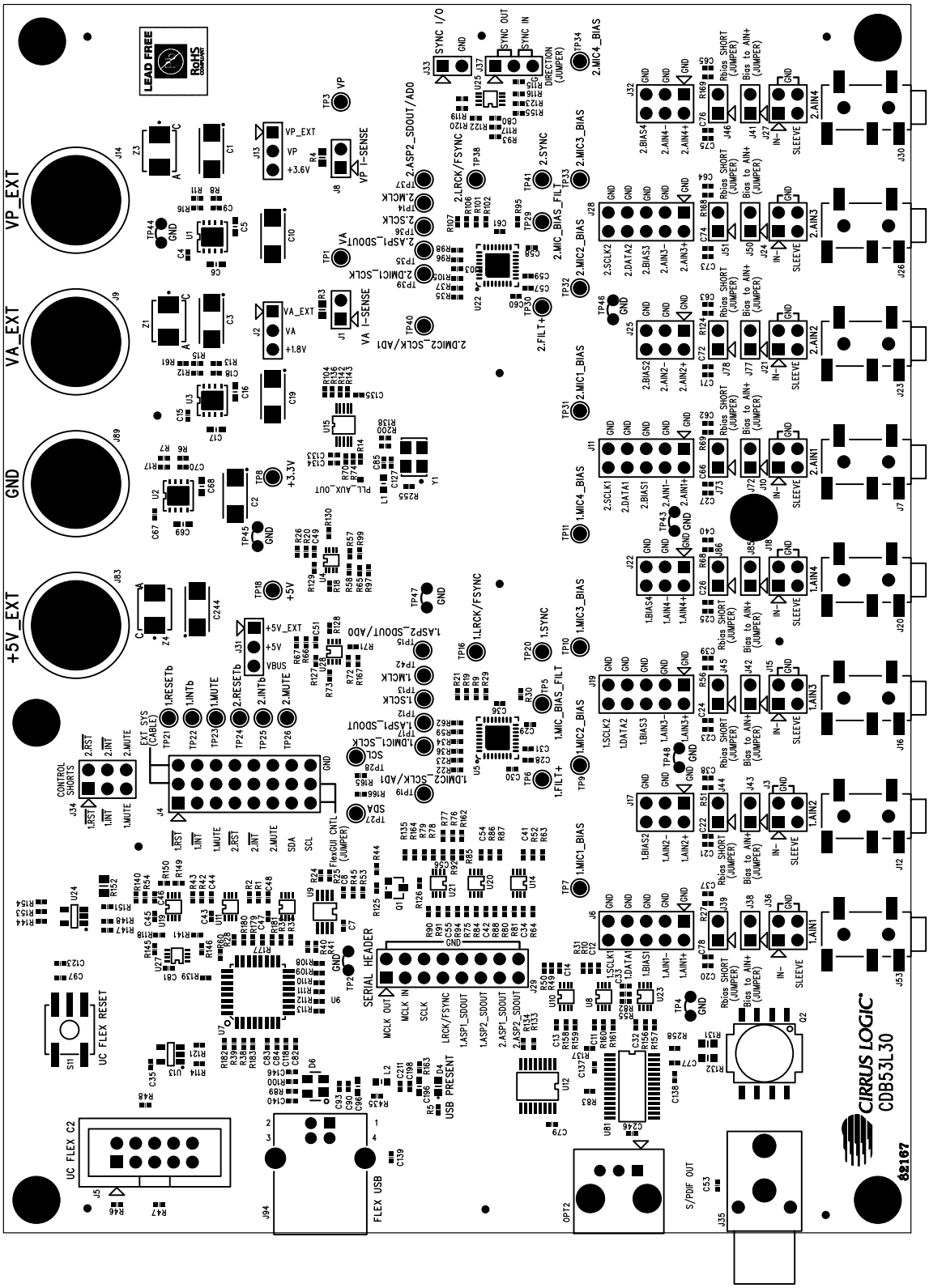


Figure 7-1. Assembly Drawing (Top Side)

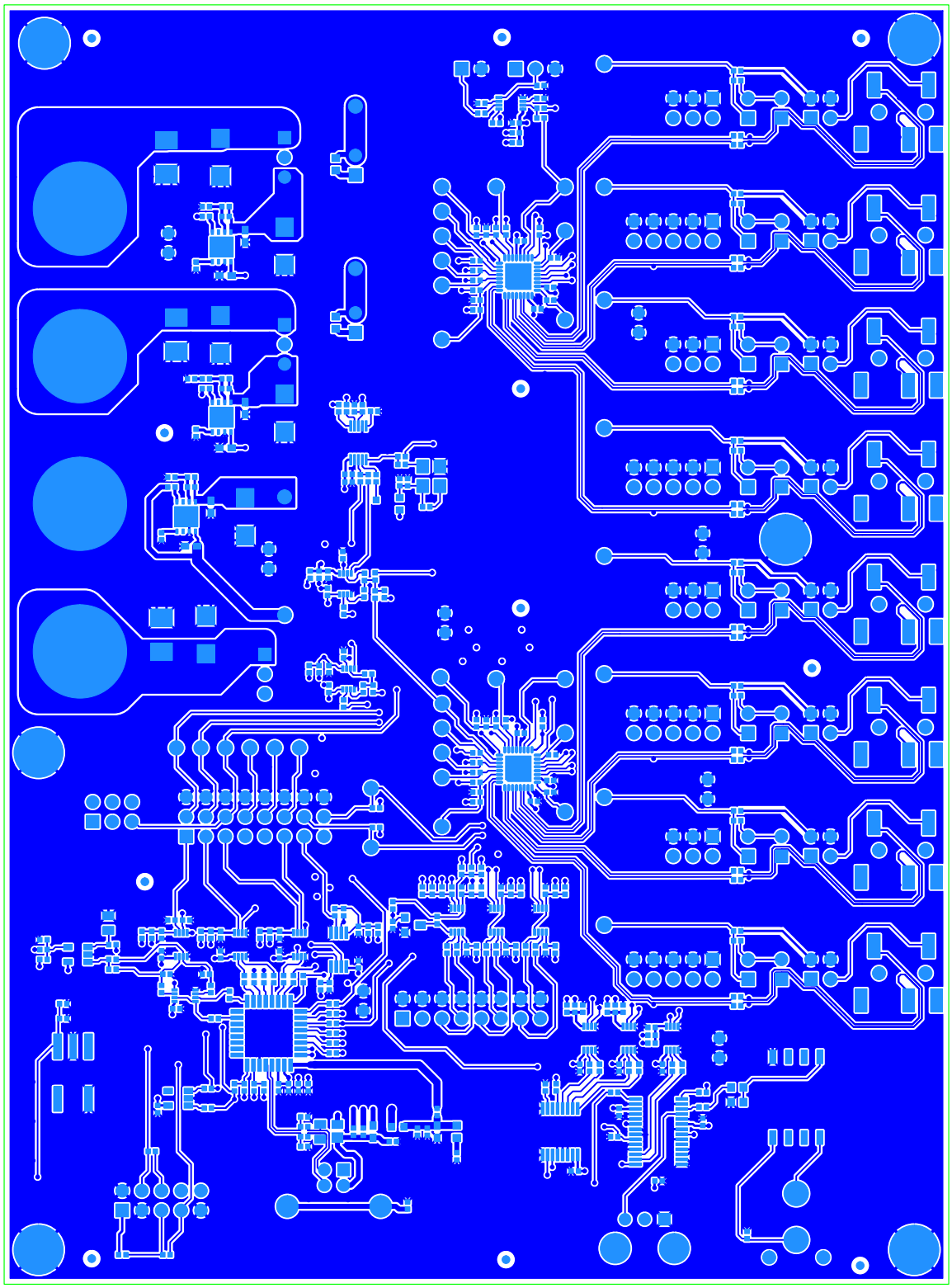


Figure 7-2. Layer 1 (Component, Signal—Top)

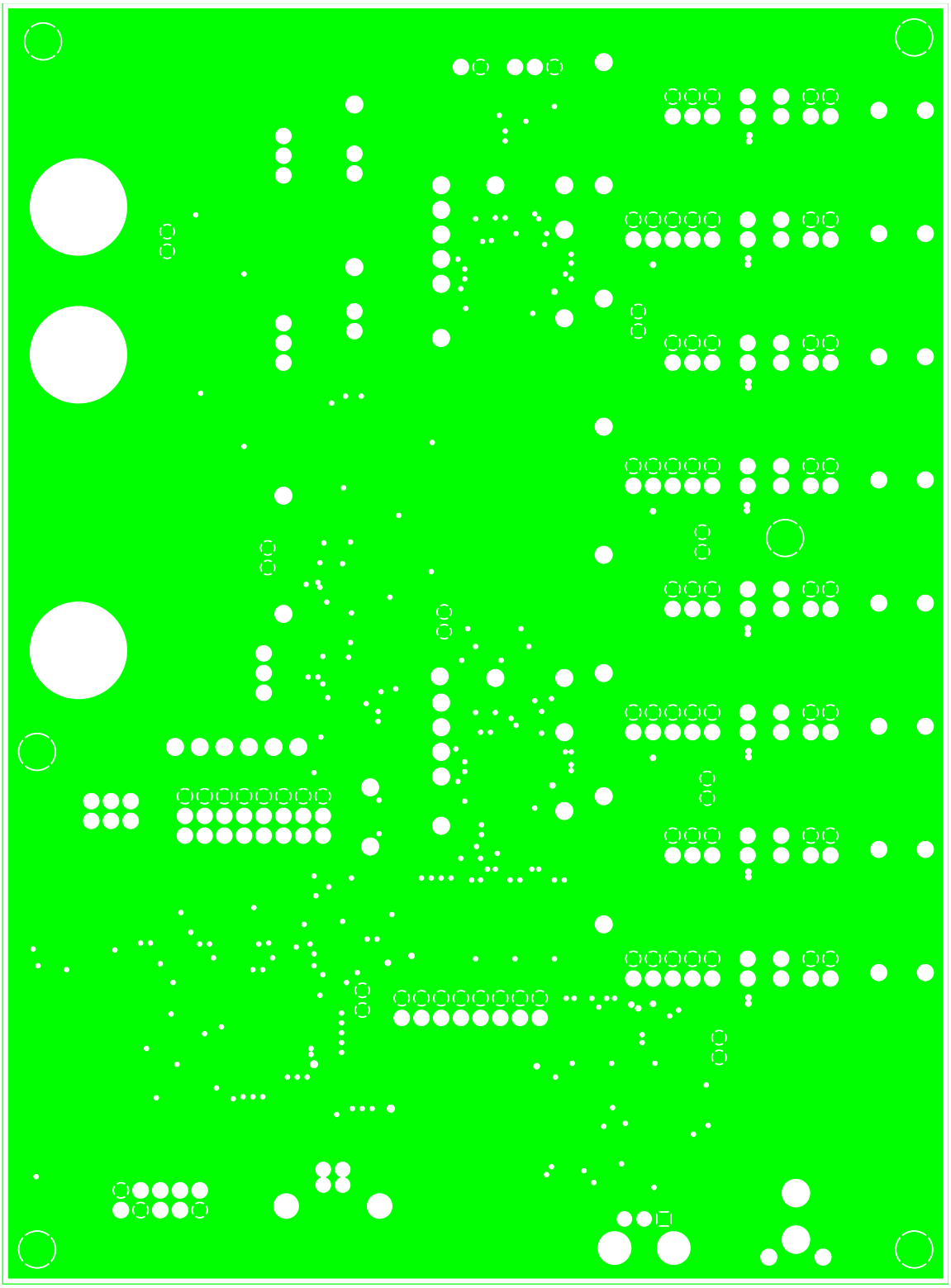


Figure 7-3. Layer 2 (Ground)

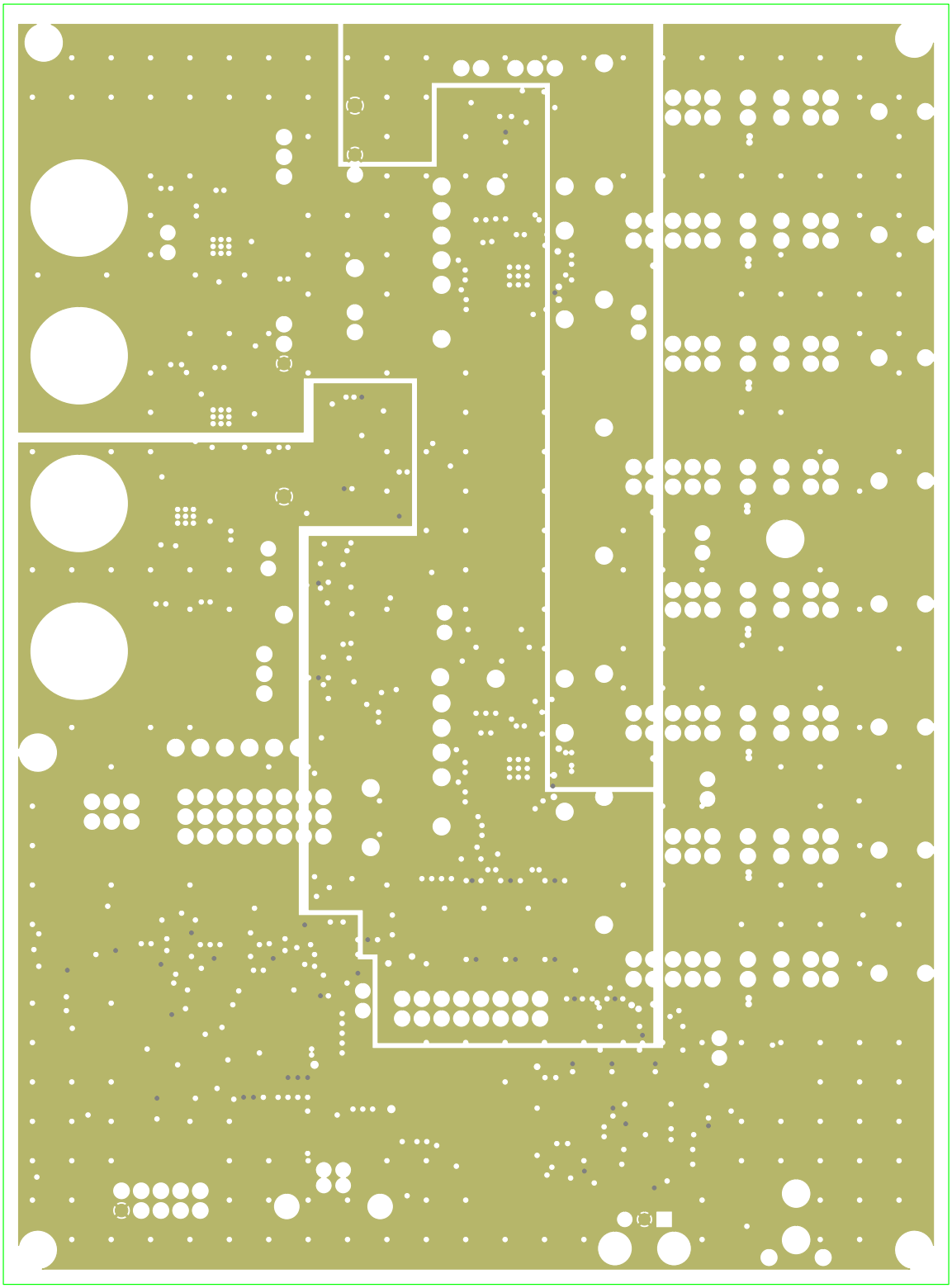


Figure 7-4. Layer 3 (+3.3 V, +1.8 V, VP)

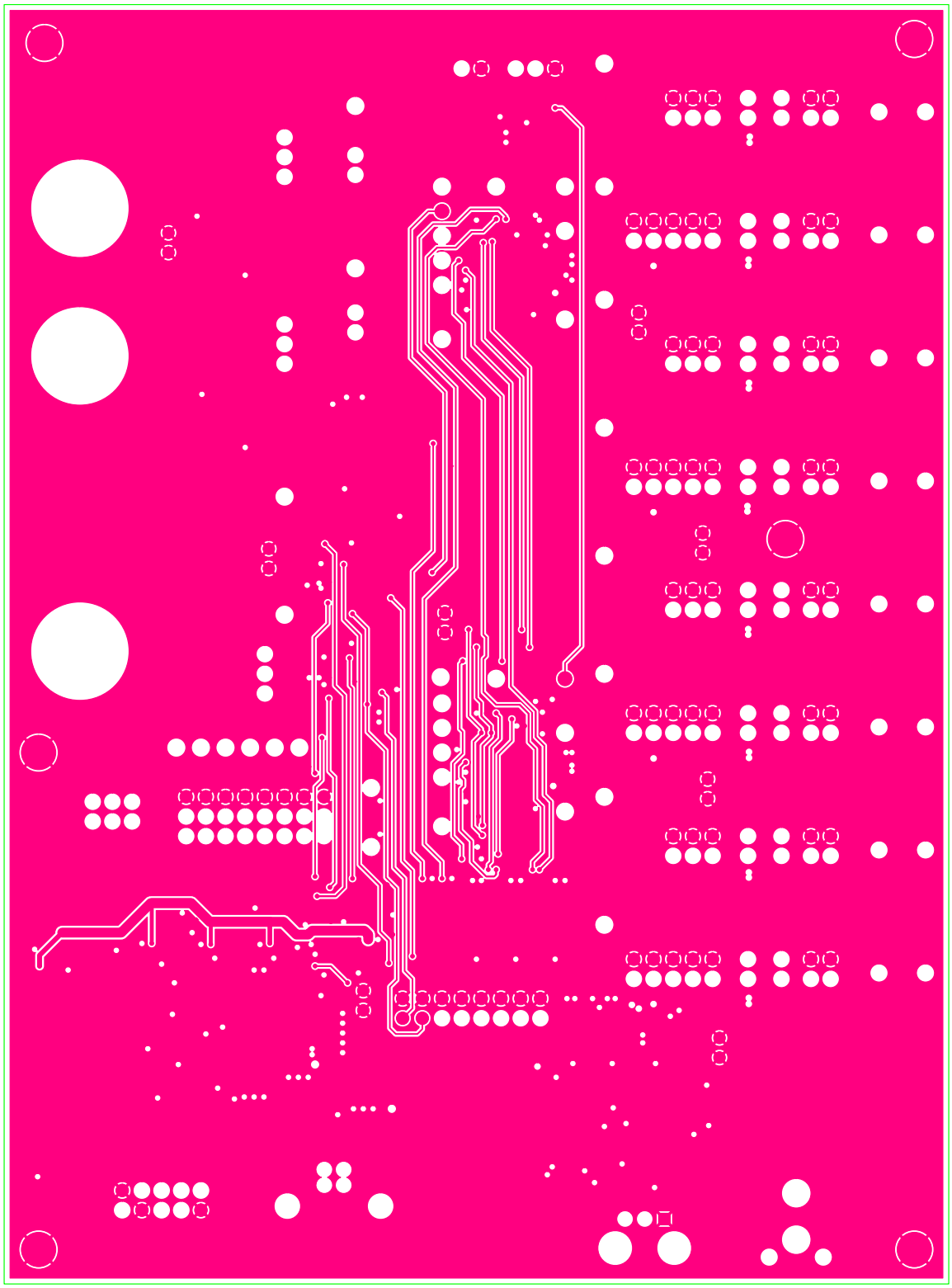


Figure 7-5. Layer 4 (Signal)

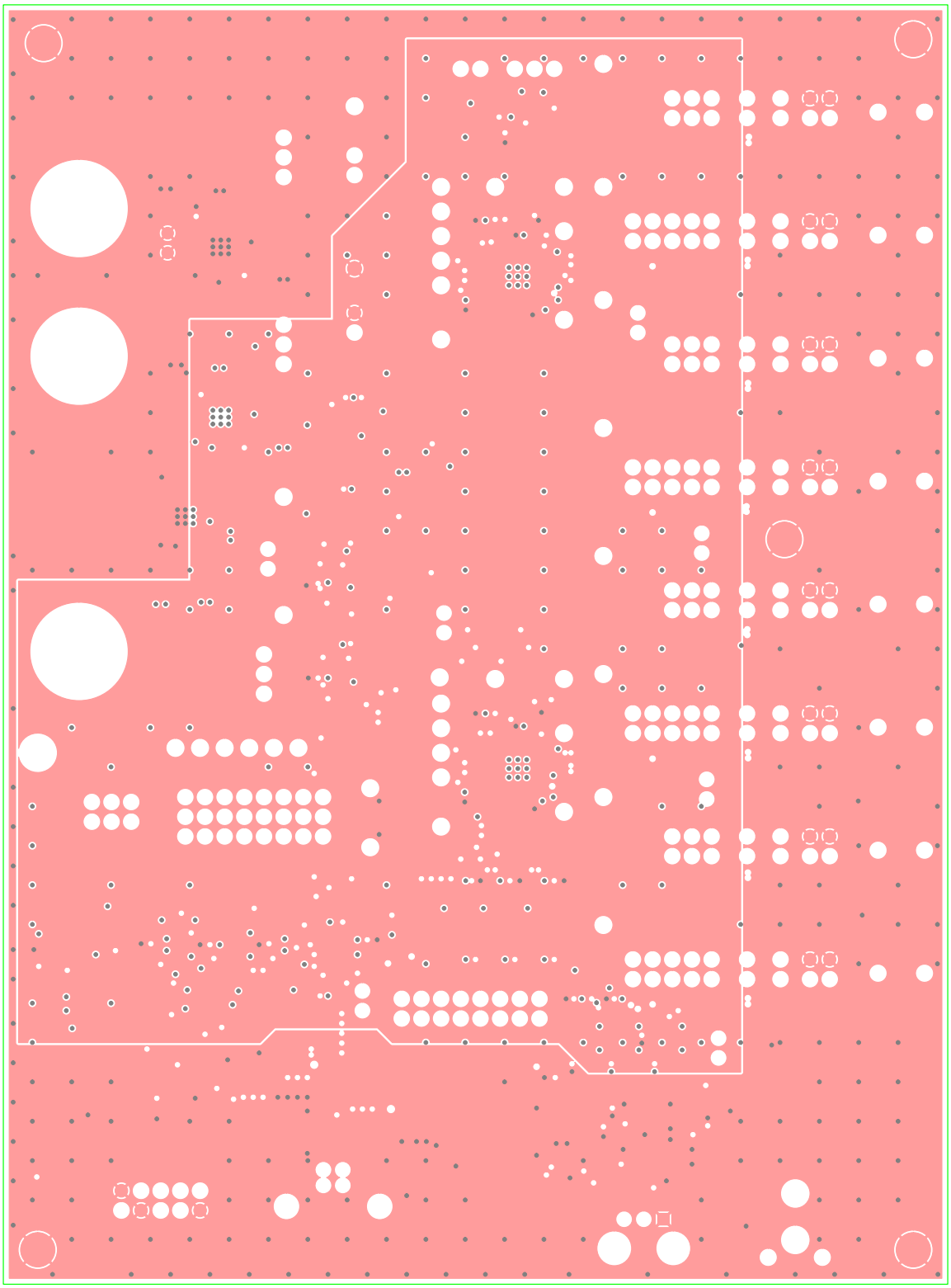


Figure 7-6. Layer 5 (VA)

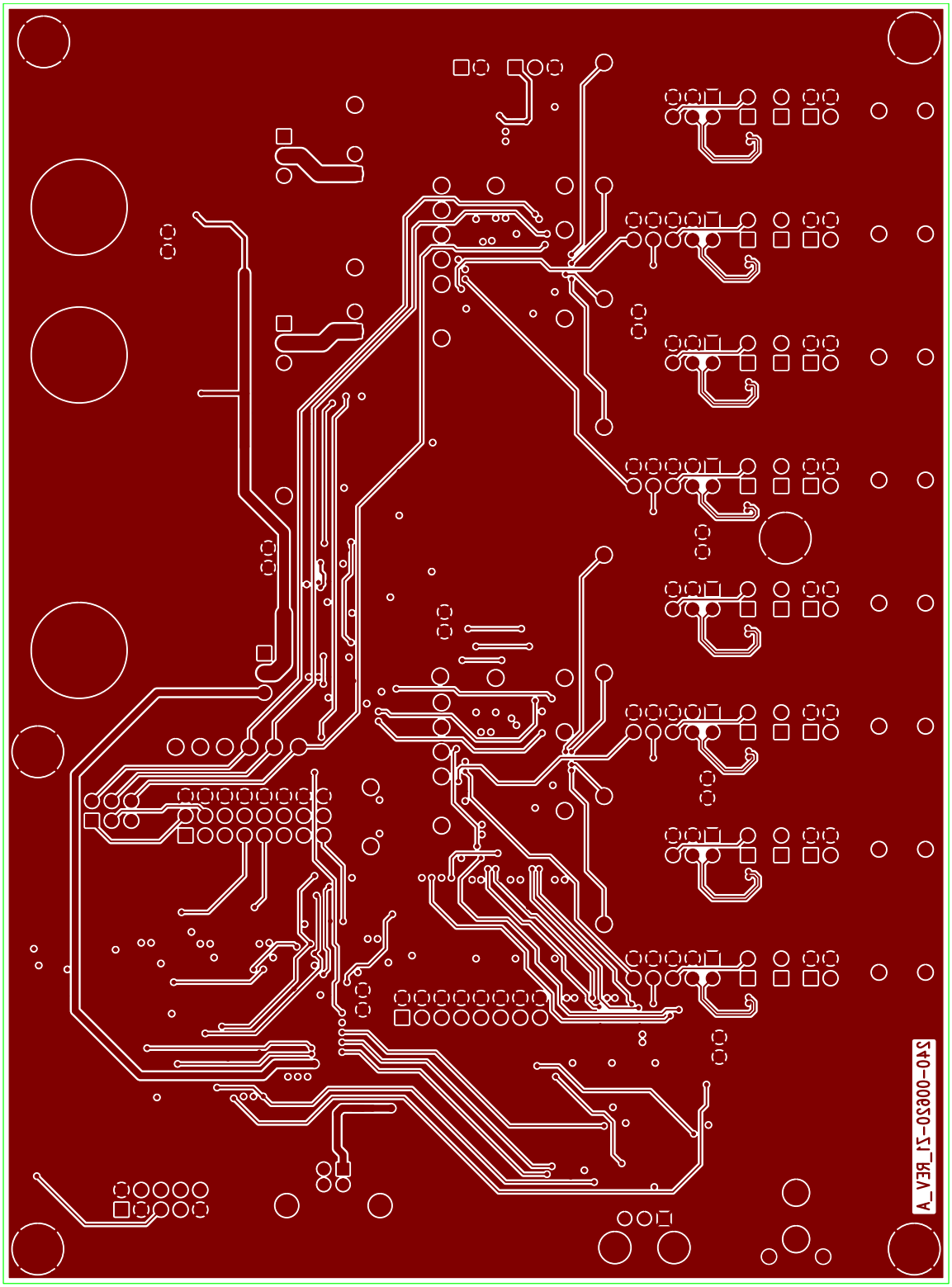


Figure 7-7. Layer 6 (Signal—Bottom)

8 Revision History

Release	Changes
DB1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.