ANALOG DEVICES

Circuit Note
CN-0227

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Devices Connected/Referenced	
AD9467	16-Bit, 250 MSPS Analog-to-Digital Converter
ADL5562	3.3 GHz Ultralow Distortion RF/IF Differential Amplifier

High Performance, 16-Bit, 250 MSPS Wideband Receiver with Antialiasing Filter

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit, shown in Figure 1, is a wideband receiver front end based on the ADL5562 ultralow noise differential amplifier driver and the AD9467 16-bit, 250 MSPS analog-to-digital converter.

The third-order Butterworth antialiasing filter is optimized based on the performance and interface requirements of the amplifier and ADC. The total insertion loss due to the filter network and other components is only 1.8 dB.

The overall circuit has a bandwidth of 152 MHz with a pass band flatness of 1 dB. The SNR and SFDR measured with a 120 MHz analog input are 72.6 dBFS and 82.2 dBc, respectively.

CIRCUIT DESCRIPTION

The circuit accepts a single-ended input and converts it to differential using a wide bandwidth (3 GHz) M/A-COM ECT1-1-13M 1:1 transformer. The ADL5562 3.3 GHz differential amplifier has a differential input impedance of 400 Ω when operating at a gain of 6 dB and 200 Ω when operating at a gain of 12 dB. A gain option of 15.5 dB is also available.

The ADL5562 is an ideal driver for the AD9467, and the fully differential architecture through the low-pass filter and into the ADC provides good high frequency common-mode rejection, as well as minimizes second-order distortion products. The ADL5562 provides a gain of 6 dB or 12 dB depending on the input connection. In the circuit, a gain of 6 dB was used to compensate for the insertion loss of the filter network and transformer (approximately 1.8 dB), providing an overall signal gain of 3.9 dB.

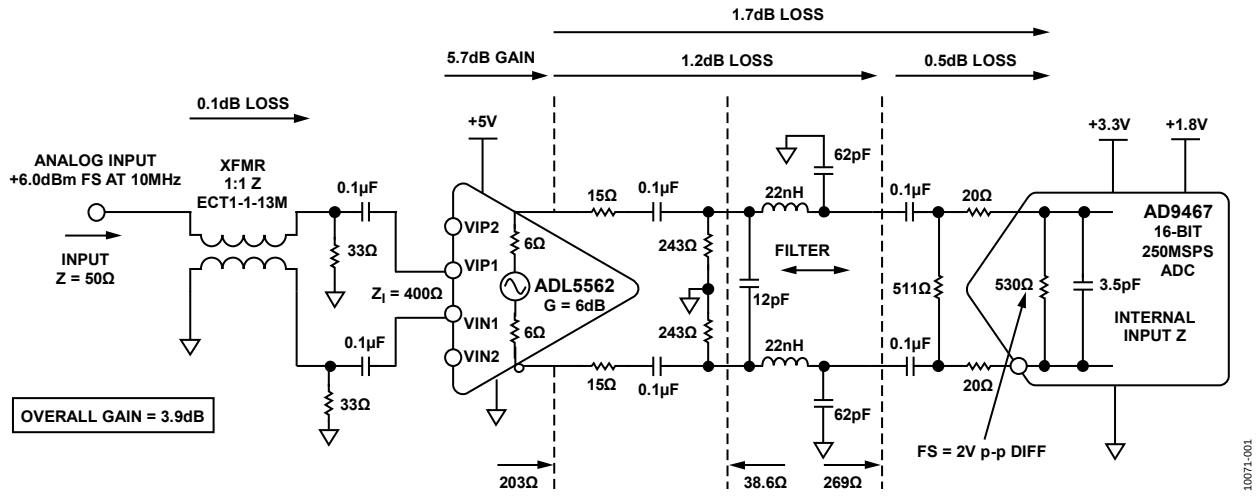

Figure 1. 16-Bit, 250 MSPS Wideband Receiver Front End (Simplified Schematic: All Connections and Decoupling Not Shown)
Gains, Losses, and Signal Levels Measured Values at 10 MHz

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

An input signal of 6.0 dBm produces a full-scale 2 V p-p differential signal at the ADC input.

The antialiasing filter is a third-order Butterworth filter designed with a standard filter design program. A Butterworth filter was chosen because of its flat response within the pass band. A third order filter yields an ac noise bandwidth ratio of 1.05 and can be designed with the aid of several free filter programs such as Nuhertz Technologies Filter Free, or the Quite Universal Circuit Simulator (Qucs) Free Simulation.

To achieve best performance, load the ADL5562 with a net differential load of 200 Ω. The 15 Ω series resistors isolate the filter capacitance from the amplifier output, and the 243 Ω resistors in parallel with the downstream impedance yield a net load impedance of 203 Ω when added to the 30 Ω series resistance.

The 20 Ω resistors in series with the ADC inputs isolate internal switching transients from the filter and the amplifier. The 511 Ω resistor in parallel with the ADC serves to reduce the input impedance of the ADC for more predictable performance.

The third-order Butterworth filter was designed with a source impedance of 38.6 Ω, a load impedance of 269 Ω, and a 3 dB bandwidth of 180 MHz. The calculated values from the program are shown in Figure 1. The values chosen for the filter passive components were the closest standard values to those generated by the program.

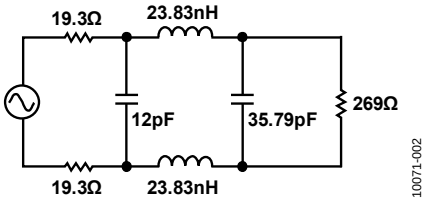

Figure 2. Design for Third-Order Differential Butterworth Filter with Z_S = 38.6 Ω, Z_L = 269 Ω, F_C = 180 MHz

The internal 3.5 pF capacitance of the ADC was subtracted from the value of the second shunt capacitor to yield a value of 32.29 pF. In the circuit, this capacitor was realized using two 62 pF capacitors connected to ground as shown in Figure 1. This provides the same filtering effect and offers some ac common-mode rejection.

The measured performance of the system is summarized in Table 1, where the 3 dB bandwidth is 152 MHz. The total insertion loss of the network is approximately 2 dB. The bandwidth response is shown in Figure 3; the SNR and SFDR performance are shown in Figure 4.

Table 1. Measured Performance of the Circuit

Performance Specs at 2 V p-p FS	Final Results
Cutoff Frequency (−3 dB)	152 MHz
Pass-Band Flatness (6 MHz to 125 MHz)	1 dB
SNRFS at 120 MHz	72.6 dBFS
SFDR at 120 MHz	82.2 dBc
H2/H3 at 120 MHz	86.6 dBc/82.2 dBc
Overall Gain at 10 MHz	3.9 dB
Input Drive at 10 MHz	6.0 dBm

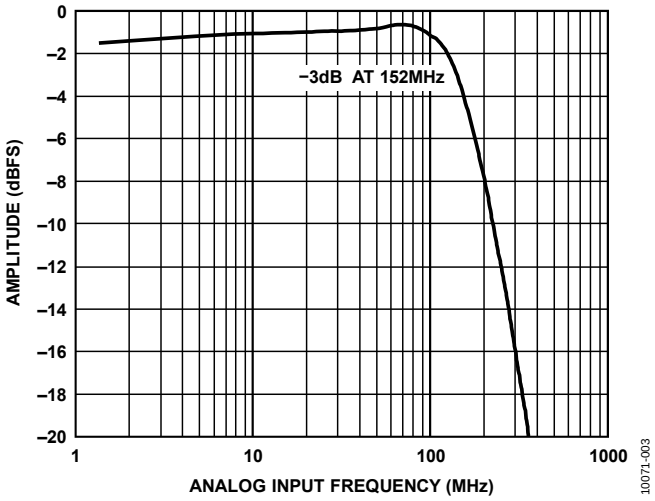

Figure 3. Pass Band Flatness Performance vs. Frequency

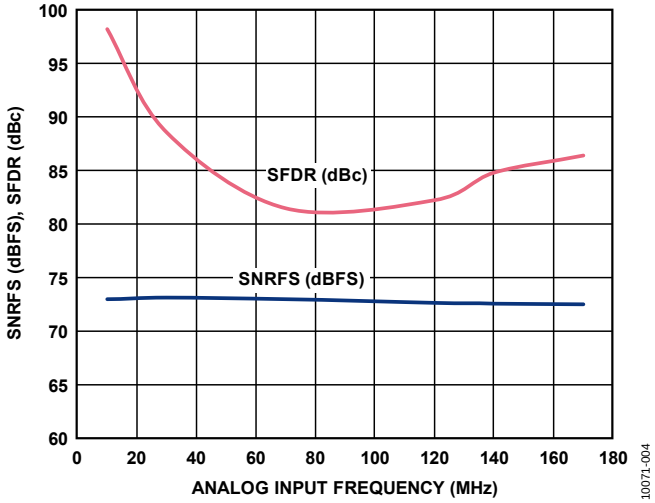

Figure 4. SNR/SFDR Performance vs. Frequency

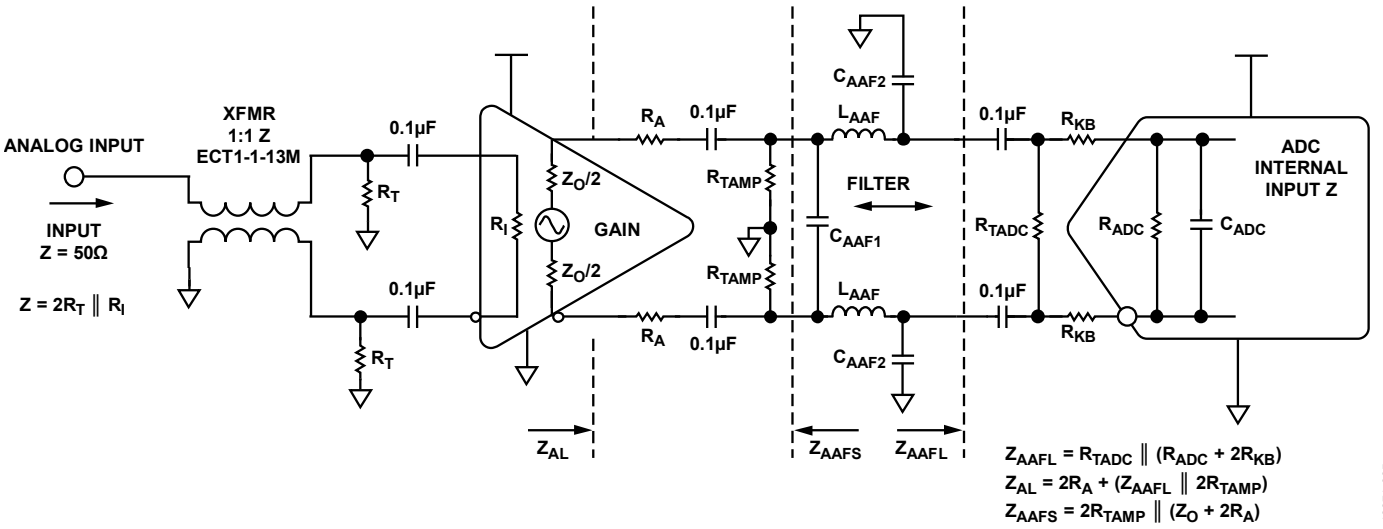

Figure 5. Generalized Differential Amplifier/ADC Interface with Low-Pass Filter

Filter and Interface Design Procedure

In this section, a general approach to the design of the amplifier/ADC interface with filter is presented. To achieve optimum performance (bandwidth, SNR, and SFDR), there are certain design constraints placed on the general circuit by the amplifier and the ADC:

1. The amplifier should see the correct dc load recommended by the data sheet for optimum performance.
2. The correct amount of series resistance must be used between the amplifier and the load presented by the filter. This is to prevent undesired peaking in the pass band.
3. The input to the ADC should be reduced by an external parallel resistor, and the correct series resistance should be used to isolate the ADC from the filter. This series resistor also reduces peaking.

The generalized circuit shown in Figure 5 applies to most high speed differential amplifier/ADC interfaces and will be used as a basis for the discussion. This design approach will tend to minimize the insertion loss of the filter by taking advantage of the relatively high input impedance of most high speed ADCs and the relatively low impedance of the driving source (amplifier).

The basic design process is as follows:

1. Select the external ADC termination resistor R_{TADC} so that the parallel combination of R_{TADC} and R_{ADC} is between 200 Ω and 400 Ω.
2. Select R_{KB} based on experience and/or the ADC data sheet recommendations, typically between 5 Ω and 36 Ω.
3. Calculate the filter load impedance using:

   $$Z_{AAFL} = R_{TADC} \,||\, (R_{ADC} + 2R_{KB})$$

4. Select the amplifier external series resistor R_A. Make R_A less than 10 Ω if the amplifier differential output impedance is 100 Ω to 200 Ω. Make R_A between 5 Ω and 36 Ω if the output impedance of the amplifier is 12 Ω or less.
5. Select R_{TAMP} so that the total load seen by the amplifier, Z_{AL}, is optimum for the particular differential amplifier chosen using the equation:

   $$Z_{AL} = 2R_A + (Z_{AAFL} \,||\, 2R_{TAMP}).$$

6. Calculate the filter source resistance:

   $$Z_{AAFS} = 2R_{TAMP} \,||\, (Z_O + 2R_A).$$

7. Using a filter design program or tables design the filter using the source and load impedances, Z_{AAFS} and Z_{AAFL}, type of filter, bandwidth, and order. Use a bandwidth that is about 40% higher than one-half the sampling rate to ensure flatness in the frequency span between dc and fs/2.
8. The internal ADC capacitance, C_{ADC}, should be subtracted from the final shunt capacitor value generated by the program. The program will give the value C_{SHUNT2} for the differential shunt capacitor. The final common-mode shunt capacitance is

   $$C_{AAF2} = 2(C_{SHUNT2} - C_{ADC}).$$

After running these preliminary calculations, the circuit should be given a quick review for the following items.

1. The value of C_{AAF2} should be at least 10 pF so that it is several times larger than C_{ADC}. This minimizes the sensitivity of the filter to variations in C_{ADC}.
2. The ratio of Z_{AAFL} to Z_{AAFS} should not be more than about 7 so that the filter is within the limits of most filter tables and design programs.
3. The value of C_{AAF1} should be at least 5 pF to minimize sensitivity to parasitic capacitance and component variations.
4. The inductor, L_{AAF}, should be a reasonable value of at least several nH.

In some cases, the filter design program may provide more than one unique solution, especially with higher order filters. The solution that uses the most reasonable set of component values should always be chosen. Also, choose a configuration that ends in a shunt capacitor so that it can be combined with the ADC input capacitance.

Circuit Optimization Techniques and Trade-Offs

The parameters in this interface circuit are very interactive, therefore, it is almost impossible to optimize the circuit for all key specifications (bandwidth, bandwidth flatness, SNR, SFDR, and gain). However, the peaking, which often occurs in the bandwidth response, can be minimized by varying R_A and R_{KB}.

Notice in Figure 6 how the pass-band peaking is reduced as the value of the output series resistance, R_A, is increased. However, as the value of this resistance increases, there is more signal attenuation, and the amplifier must drive a larger signal to fill the ADCs full-scale input range.

The value of R_A also affects SNR performance. Larger values, while reducing the bandwidth peaking, tend to slightly increase the SNR because of the higher signal level required to drive the ADC full scale.

Select the R_{KB} series resistor on the ADC inputs to minimize distortion caused by any residual charge injection from the internal sampling capacitor within the ADC. Increasing this resistor also tends to reduce bandwidth peaking.

However, increasing R_{KB} increases signal attenuation, and the amplifier must drive a larger signal to fill the ADC input range.

Another method for optimizing the pass-band flatness is to vary the filter shunt capacitor, C_{AAF2}, by a small amount.

Normally, the ADC input termination resistor, R_{TADC}, is selected to make the net ADC input impedance between 200 Ω and 400 Ω. Making it lower reduces the effect of the ADC input capacitance and may stabilize the filter design; however, increases the insertion loss of the circuit. Increasing the value also reduces peaking.

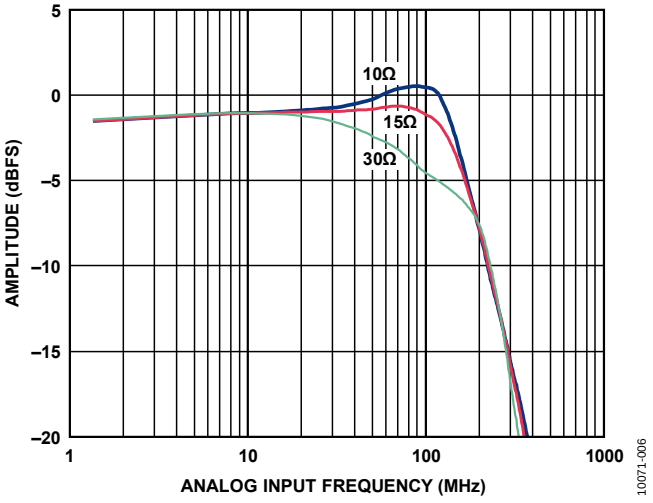

Figure 6. Pass-Band Flatness Performance vs. Amplifier Output Series Resistance, R_A

Balancing these trade-offs can be somewhat difficult. In this design, each parameter was given equal weight; therefore, the values chosen are representative of the interface performance for all the design characteristics. In some designs, different values may be chosen to optimize SFDR, SNR, or input drive level, depending on system requirements.

The SFDR performance in this design is determined by two factors: the amplifier and ADC interface component values as shown in Figure 1, and the setting of the internal front-end buffer bias current in the AD9467 via an internal register. The final SFDR performance numbers shown in Table 1 and Figure 4 were obtained after following the SFDR optimization described in the AD9467 data sheet.

Another trade-off that can be made in this particular design is the ADC full-scale setting. The full-scale ADC differential input voltage was set for 2 V p-p for the data obtained with this design, which optimizes SFDR. Changing the full-scale input range to 2.5 V p-p yields about 1.5 dB improvement in SNR but slightly degrades the SFDR performance. The input range is set by the value loaded into an internal register in the AD9467 as described in the data sheet.

Note that the signal in this design is ac coupled with the 0.1 µF capacitors to block the common-mode voltages between the amplifier, its termination resistors, and the ADC inputs. Refer to the AD9467 data sheet for further details regarding common-mode voltages.

Passive Component and PC Board Parasitic Considerations

The performance of this or any high speed circuit is highly dependent on proper PCB layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, and power and ground planes. See Tutorials MT-031 and MT-101 for more detailed information regarding PCB layout for high speed ADCs and amplifiers.

Use low parasitic surface-mount capacitors, inductors, and resistors for the passive components in the filter. The inductors chosen are from the Coilcraft 0603CS series. The surface mount capacitors used in the filter are 5%, C0G, 0402-type for stability and accuracy.

See the CN-0227 Design Support Package for complete documentation on the system.

COMMON VARIATIONS

For applications that require less bandwidth and lower power, the ADL5561 differential amplifier can be used. The ADL5561 has a bandwidth of 2.9 GHz and only uses 40 mA of current. For even lower power and bandwidth, the ADA4950-1 can also be used. This device has a 1 GHz bandwidth and only uses 10 mA of current. For higher bandwidth, the 6 GHz ADL5565 differential amplifier is pin compatible with the others previously listed.

CIRCUIT EVALUATION AND TEST

This circuit uses a modified AD9467-250EBZ circuit board and the HSC-ADC-EVALCZ FPGA-based data capture board. The two boards have mating high speed connectors, allowing for the quick setup and evaluation of the circuit's performance. The modified AD9467-250EBZ board contains the circuit evaluated as described in this note, and the HSC-ADC-EVALCZ data capture board is used in conjunction with Visual Analog evaluation software, as well as the SPI Controller software to properly control the ADC and capture the data. See User Guide UG-200 for the schematics, BOM, and layout for the AD9467-250EBZ board. The **readme.txt** file in the CN-0227 Design Support Package describes the modifications made to the standard AD9467-250EBZ board. Application Note AN-835 contains complete details on how to set up the hardware and software to run the tests described in this circuit note.

LEARN MORE

CN-0227 Design Support Package: http://www.analog.com/CN0227-DesignSupport

UG-200: *Evaluating the AD9467 16-Bit, 200 MSPS/250 MSPS ADC*

Arrants, Alex, Brad Brannon and Rob Reeder, AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, Analog Devices.

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, *Analog Dialogue* 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Quite Universal Circuit Simulator

Nuhertz Technologies, Filter Free Filter Design Program

Reeder, Rob, *Achieve CM Convergence between Amps and ADCs*, Electronic Design, July 2010.

Reeder, Rob, *Mine These High-Speed ADC Layout Nuggets For Design Gold*, Electronic Design, September 15, 2011.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 1: Power and Ground Planes*, November 2010.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 2: Using Power and Ground Planes to Your Advantage*, February 2011.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 3: The E-Pad Low Down*, June 2011.

Data Sheets and Evaluation Boards

AD9467 Data Sheet

ADL5562 Data Sheet

Circuit Evaluation Board (AD9467-250EBZ)

Standard Data Capture Platform (HSC-ADC-EVALCZ)

REVISION HISTORY

2/12—Rev. 0 to Rev. A

Changes to Figure 1 1

11/11—Revision 0: Initial Version