August 22, 2012

CP2104 Errata

Hardware Errata Status Summary

Errata #	Title	Impact	Status	
			Affected Revisions	Fixed Revision
H1	USB D+/D- Driver Impedance	Minor	Revision E	Revision F
H2	UART, GPIO, Suspend Signals Driven Low After Power Cycling	Major	Revision A–E	Revision F

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

H1. USB D+/D- Driver Impedance

Description: The output impedance of the drivers on the USB D+ and D- data lines is nominally 28 Ω but, in some cases, may be as low as 26 Ω. The minimum USB specification for full-speed devices on the D+ and D- data lines is 28 Ω.

Impact: This may impact systems that need to be submitted for USB compliance testing. The specification for USB compliance is a system-level parameter, not a chip-level parameter. In most systems, the lower impedance of the device will not be a factor. A typical PCB will add 2-3 Ω to the effective driver impedance and bring the system level impedance within specifications.

Workaround: For systems that require USB certification, it is recommended to add some series impedance (between 5 and 8 Ohms, ¼ watt or higher) to D+ and D- in the PCB design.

H2. UART, GPIO, Suspend Signals Driven Low after Power Cycling

Description: The UART, GPIO, and suspend signals will be driven low for approximately 40 microseconds after power cycling the device and then return to the configured reset state.

Impact: This may impact systems in which the CP2104 is connected to devices that are powered from a separate supply and turned on before the CP2104 receives power through the 5 V regulator or through VDD and VIO pins. The drop of the CP2104 signals may be seen as invalid data by the connected devices.

Workaround: In systems that are affected by this drop, the CP2104 should be powered through the 5 V regulator or through the VDD and VIO pins from the same supply used by devices that are connected to the UART, GPIO, and suspend signals of the CP2104.

Data Sheet Errata Status Summary

The Documentation Errata is applicable to the following document:

- CP2104 Data Sheet Revision 1.0

Errata #	Title	Impact	Data Sheet
D1	ROM Programming Voltage	Minor	Issue Exists

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

D1. ROM Programming Voltage

Description: The data sheet incorrectly indicates that VDD must remain at 3.3 V or higher to successfully write to the configuration ROM. Instead, the voltage on the VIO pin must remain at 3.3 V or higher when writing to the configuration ROM.

Impact: For systems that connect VDD and VIO together, there is no impact. For systems that have a separate voltage source for VIO and are configuring the ROM in-system, VIO must remain at 3.3 V while programming is in progress.

Resolution: This note will be fixed in the Revision 1.1 of the CP2104 Data Sheet.