CP2120

SPI-I²C Bridge and GPIO Port Expander

Single Chip SPI to I²C Bridge
- Integrated clock, no external clock required
- On-chip voltage monitor

Slave Serial Peripheral Interface (SPI)
- Up to 1.0 Mbit/s transfers
- Configurable to Least Significant Bit (LSB) or Most Significant Bit (MSB) first transfers

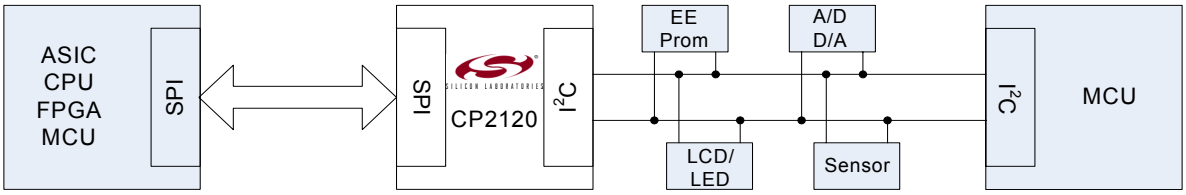
I²C Master Interface
- Operates at configurable rates up to 400 kHz
- 255 byte RX and TX data buffers

General Purpose Input and Output Port Pin Expansion
- 8 pins configurable as push-pull or open-drain
- 1 pin configurable as an edge-triggered interrupt source
- All pins 5 V tolerant

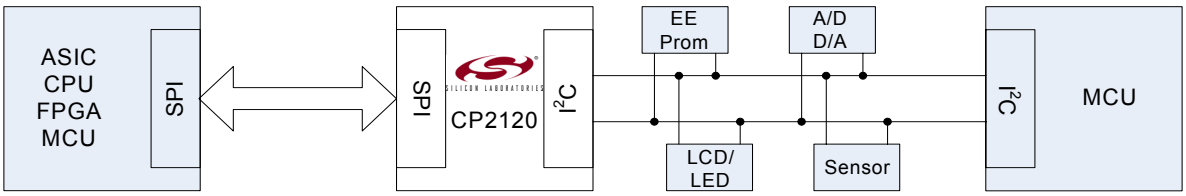
Supply Voltage: 2.7 to 3.6 V
- Typical operating current of 6.4 mA

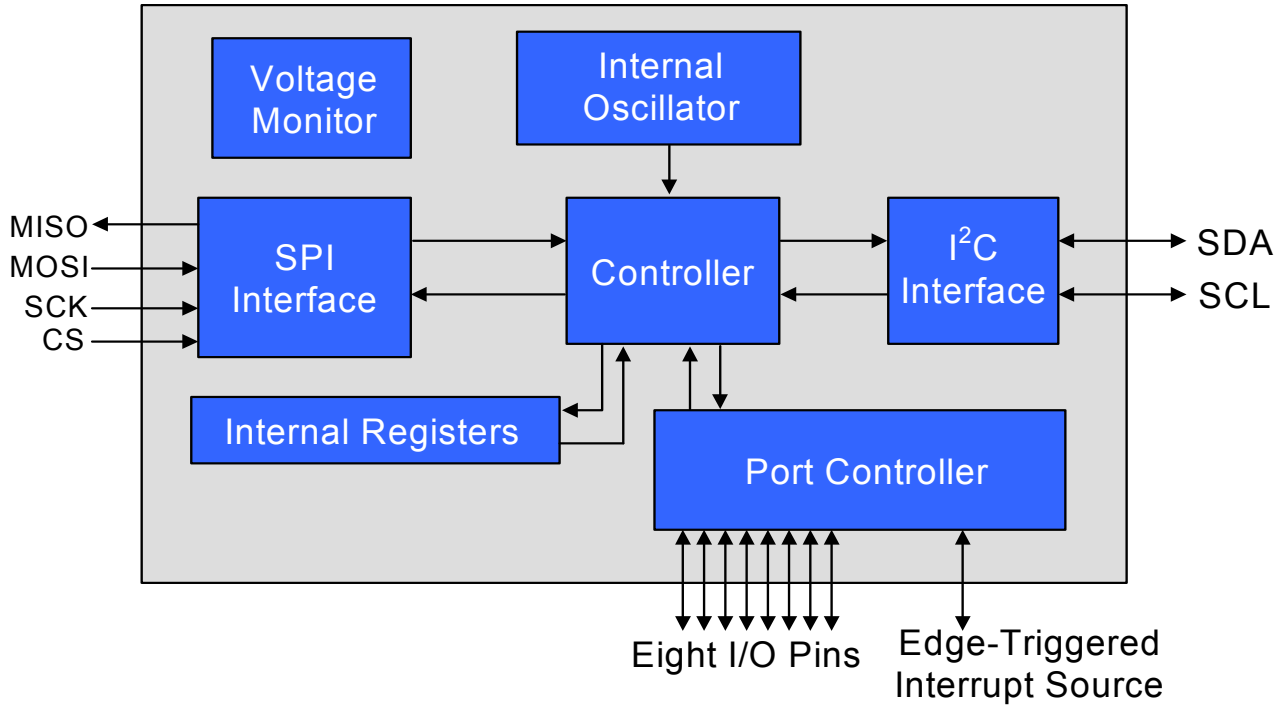
Small Package
- 20-pin 4x4 mm Pb-free QFN

SPI-I²C Bridge Functionality



GPIO Port Expansion Functionality





Selected Electrical Specifications

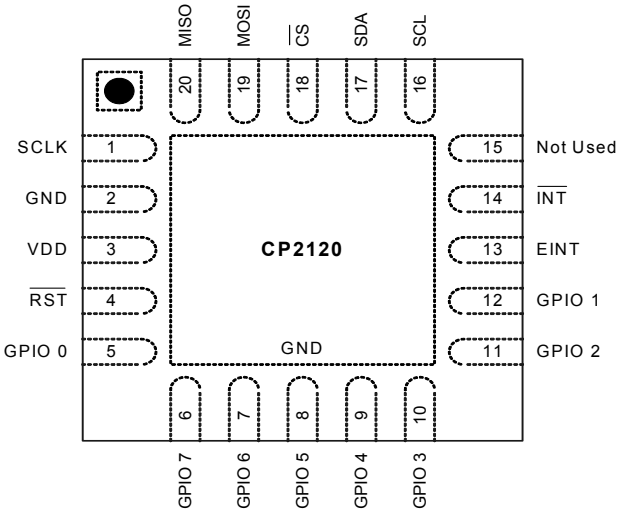
(T_A = –40 to +85 C° unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
Global Characteristics					
Supply Voltage		2.7	—	3.6	V
Supply Current		—	6.4	—	mA
Bus Characteristics					
SPI Bus Speed		7	—	1000	kHz
I²C Bus Speed		7	—	400	kHz

CP2120 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	SCLK	Digital Input	SPI bus clock signal
2	GND		Ground
3	VDD		Power supply voltage
4	$\overline{RST}$	Digital Input/Output	Reset
5–12	GPIO	Digital Input/Output	General purpose input/output
13	EINT	Digital Input	Edge-triggered interrupt source
14	INT	Digital Output	CP2120 interrupt indicator
15	n/c		No connection
16	SCL	Digital Input/Output	I²C bus bidirectional clock signal
17	SDA	Digital Input/Output	I²C bus bidirectional data signal
18	CS	Digital Input	SPI bus chip select
MOSI	19	Digital Input	SPI bus Master Out Slave In signal
MISO	20	Digital Output	SPI bus Master In Slave Out signal

Package Information



CP2120 Evaluation Board