DDR SDRAM UNBUFFERED DIMM

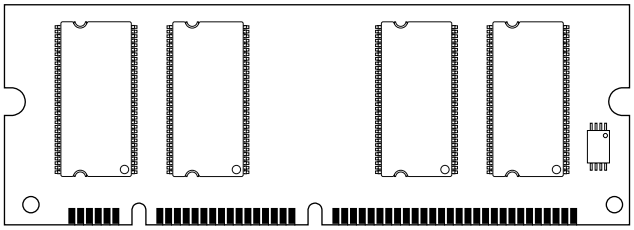
MT4VDDT1632U – 64MB
MT4VDDT3232U – 128MB

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/products/modules

Features

- 100-pin, dual in-line memory module (DIMM)
- Fast data transfer rate: PC2100 and PC2700
- Utilizes 266 MT/s or 333 MT/s DDR SDRAM components
- 64MB (16 Meg x 32) and 128MB (32 Meg x 32)
- V_{DD} = $V_{DD}Q$ = +2.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ received with data—*i.e.*, source-synchronous data capture
- Differential clock inputs CK and CK#
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Auto Refresh and Self Refresh Modes 15.625µs (64MB), 7.8125µs (128MB) maximum average periodic refresh interval
- Gold edge contacts

Figure 1: 100-Pin DIMM (MO-161)



OPTIONS	MARKING
• Package	
100-pin DIMM (standard)	G
100-pin DIMM (lead-free)	Y[1]
• Operating Temperature Range	
Commercial (ambient)	none
Industrial (ambient)	I
• Frequency/CAS Latency[2]	
6ns/167 MHz (333MT/s) CL = 2.5	-6
7.5ns/133 MHz (266 MT/s) CL = 2	-75Z[1]
7.5ns/133 MHz (266 MT/s) CL = 2.5	-75

NOTE: 1. Contact Micron for product availability.
2. CL = CAS (READ) latency.

Table 1: Address Table

	MT4VDDT1632U	MT4VDDT3232U
Refresh Count	4K	8K
Row Addressing	4K (A0–A11)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)
Column Addressing	1K (A0–A9)	1K (A0–A9)
Module Rank Addressing	1 (S0#)	1 (S0#)

Table 2: Part Numbers and Timing Parameters

PART NUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA BIT RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT4VDDT1632UG-6__	64MB	16 Meg x 32	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT1632UY-6__	64MB	16 Meg x 32	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT1632UG-75__	64MB	16 Meg x 32	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT4VDDT1632UY-75__	64MB	16 Meg x 32	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT4VDDT3232UG-6__	128MB	32 Meg x 32	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT3232UY-6__	128MB	32 Meg x 32	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT3232UG-75__	128MB	32 Meg x 32	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT4VDDT3232UY-75__	128MB	32 Meg x 32	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

NOTE:

All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT4VDDT1632UG-75B1

Table 3: Pin Assignment (100-Pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	DQ0	14	VDD	26	A5	39	DQ18
2	VSS	15	DQ11	27	A3	40	DQ19
3	DQ1	16	VSS	28	A1	41	VDD
4	DQS0	17	CK0	29	A10	42	DQ24
5	VDD	18	CK0#	30	VDD	43	DQ25
6	DQ2	19	VDD	31	BA0	44	VSS
7	DQ3	20	NC	32	WE#	45	DQS3
8	VDD	21	NC/A12	33	S0#	46	DQ26
9	DQ8	22	NC	34	DQ16	47	VSS
10	DQ9	23	A9	35	VSS	48	DQ27
11	VSS	24	A7	36	DQ17	49	SA0
12	DQS1	25	VSS	37	DQS2	50	VREF
13	DQ10			38	VDD		

Table 4: Pin Assignment (100-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
51	DQ4	64	VDD	76	A2	89	DQ22
52	VSS	65	DQ15	77	A0	90	DQ23
53	DQ5	66	VSS	78	BA1	91	VDD
54	DM0	67	DNU	79	RAS#	92	DQ28
55	VDD	68	DNU	80	VDD	93	DQ29
56	DQ6	69	VDD	81	CAS#	94	VSS
57	DQ7	70	CKE0	82	NC	95	DM3
58	VDD	71	A11	83	DNU	96	DQ30
59	DQ12	72	A8	84	DQ20	97	VSS
60	DQ13	73	A6	85	VSS	98	DQ31
61	VSS	74	A4	86	DQ21	99	SDA
62	DM1	75	VSS	87	DM2	100	SCL
63	DQ14			88	VDD		

NOTE:

Pin 21 is No Connect for the 64MB module, or A12 for the 128MB module.

Figure 2: Module Layout

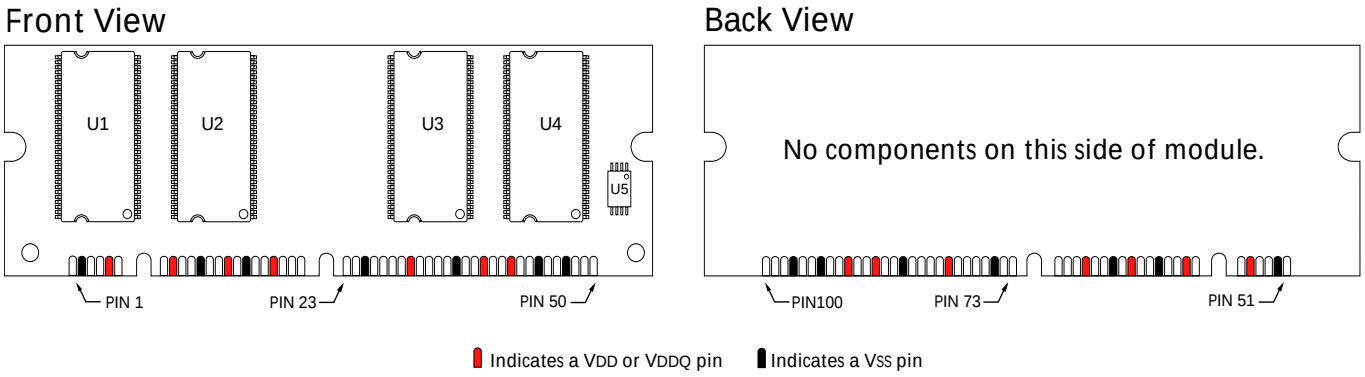


Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment Tables for pin number and symbol information

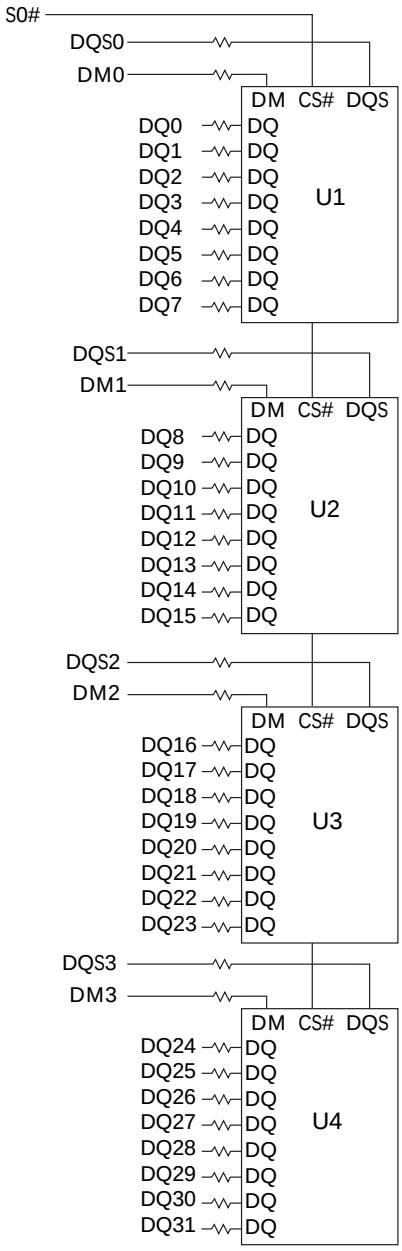
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
32, 79, 81	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
17, 18	CK0, CK0#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK,and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
70	CKE0	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank).CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied.
33	S0#	Input	Chip Selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
31, 78	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
21 (128MB), 23, 24, 26-29, 71-74, 76, 77	A0–A11 (64MB) A0–A12 (128MB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
4, 12, 37, 45	DQS0–DQS3	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
54, 62, 87, 95	DM0–DM3	Input	Data Write Mask. DM LOW allows WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.
1, 3, 6, 7, 9,10, 13, 15, 34, 36, 39, 40, 42, 43, 46, 48, 51, 53, 56, 57, 59, 60, 63, 65, 84, 86, 89, 90, 92, 93, 96, 98	DQ0–DQ31	Input/ Output	Data I/Os: Data bus.
49	SA0	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
99	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.

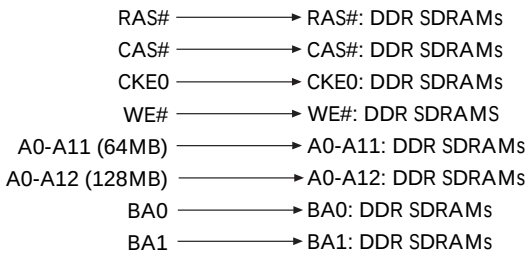
Table 5: Pin Descriptions (Continued)

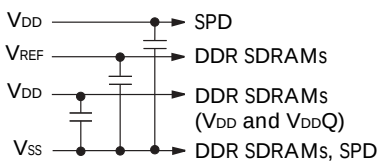
Pin numbers may not correlate with symbols; refer to Pin Assignment Tables for pin number and symbol information

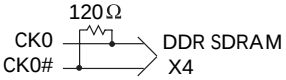
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
100	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
50	V_{REF}	Supply	SSTL_2 reference voltage.
5, 8, 14, 19, 30, 38, 41, 55, 58, 64, 69, 80, 88, 91	V_{DD}	Supply	Power Supply: +2.5V ±0.2V. Please see note 49, on page 20.
2, 11, 16, 25, 35, 44, 47, 52, 61, 66, 75, 85, 94, 97	V_{SS}	Supply	Ground.
67, 68, 83	DNU	—	Do Not Use: This pin is not connected on these modules, but is an assigned pin on other modules in this product family.
20, 21 (64MB only), 22, 82	NC	—	No Connect: These pins should be left unconnected.

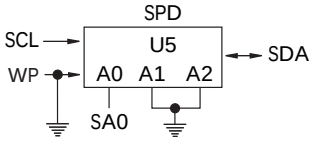
Figure 3: Functional Block Diagram











NOTE: All resistor values are 22Ω unless otherwise specified.
Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part number guide at www.micron.com/numberguide.

Standard modules use the following DDR SDRAM devices:
MT46V16M8TG (64MB); MT46V32M8TG (128MB)

Lead-free modules use the following DDR SDRAM devices:
MT46V16M8P (64MB); MT46V32M8P (128MB)

General Description

The MT4VDDT1632U and MT4VDDT3232U are high-speed CMOS, dynamic random-access, 64MB and 128MB memory modules organized in x32 configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select device bank; A0–A11(64MB) or A0–A12 (128MB) select device row). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM device operation, refer to the 128Mb or 256Mb DDR SDRAM component data sheets.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Mode Register Definition

The mode register is used to define the specific mode of operation of DDR SDRAM devices. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 4, Mode Register Definition Diagram, on page 8. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 (64MB) or A7–A12 (128MB) specify the operating mode.

Burst Length

Read and write accesses to DDR SDRAM devices are burst oriented, with the burst length being programmable, as shown inFigure 4, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A9 when the burst length is set to two, by A2–A9 when the burst length is set to four and by A3–A9 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6, Burst Definition Table, on page 9.

Read Latency

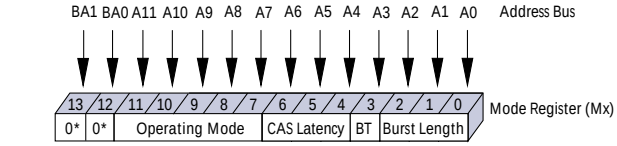
The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in Figure 5, CAS Latency Diagram, on page 9.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 7, CAS Latency (CL) Table, on page 9, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

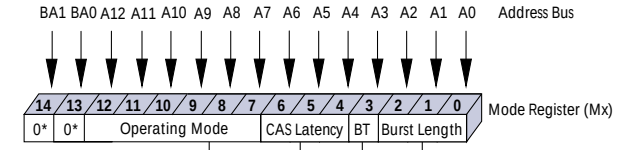
Figure 4: Mode Register Definition Diagram

64MB Module Address Bus



* M13 and M12 (BA1and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

128MB Module Address Bus



* M14 and M13 (BA1 and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Table 6: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS			ORDER OF ACCESSES WITHIN A BURST	
				TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

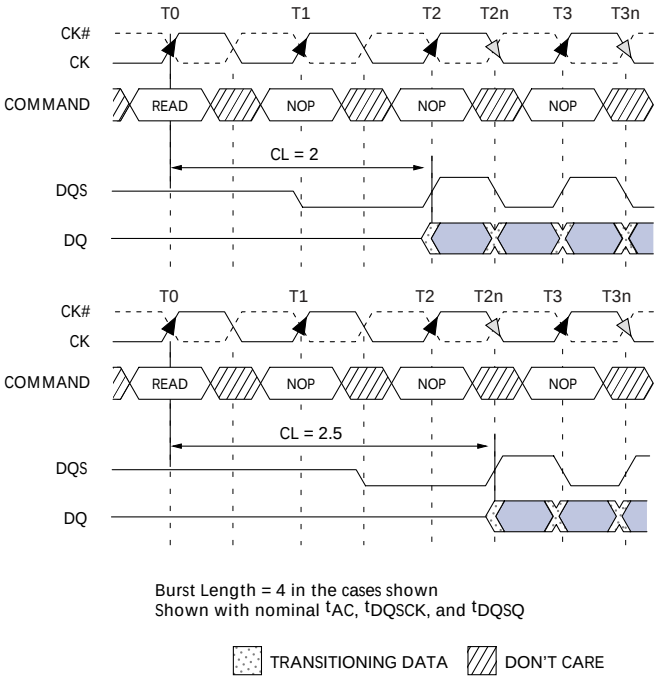
NOTE:

1. For a burst length of two, A1–A9 select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2–A9 select the four-data-element block; A0–A1 select the first access within the block.
3. For a burst length of eight, A3–A9 select the eight-data-element block; A0–A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Table 7: CAS Latency (CL) Table

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ)	
	CL = 2	CL = 2.5
-6	N/A	75 ≤ f ≤167
-75Z	75 ≤ f ≤ 100	75 ≤ f ≤133
-75	N/A	75 ≤ f ≤133

Figure 5: CAS Latency Diagram



Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A11 (64MB) or A7–A12 (128MB) each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A11 (64MB), or A7 and A9–A12 (128MB) each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A11 (64MB) or A7–A12 (128MB) are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 6, Extended Mode Register Definition Diagram, on page 10. The extended mode register is programmed via the LOAD MODE REGIS-

TER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

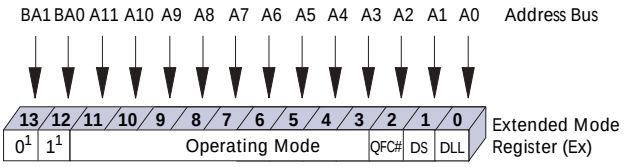
The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

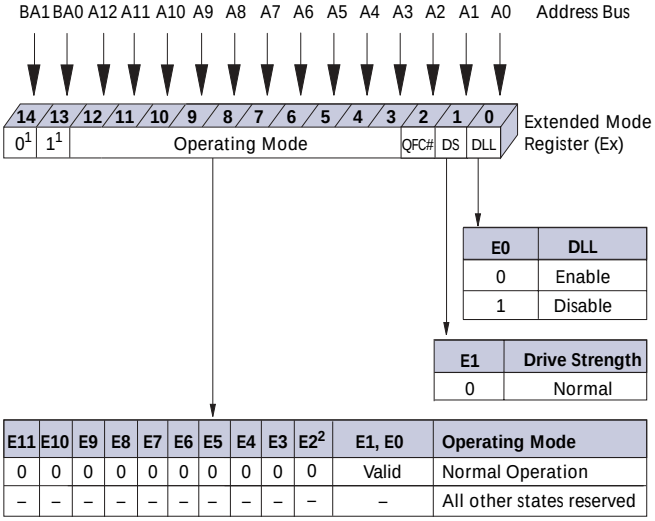
The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time DLL is enabled, 200 clock cycles with CKE HIGH must occur before a READ command can be issued.

Figure 6: Extended Mode Register Definition Diagram

64MB Module



128MB Module



E0	DLL
0	Enable
1	Disable

E1	Drive Strength
0	Normal

E11	E10	E9	E8	E7	E6	E5	E4	E3	E2[2]	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	–	–	–	–	–	All other states reserved

NOTE:

1. BA1 and BA0 (E13 and E12 for 64MB or E14 and E13 for 128MB) must be “0, 1” to select the Extended Mode Register (vs. the base Mode Register).
2. QFC# is not supported.

Commands

Table 8, Commands Truth Table, and Table 9, DM Operation Truth Table, provide a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb or 256Mb DDR SDRAM component data sheet.

Table 8: Commands Truth Table

CKE is HIGH for all commands shown except SELF REFRESH; all states and sequences not shown are illegal or reserved

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	1
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	2
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	3
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	3
BURST TERMINATE	L	H	H	L	X	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	8

NOTE:

1. DESELECT and NOP are functionally interchangeable.
2. BA0–BA1 provide device bank address and A0–A11 (64MB) or A0–A12 (128MB) provide row address.
3. BA0–BA1 provide device bank address; A0–A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
4. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
5. A10 LOW: BA0–BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0–BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A11 (64MB) or A0–A12 (128MB) provide the op-code to be written to the selected mode register.

Table 9: DM Operation Truth Table

Used to mask write data; provided coincident with the corresponding data

NAME (FUNCTION)	DM	DQS
WRITE Enable	L	Valid
WRITE Inhibit	H	X

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on V_{DD} Supply
Relative to V_{SS} . . . . . -1V to +3.6V
Voltage on V_{DDQ} Supply
Relative to V_{SS} . . . . . -1V to +3.6V
Voltage on V_{REF} and Inputs
Relative to V_{SS} . . . . . -1V to +3.6V
Voltage on I/O Pins
Relative to V_{SS} . . . . . -0.5V to V_{DDQ} +0.5V
Operating Temperature,
T_A (ambient - commercial) . . . . . 0°C to +70°C
T_A (ambient - industrial) . . . . . -40°C to +85°C
Storage Temperature (plastic) . . . . . -55°C to +150°C
Short Circuit Output Current 50mA

Table 10: DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 14, 49; notes appear on pages 17–20; 0°C ≤ T_A ≤ +70°C

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{DD}	2.3	2.7	V	32, 42
I/O Supply Voltage		V_{DDQ}	2.3	2.7	V	32, 42, 37
I/O Reference Voltage		V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	6, 37
I/O Termination Voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 37
Input High (Logic 1) Voltage		V_{IH} (DC)	V_{REF} + 0.15	V_{DD} + 0.3	V	25
Input Low (Logic 0) Voltage		V_{IL} (DC)	-0.3	V_{REF} - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ VDD, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Command/ Address, RAS#, CAS#, WE#, CKE, S#, CK, CK#	I_I	-8	8	µA	48
	DM		-2	2		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	DQ, DQS	I_{OZ}	-5	5	µA	48
OUTPUT LEVELS High Current (V_{OUT} = V_{DDQ}-0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	-16.8	–	mA	33, 41
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA	

Table 11: AC Input Operating Conditions

Notes: 1–5, 14, 49, 50; notes appear on pages 17–20; 0°C ≤ T_A ≤ +70°C; V_{DD} = V_{DDQ} = +2.5V ±0.2V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH} (AC)	V_{REF} + 0.310	–	V	12, 25, 40
Input Low (Logic 0) Voltage	V_{IL} (AC)	–	V_{REF} - 0.310	V	12, 25, 40
I/O Reference Voltage	V_{REF} (AC)	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	6

Table 12: IDD Specifications and Conditions – 64MB

DDR SDRAM components only

Notes: 1–5, 14, 49; notes appear on pages 17–20; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

			MAX			
PARAMETER/CONDITION		SYMBOL	-6	-75Z/-75	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	500	420	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	540	480	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = (LOW)		IDD2P	12	12	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; tCK = tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	180	180	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	100	80	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX);tCK = tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	200	180	mA	39
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	560	500	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W[a]	560	480	mA	20
AUTO REFRESH CURRENT	tREFC = tRFC (MIN)	IDD5	1,060	840	mA	20, 45
	tREFC = 15.625µs	IDD5A	20	20	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	12	8	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, tRC = tRC (MIN); tCK = tCK (MIN); Address and control inputs change only during Active READ or WRITE commands		IDD7	1,420	1,300	mA	20, 44

Table 13: IDD Specifications and Conditions – 128MB

DDR SDRAM components only

Notes: 1–5, 14, 49; notes appear on pages 17–20; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

			MAX			
PARAMETER/CONDITION		SYMBOL	-6	-75Z/-75	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	500	480	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); IOUT= 0mA; Address and control inputs changing once per clock cycle		IDD1	680	620	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		IDD2P	16	16	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^tCK = ^tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN= VREF for DQ, DQS, and DM		IDD2F	200	180	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		IDD3P	120	120	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	240	200	mA	39
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); IOUT = 0mA		IDD4R	700	700	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	700	600	mA	20
AUTO REFRESH CURRENT	^tREFC = ^tRFC (MIN)	IDD5	1,020	980	mA	20, 45
	^tREFC = 7.8125µs	IDD5A	24	24	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	16	16	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); Address and control inputs change only during Active READ or WRITE commands		IDD7	1,640	1,460	mA	20, 44

Table 14: Capacitance (All Modules)

Note: 11; notes appear following parameter tables.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4	5	pF
Input Capacitance: Command and Address, S#, CK, CK#, CKE	C_{I1}	8	12	pF

Table 15: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–5, 12–15, 29, 49; notes appear on pages 17–20; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.5V ±0.2V

AC CHARACTERISTICS			-6		-75Z/-75			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQ from CK/CK#		t_{AC}	-0.7	+0.7	-0.75	+0.75	ns	
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	26
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	26
Clock cycle time	CL = 2.5	t_{CK} (2.5)	6	13	7.5	13	ns	38, 47
	CL = 2	t_{CK} (2)	7.5	13	10	13	ns	38, 47
DQ and DM input hold time relative to DQS		t_{DH}	0.45		0.5		ns	23, 27
DQ and DM input setup time relative to DQS		t_{DS}	0.45		0.5		ns	23, 27
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		ns	27
Access window of DQS from CK/CK#		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	ns	
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.45		0.5	ns	22, 23
Write command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}	
Half clock period		t_{HP}	t_{CH},t_{CL}		t_{CH},t_{CL}		ns	30
Data-out high-impedance window from CK/CK#		t_{HZ}		+0.70		+0.75	ns	16, 43
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.7		-0.75		ns	16, 43
Address and control input hold time (fast slew rate)		t_{IH_F}	0.75		0.90		ns	12
Address and control input setup time (fast slew rate)		t_{IS_F}	0.75		0.90		ns	12
Address and control input hold time (slow slew rate)		t_{IH_S}	0.8		1		ns	12
Address and control input setup time (slow slew rate)		t_{IS_S}	0.8		1		ns	12
Address and Control input pulse width (for each input)		t_{IPW}	2.2		2.2		ns	
LOAD MODE REGISTER command cycle time		t_{MRD}	12		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns	22, 23
Data hold skew factor		t_{QHS}		0.60		0.75	ns	
ACTIVE to PRECHARGE command		t_{RAS}	42	70,000	40	120,000	ns	31, 50

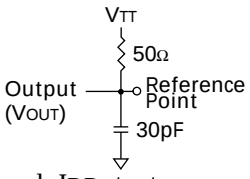
Table 15: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes: 1–5, 12–15, 29, 49; notes appear on pages 17–20; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.5V ±0.2V

AC CHARACTERISTICS			-6		-75Z/-75			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
ACTIVE to READ with Auto precharge command		^tRAP	15		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	60		65		ns	
AUTO REFRESH command period		^tRFC	72		75		ns	45
ACTIVE to READ or WRITE delay		^tRCD	15		20		ns	
PRECHARGE command period		^tRP	15		20		ns	
DQS read preamble		^tRPRE	0.9	1.1	0.9	1.1	^tCK	36
DQS read postamble		^tRPST	0.4	0.6	0.4	0.6	^tCK	36
ACTIVE bank a to ACTIVE bank b command		^tRRD	12		15		ns	
DQS write preamble		^tWPRE	0.25		0.25		^tCK	
DQS write preamble setup time		^tWPRES	0		0		ns	18, 19
DQS write postamble		^tWPST	0.4	0.6	0.4	0.6	^tCK	17
Write recovery time		^tWR	15		15		ns	
Internal WRITE to READ command delay		^tWTR	1		1		^tCK	
Data valid output window		na	^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	22
REFRESH to REFRESH command interval	64MB	^tREFC		140		140.6	µs	21
	128MB			70.3		70.3		
Average periodic refresh interval	64MB	^tREFI		15.6		15.6	µs	21
	128MB			7.8		7.8		
Terminating voltage delay to V_{DD}		^tVTD	0		0		ns	
Exit SELF REFRESH to non-READ command		^tXSNR	75		75		ns	
Exit SELF REFRESH to READ command		^tXSRD	200		200		^tCK	

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



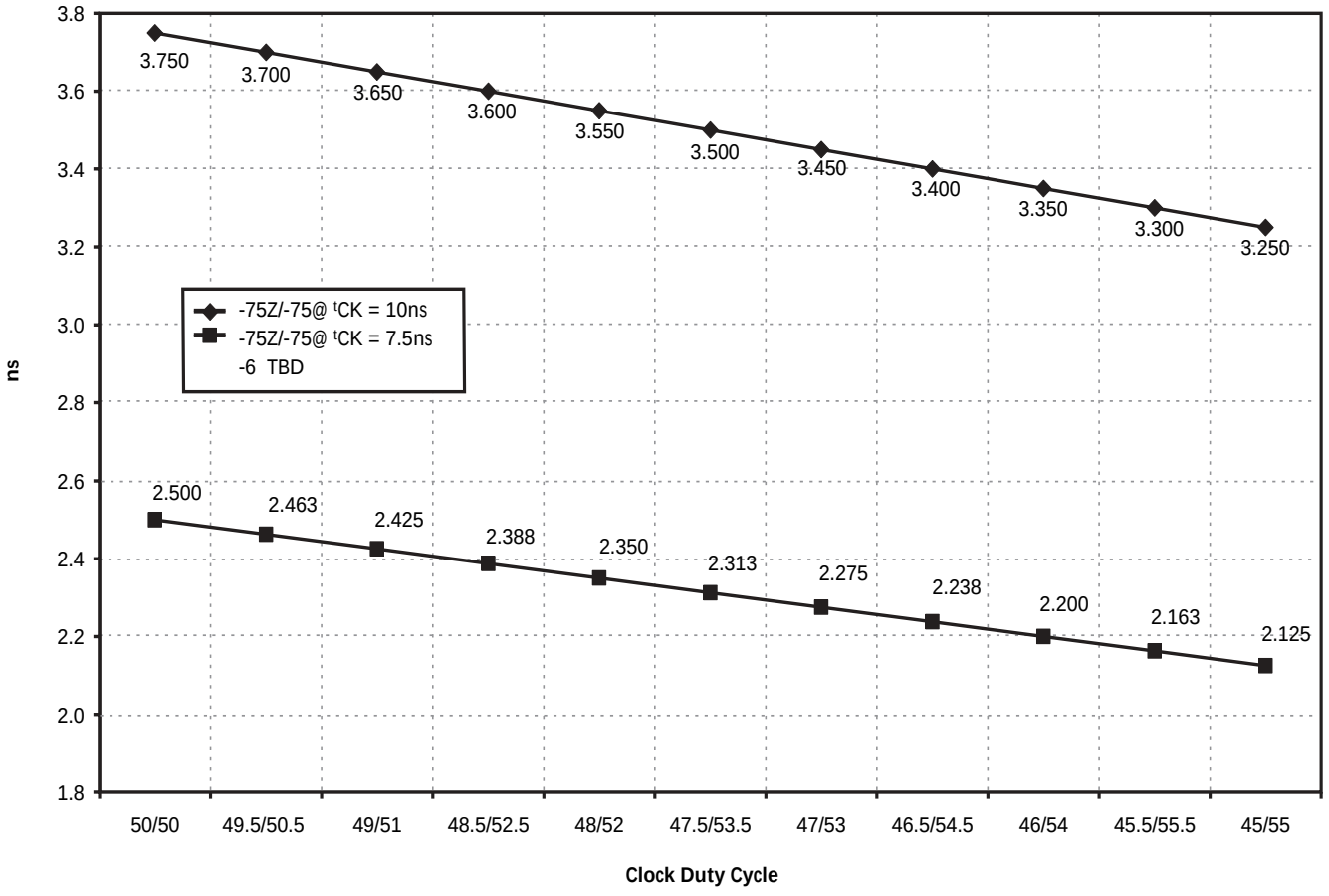
4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL} (AC) and V_{IH} (AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -75Z and CL = 2.5 for -6 and -75 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V, V_{REF} = VSS, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = V_{DDQ}/2, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates less than 1 V/ns and greater than or equal to 0.5 V/ns. If slew rate is less than 0.5 V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from 500mV/ns, while ^{t}IH is unaffected. If slew rate exceeds 4.5V/ns, functionality is uncertain. For -6, slew rates must be ≥ 0.5 V/ns.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x V_{DDQ} is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low, or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions high [above V_{IH} DC (MIN)] then it must not transition low (below V_{IH}DC) prior to ^{t}DQSH (MIN).
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
20. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
21. The refresh period 64ms. This equates to an average refresh rate of 15.625µs (64MB) or 7.8125µs (128MB). However, an AUTO REFRESH command must be asserted at least once every 140.6µs

(64MB) or 70.3µs (128MB); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.

22. The valid data window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain. Figure 7, Derating Data Valid Window (^{t}QH - ^{t}DQSQ), shows data valid window derating curves for duty cycles ranging between 50/50 and 45/55.
23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, VIL (AC) or VIH (AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, VIL (DC) or VIH (DC).
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain. For -6, slew rates must be ≥ 0.5 V/ns.
28. VDD must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.

Figure 7: Derating Data Valid Window

(^{t}QH - ^{t}DQSQ)



30. ^{t}HP min is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch to the nominal voltage must be less than 1/3 of the clock and not more than +400mV or 2.9 volts maximum, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2 volts minimum, whichever is more positive.
33. Normal Output Drive Curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics, on page 20.
    b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics, on page 20.
    c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics, on page 20.
    d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics, on page 20.
    e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.
34. Reduced Output Drive Curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 10, Reduced Output Pull-Down Characteristics, on page 20.
    b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 10, Reduced Output Pull-Down Characteristics, on page 20.
    c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 11, Reduced Output Pull-Up Characteristics, on page 20.
    d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 11, Reduced Output Pull-Up Characteristics, on page 20.
    e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage.
    f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.
35. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition. ^{t}LZ (MIN) will prevail over ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
36. ^{t}RPST end point and ^{t}RPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (^{t}RPST), or begins driving (^{t}RPRE).
37. During initialization, $V_{DD}Q$, V_{TT}, and V_{REF} must be equal to or less than V_{DD} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power up, even if $V_{DD}/V_{DD}Q$ are 0 volts, provided a minimum of 42 ohms of series resistance is used between the V_{TT} supply and the input pin.
38. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
39. For the -6 and -75 $I_{DD}3N$ is specified to be 35mA per DDR SDRAM at 100 MHz.
40. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.

Figure 8: Pull-Down Characteristics

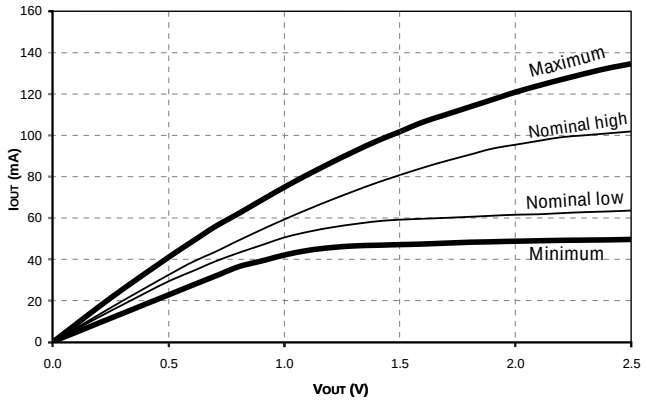


Figure 9: Pull-Up Characteristics

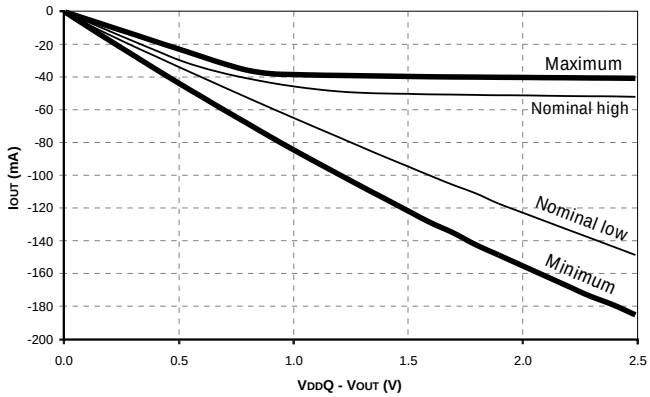


Figure 10: Reduced Output Pull-Down Characteristics

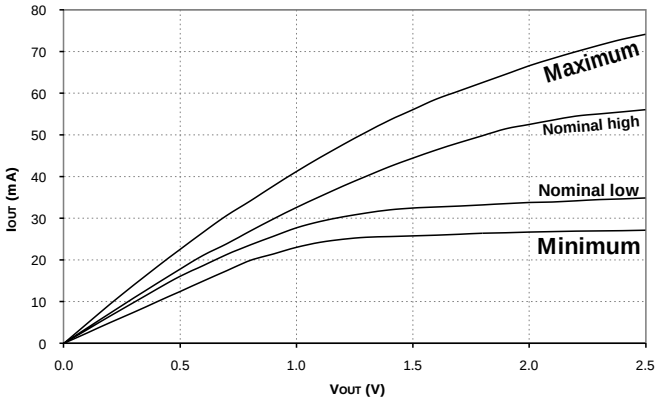
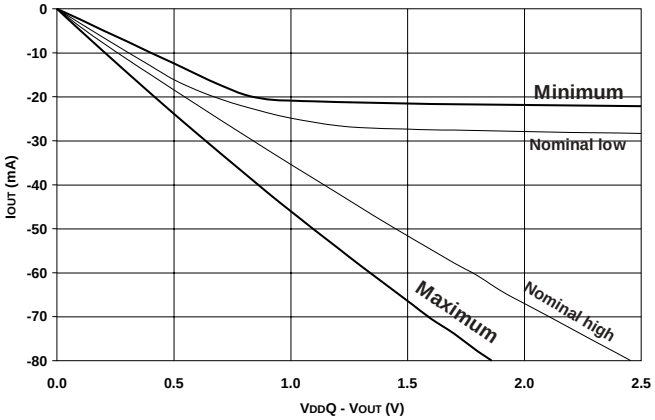


Figure 11: Reduced Output Pull-Up Characteristics



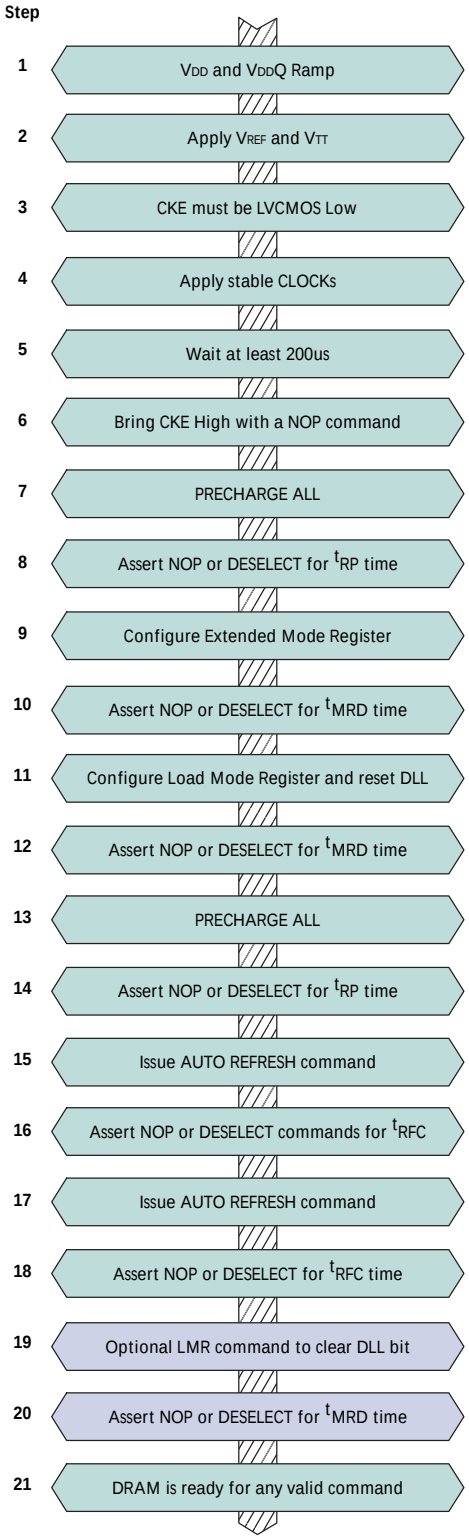
41. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
42. VDD and VDDQ must track each other.
43. Random addressing changing and 50 percent of data changing at every transfer.
44. Random addressing changing and 100 percent of data at every transfer.
45. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
46. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is "worst case."
47. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
48. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
49. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.
50. The -6 speed grade will operate with ^{t}RAS (MIN) = 40ns and ^{t}RAS (MAX) = 120,000ns at any slower frequency.

Initialization

To ensure device operation the DRAM must be initialized as described below:

1. Simultaneously apply power to VDD and VDDQ.
2. Apply VREF and then VTT power.
3. Assert and hold CKE at a LVCMOS logic low.
4. Provide stable CLOCK signals.
5. Wait at least 200µs.
6. Bring CKE high and provide at least one NOP or DESELECT command. At this point the CKE input changes from a LVCMOS input to a SSTL2 input only and will remain a SSTL_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least ^{t}RP time, during this time NOPs or DESELECT commands must be given.
9. Using the LMR command program the Extended Mode Register (E0 = 0 to enable the DLL and E1 = 0 for normal drive or E1 = 1 for reduced drive, E2 through En must be set to 0; where n = most significant bit).
10. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
11. Using the LMR command program the Mode Register to set operating parameters and to reset the DLL. Note at least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least ^{t}RP time, only NOPs or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
16. Wait at least ^{t}RFC time, only NOPs or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
18. Wait at least ^{t}RFC time, only NOPs or DESELECT commands are allowed.
19. Although not required by the Micron device, JEDEC requires a LMR command to clear the DLL bit (set M8 = 0). If a LMR command is issued the same operating parameters should be utilized as in step 11.
20. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
21. At this point the DRAM is ready for any valid command. Note 200 clock cycles are required between step 11 (DLL Reset) and any READ command.

Figure 12: Initialization Flow Diagram



SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 13, Data Validity, and Figure 14, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 14, Definition of Start and Stop).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 13: Data Validity

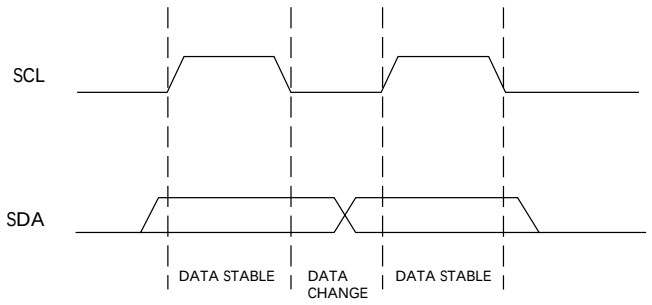


Figure 14: Definition of Start and Stop

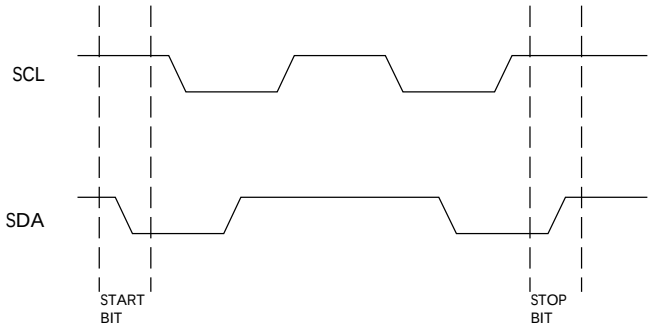


Figure 15: Acknowledge Response from Receiver

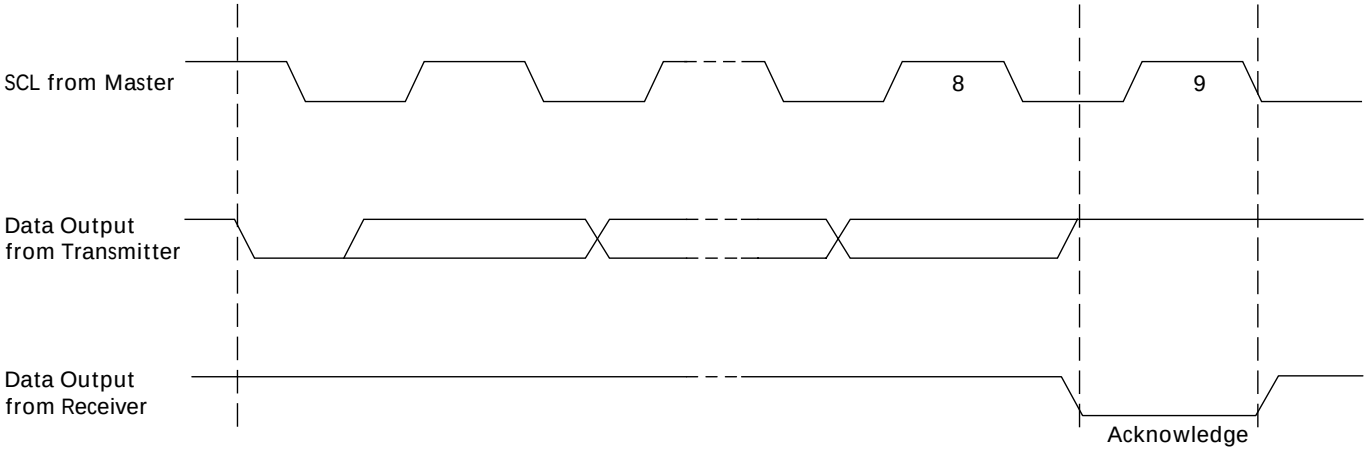


Table 16: EEPROM Device Select Code

Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 17: EEPROM Operating Modes

MODE	RW BIT	WC	BYTES	INITIAL SEQUENCE
Current Address Read	1	VIH or VIL	1	START, Device Select, RW = '1'
Random Address Read	0	VIH or VIL	1	START, Device Select, RW = '0', Address
	1	VIH or VIL	1	reSTART, Device Select, RW = '1'
Sequential Read	1	VIH or VIL	≥ 1	Similar to Current or Random Address Read
Byte Write	0	VIL	1	START, Device Select, RW = '0'
Page Write	0	VIL	≤ 16	START, Device Select, RW = '0'

Figure 16: SPD EEPROM Timing Diagram

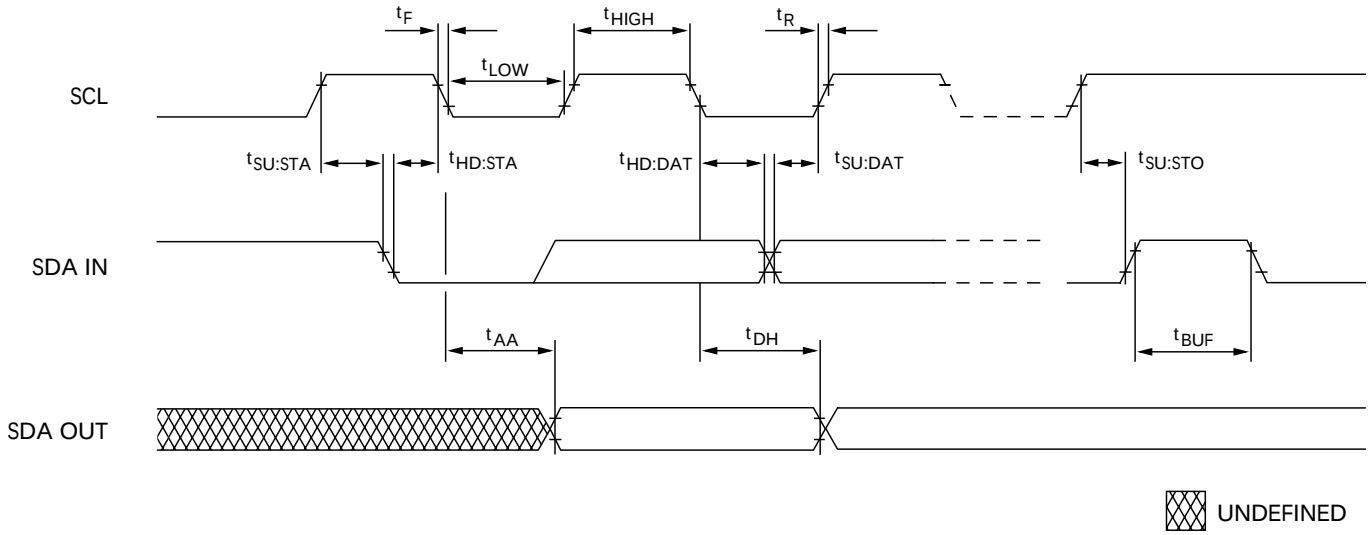


Table 18: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: VIN = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{REF}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

Table 19: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

NOTE:

1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 20: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes appear on page 26

BYTE	DESCRIPTION	ENTRY (VERSION)	MT4VDDT1632U	MT4VDDT3232U
0	Number of SPD Bytes Used By Micron	128	80	80
1	Total Number of Bytes In SPD Device	256	08	08
2	Fundamental Memory Type	DDR SDRAM	07	07
3	Number of Row Addresses on Assembly	12, 13	0C	0D
4	Number of Column Addresses on Assembly	10	0A	0A
5	Number of Physical Ranks on DIMM	1	01	01
6	Module Data Width	32	20	20
7	Module Data Width (Continued)	0	00	00
8	Module Voltage Interface Levels	SSTL 2.5V	04	04
9	SDRAM Cycle Time, (^{t}CK) (CAS Latency = 2.5)	6ns (-6) 7.0ns (-75Z) 7.5ns (-75)	60 70 75	60 70 75
10	SDRAM Access From Clock, ^{t}AC (CAS Latency = 2.5)	0.7ns (-6) 0.75ns (-75Z/-75)	70 75	70 75
11	Module Configuration Type	None	00	00
12	Refresh Rate/type	15.62µs, 7.8µs/SELF	80	82
13	Sdram Device Width (Primary DDR SDRAM)	8	08	08
14	Error-checking Ddr Sdram Data Width	None	00	00
15	Minimum Clock Delay, Back-to-back Random Column Access	1 clock	01	01
16	Burst Lengths Supported	2, 4, 8	0E	0E
17	Number Of Banks On Ddr Sdram Device	4	04	04
18	Cas Latencies Supported	2, 2.5	0C	0C
19	Cs Latency	0	01	01
20	We Latency	1	02	02
21	Sdram Module Attributes	Unbuffered/Diff. Clock	20	20
22	Sdram Device Attributes: General	Fast/Concurrent AP	C0	C0
23	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2)	7.5ns (-6) 10ns (-75)	75 A0	75 A0
24	SDRAM Access from Clock, ^{t}AC (CAS Latency = 2)	0.7ns (-6) 0.75ns (-75Z/-75)	70 75	70 75
25	SDRAM Cycle Time, ^{t}CK (CAS Latency = 1.5)	N/A	00	00
26	SDRAM Access from CK, ^{t}AC (CAS Latency = 1.5)	N/A	00	00
27	Minimum Row Precharge Time, ^{t}RP (see note 3)	18ns (-6) 20ns (-75Z/-75)	48 50	48 50
28	Minimum Row Active to Row Active, ^{t}RRD	12ns (-6) 15ns (-75Z/-75)	30 3C	30 3C
29	Minimum RAS# to CAS# Delay, ^{t}RCD	18ns (-6) 20ns (-75Z/-75)	48 50	48 50
30	Minimum RAS# Pulse Width, ^{t}RAS (See note 1)	42ns (-6) 45ns (-75Z/-75)	2A 2D	2A 2D
31	Module Rank Density	64MB, 128MB	10	20
32	Address and Command Setup Time, ^{t}IS (See note 2)	0.8ns (-6) 1.0ns (-75Z/-75)	80 A0	80 A0

Table 20: Serial Presence-Detect Matrix (Continued)

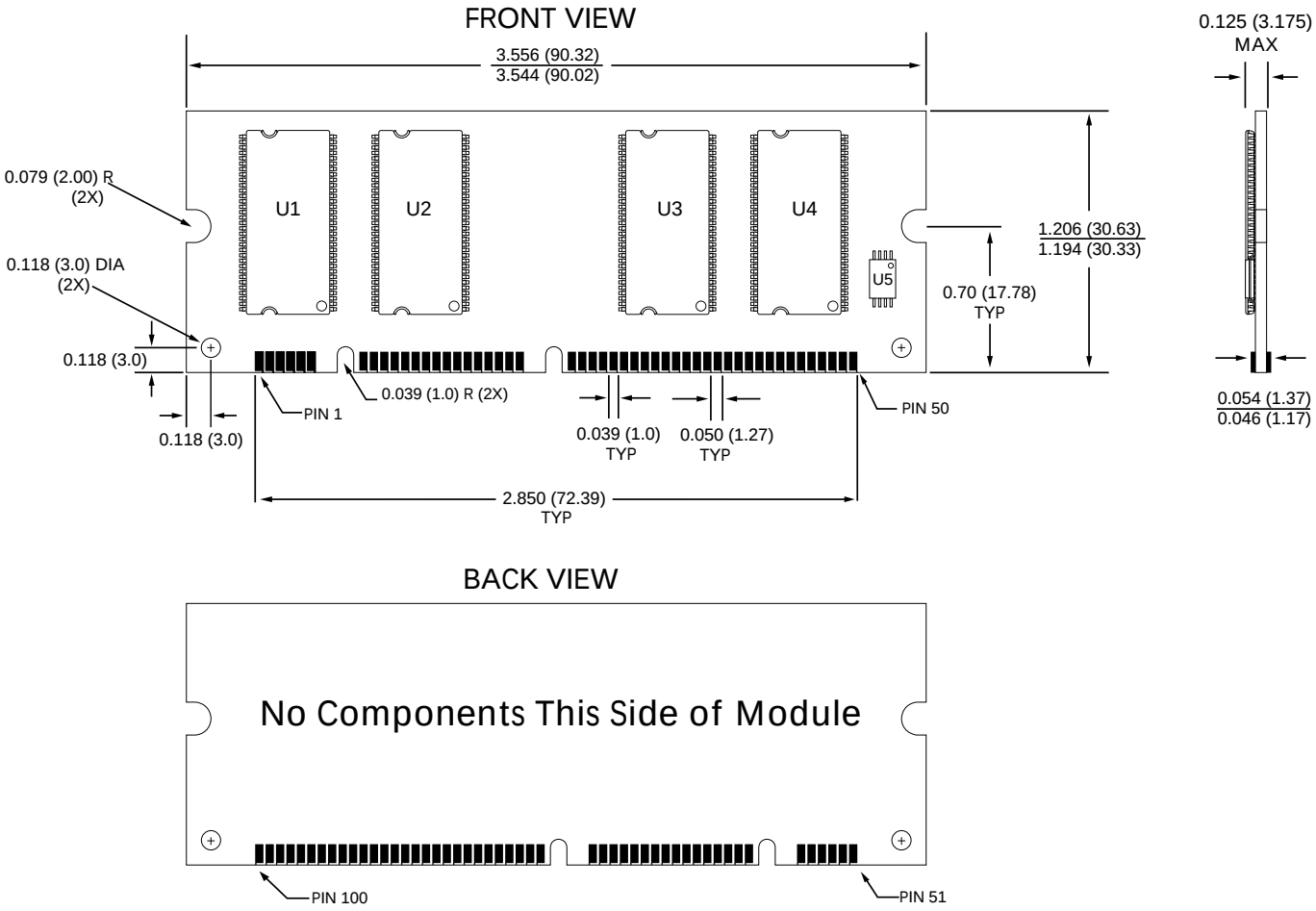
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes appear on page 26

BYTE	DESCRIPTION	ENTRY (VERSION)	MT4VDDT1632U	MT4VDDT3232U
33	Address and Command Hold Time, ^{t}IH (See note 2)	0.8ns (-6) 1.0ns (-75Z/-75)	80 A0	80 A0
34	Data/Data Mask Input Setup Time, ^{t}DS	0.45ns (-6) 0.5ns (-75Z/-75)	45 50	45 50
35	Data/Data Mask Input Hold Time, ^{t}DH	0.45ns (-6) 0.5ns (-75Z/-75)	45 50	45 50
36-40	Reserved		00	00
41	Min Active Auto Refresh Time, ^{t}RC (see note 3)	60ns (-6) 65ns (-75Z/-75)	3C 41	3C 41
42	Minimum Auto Refresh to Active/Auto Refresh Command Period, ^{t}RFC	72ns (-6) 75ns (-75Z/-75)	48 4B	48 4B
43	SDRAM Device Max Cycle Time, ^{t}CKMAX	12ns (-6) 13ns (-75Z/-75)	30 34	30 34
44	SDRAM Device Max DQS-DQ Skew Time, ^{t}DQSQ	0.45ns (-6) 0.5ns (-75Z/-75)	2D 3C	2D 3C
45	SDRAM Device Max Read Data Hold Skew Factor, ^{t}QHS	0.55ns (-6) 0.75ns (-75Z/-75)	55 75	55 75
46	Reserved		00	00
47	DIMM Height		01	01
48–61	Reserved		00	00
62	SPD Revision	Release 1.0	10	10
63	Checksum for Bytes 0-62	-6 -75Z -75	D4 94 C4	E7 A7 D7
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC ID Code	(Continued)	FF	FF
72	Manufacturing Location	01–12	01–0C	01–0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	Pcb Identification Code	1-9	01-09	01-09
92	Identification Code (Continued)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-specific Data (RSVD)		–	–

NOTE:

1. The value of ^{t}RAS used for -75 modules is calculated from ^{t}RC - ^{t}RP. Actual device spec. value is 40 ns.
2. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster min-imim slew rate is met.
3. The value of ^{t}RP, ^{t}RCD and ^{t}RAP for -335 modules indicated as 18ns to align with industry specifications; actual DDR SDRAM device specification is 15ns.

Figure 17: 100-Pin DIMM Dimensions



NOTE:

All dimensions in inches (millimeters); $\frac{MAX}{MIN}$ or typical where noted.

Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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