CIRCUIT PROTECTION
308 Constitution Drive
Menlo Park, CA USA
www.circuitprotection.com

PolyZen

Polymer Enhanced Zener Diode
Micro-Assemblies

Over-Voltage Circuit Protection Products

PRODUCT: ZEN056V260A16CE

DOCUMENT: SCD28169
REV LETTER: A
REV DATE: JUNE 06, 2012
PAGE NO.: 1 OF 8

Specification Status: RELEASED

GENERAL DESCRIPTION

TE Circuit Protection PolyZen devices are polymer enhanced, precision Zener diode micro-assemblies. They offer resettable protection against multi-Watt fault events without the need for multi-Watt heat sinks.

The Zener diode used for voltage clamping in a PolyZen micro-assembly was selected due to its relatively flat voltage vs current response. This helps improve output voltage clamping, even when input voltage is high and diode currents are large.

An advanced feature of the PolyZen micro-assembly is that the Zener diode is thermally coupled to a resistively non-linear, polymer PTC (positive temperature coefficient) layer. This PTC layer is fully integrated into the device, and is electrically in series between V_{IN} and the diode clamped V_{OUT}.

This advanced PTC layer responds to either extended diode heating or overcurrent events by transitioning from a low to high resistance state, also known as ”tripping”. A tripped PTC will limit current and generate voltage drop. It helps to protect both the Zener diode and the follow-on electronics and effectively increases the diode’s power handling capability.

The polymer enhanced Zener diode helps protect sensitive portable electronics from damage caused by inductive voltage spikes, voltage transients, incorrect power supplies and reverse bias. These devices are particularly suitable for portable electronics and other low-power DC devices.

BENEFITS

- Stable Zener diode helps shield downstream electronics from overvoltage and reverse bias
- Trip events shut out overvoltage and reverse bias sources
- Analog nature of trip events minimizes upstream inductive spikes
- Minimal power dissipation requirements
- Single component placement

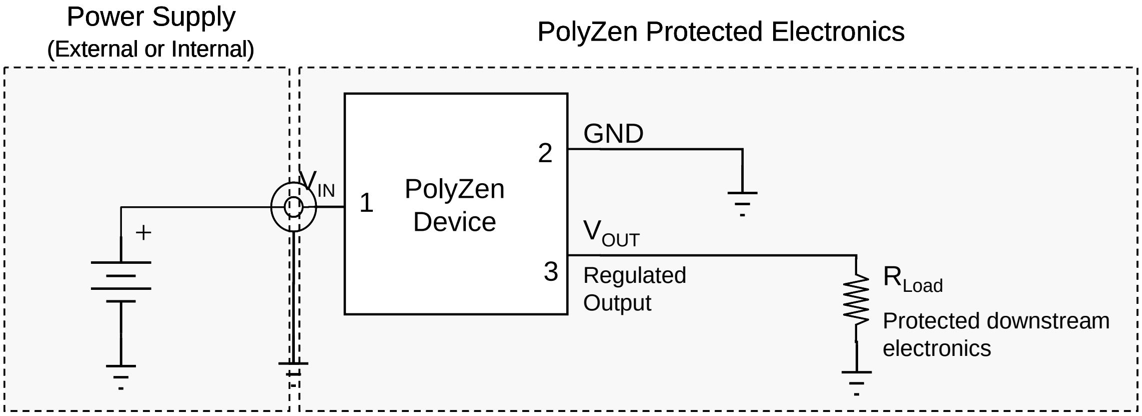
FEATURES

- Overvoltage transient suppression
- Stable V_Z vs fault current
- Time delayed, overvoltage trip
- Time delayed, reverse bias trip
- Multi-Watt power handling capability
- Integrated device construction
- RoHS Compliant

TARGET APPLICATIONS

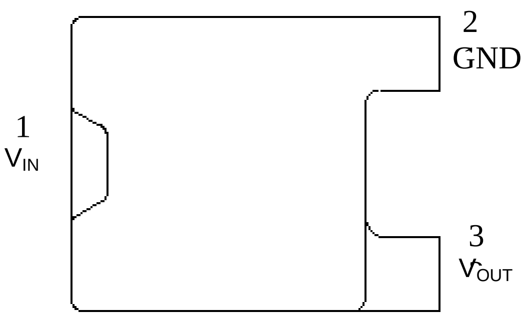
- DC power port protection in portable electronics
- DC power port protection for systems using barrel jacks for power input
- Internal overvoltage & transient suppression
- DC output voltage regulation
- Tablet PCs and portable electronics

TYPICAL APPLICATION BLOCK DIAGRAM

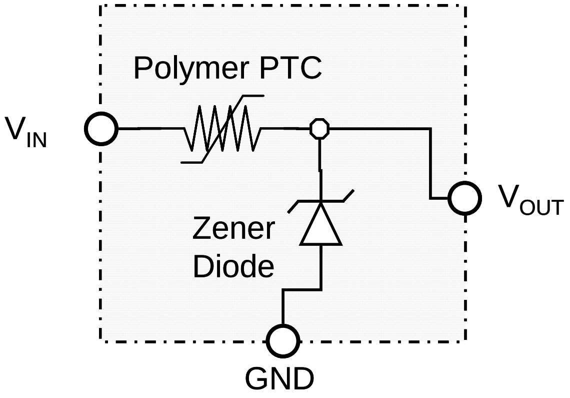


CONFIGURATION INFORMATION

Pin Configuration (Top View)



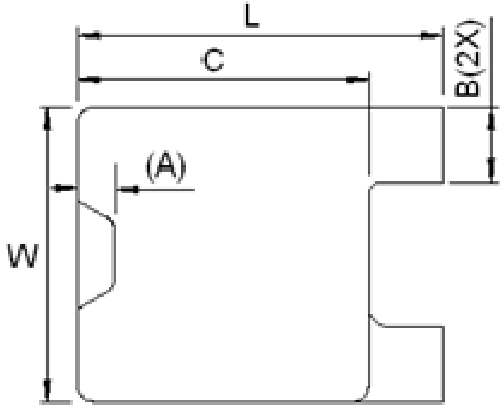
Block Diagram



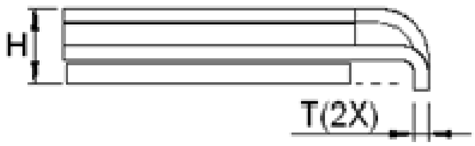
PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1	V_{IN}	**V_{IN} .** Protected input to Zener diode
2	GND	**GND**
3	V_{OUT}	**V_{OUT} .** Zener regulated voltage output

MECHANICAL DIMMENSIONS

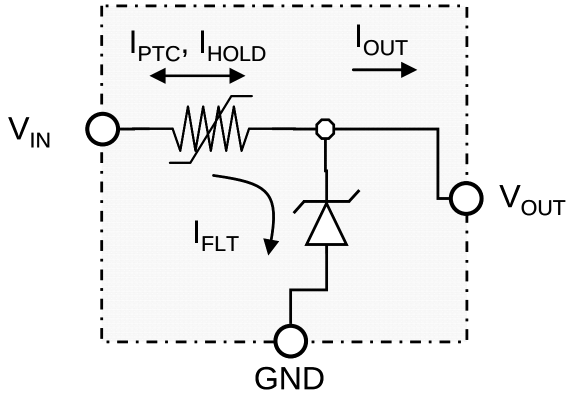


		Min	Typ	Max
			(mm)	
Length	L	4.8	5.0	5.2
Width	W	3.8	4.0	4.2
Height	H	0.8	1.0	1.2
Dimension	（A）	0.7	0.8	0.9
	B(2X)	0.9	1.0	1.1
	C	3.9	4.05	4.2
	T(2X)	0.1	0.2	0.3



DEFINITION of TERMS

I_{PTC}	Current flowing through the PTC portion of the circuit
I_{FLT}	RMS fault current flowing through the diode
I_{OUT}	Current flowing out the V_{OUT} pin of the device
Trip Event	A condition where the PTC transitions to a high resistance state, thereby significantly limiting I_{PTC} and related currents.
Trip Endurance	Time the PTC portion of the device remains in a high resistance state.



GENERAL SPECIFICATIONS

Operating Temperature	-40º to +85ºC
Storage Temperature	-40º to +85ºC

TYPICAL ELECTRICAL CHARACTERISTICS[1-3, 11] (Typical unless otherwise specified)

V_Z[4] (V)			I_{zt}[4] (A)	I_{HOLD}[5] (A)		Leakage Current		R_{Typ}[6] (Ohms)	$R1_{Max}$[7] (Ohms)	V_{Int} Max[8]		I_{FLT} Max[9]		Tripped Power Dissipation[10]	
Min	Typ	Max		@20ºC	@60ºC	Test Voltage (V)	Max Current (mA)			V_{INT} Max (V)	Test Current (A)	I_{FLT} Max (A)	Test Voltage (V)	Power (W)	Test Voltage (V)
5.45	5.60	5.75	0.1	2.6	2.0	5.25	10.0	0.032	0.045	16	5	+5 -40	+16 -12	1	16

Note 1: Electrical characteristics determined at 25ºC unless otherwise specified.

Note 2: This device is intended for limited fault protection. Repeated trip events or extended trip endurance can degrade the device and may affect performance to specifications. Performance impact will depend on multiple factors including, but not limited to, voltage, trip current, trip duration, trip cycles, and circuit design. For details or ratings specific to your application contact TE Connectivity Circuit Protection Division directly.

Note 3: Specifications developed using 1.0 ounce 0.045" wide copper traces on dedicated FR4 test boards. Performance in your application may vary.

Note 4: I_{zt} is the current at which V_z is measured ($V_Z = V_{OUT}$). Additional V_Z values are available on request.

Note 5: I_{HOLD}: Maximum steady state I_{PTC} (current entering or exiting the V_{IN} pin of the device) that will not generate a trip event at the specified temperature. Specification assumes I_{FLT} (current flowing through the Zener diode) is sufficiently low so as to prevent the diode from acting as a heat source. Testing is conducted with an "open" Zener.

Note 6: R Typ: Resistance between V_{IN} and V_{OUT} pins during normal operation at room temperature.

Note 7: R_{1Max}: The maximum resistance between V_{IN} and V_{OUT} pins at room temperature, one hour after first tripped event or after reflow soldering.

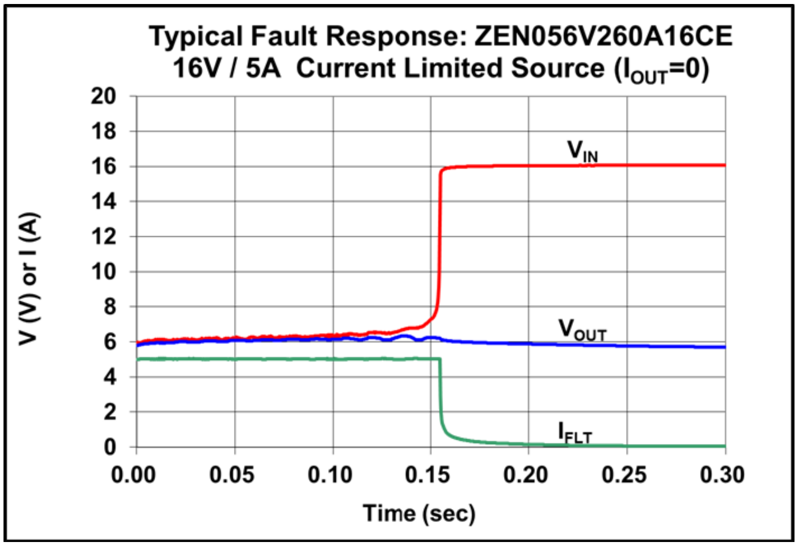
Note 8: V_{INT} Max: V_{INT} Max is defined as the voltage at which typical qualification devices (98% devices, 95% confidence) survived at least 100 trip cycles and 24 hours trip endurance at the specified voltage and current (I_{PTC}). V_{INT} Max testing is conducted using a "shorted" load ($V_{OUT} = 0$ V). V_{INT} Max is a survivability rating, not a performance rating. For performance ratings, see Note 2.

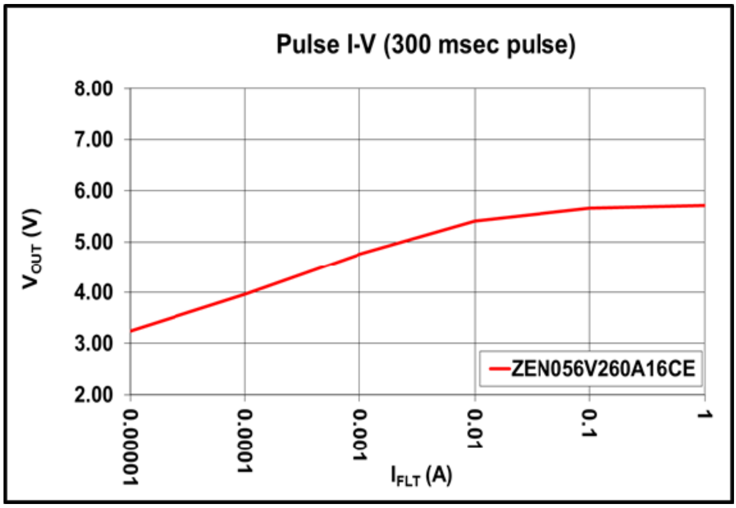
Note 9: I_{FLT} Max: Maximum RMS fault current the diode portion of the device can withstand and remain resettable. Specification is dependent on the direction of current flow through the diode. RMS fault currents above I_{FLT} Max may permanently damage the PolyZen device. Specification assumes $I_{OUT} = 0$. Testing conducted with no load connected to V_{OUT}.

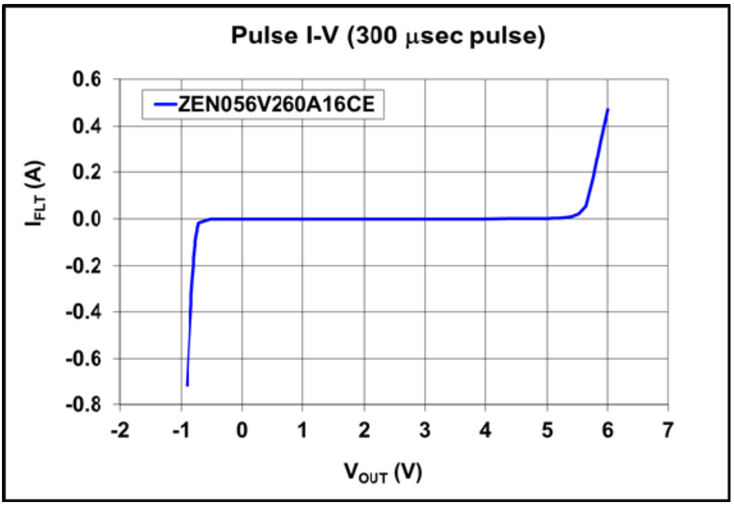
Note 10: The power dissipated by the device when in the "tripped" state, as measured on TE test boards (see note 3).

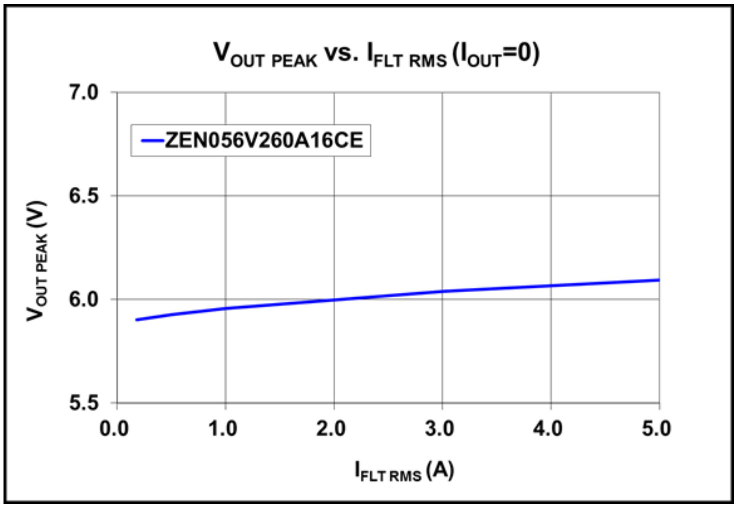
Note 11: Specifications based on limited qualification data and subject to change.

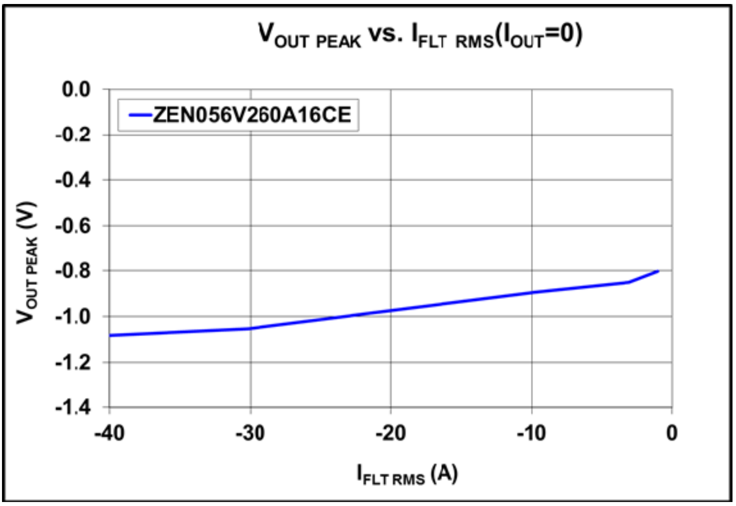
TYPICAL DEVICE CHARACTERISTICS

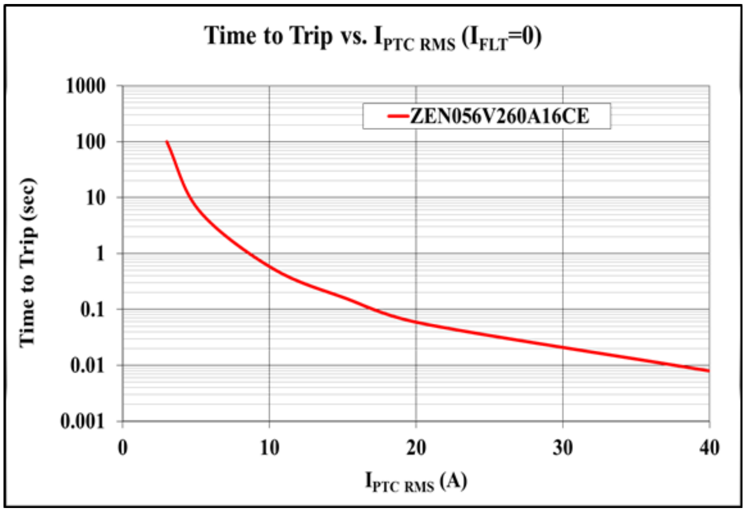


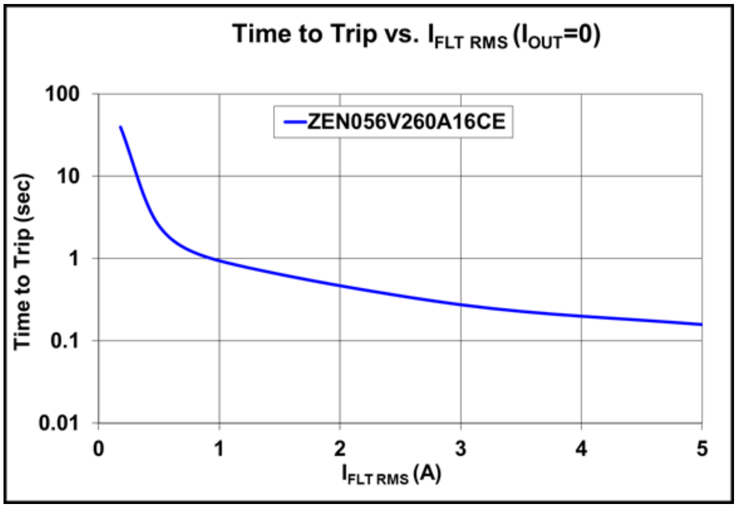


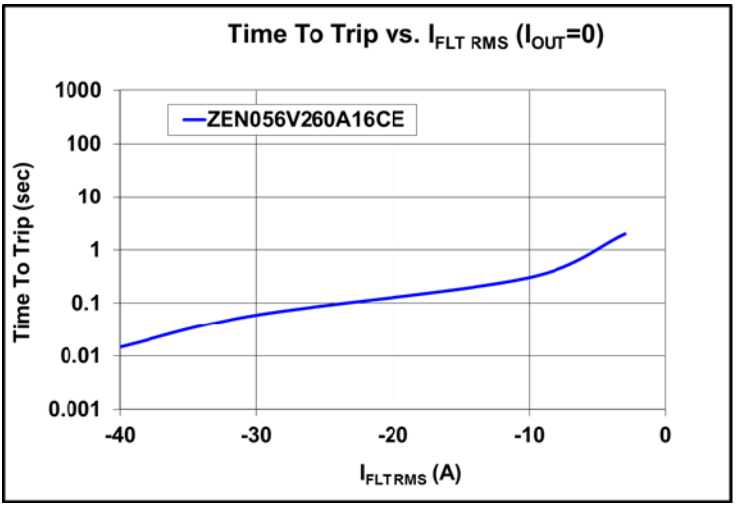


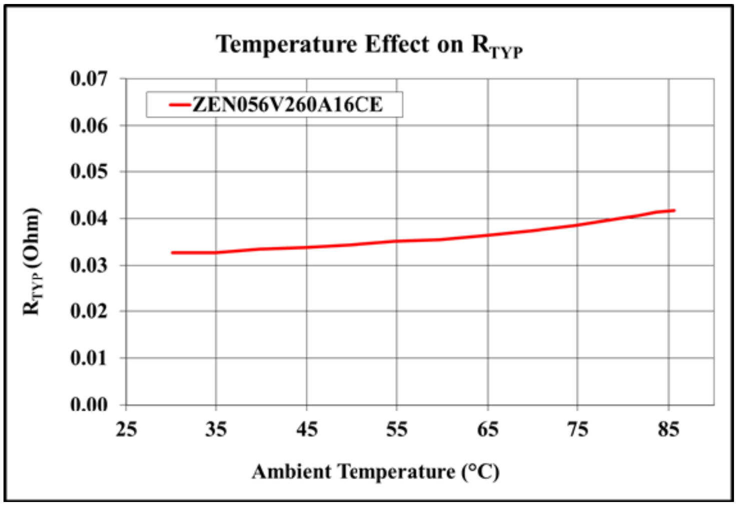


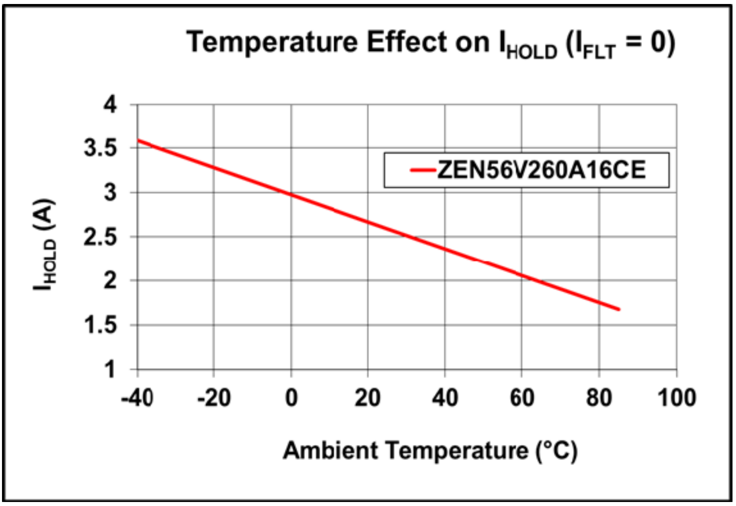



Time to Trip vs. $I_{PTC\ RMS}$ (I_{FLT}=0)

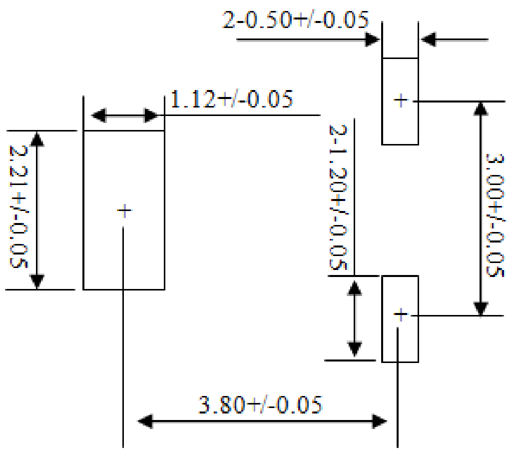

Time to Trip vs. $I_{FLT\ RMS}$ (I_{OUT}=0)


Time To Trip vs. $I_{FLT\ RMS}$ (I_{OUT}=0)

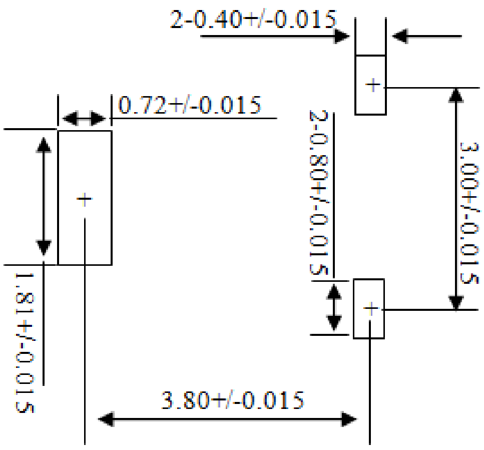

Temperature Effect on R_{TYP}


Temperature Effect on I_{HOLD} (I_{FLT} = 0)

RECOMMENDED PAD LAYOUT (mm)

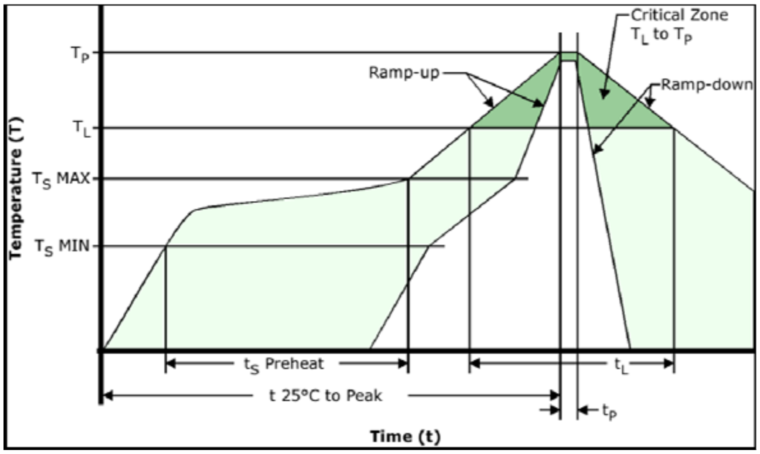


RECOMMENDED SOLDER STENCIL (mm)



Solder thickness – 0.15mm

RECOMMENDED SOLDER REFLOW PROFILE

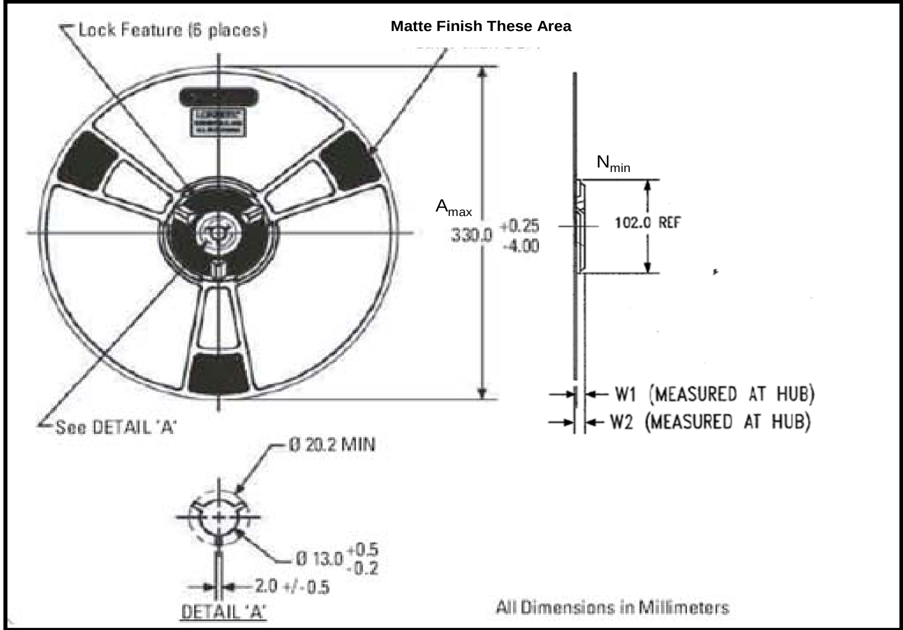


Classification Reflow Profiles	
Profile Feature	**Pb-Free Assembly**
Average Ramp-up Rate (Ts Max to Tp)	3° C/second max
Average Ramp-down Rate (Tp to T_L)	6° C/second max
Preheat	
• Temperature Min (Ts Min)	150° C
• Temperature Max (Ts Max)	200° C
• Time (ts Preheat)	60-180 seconds
Time maintained above:	
• Temperature (T_L)	217° C
• Time (t_L)	60-150 seconds
Peak / Classification Temperature	
• Temperature (T_P)	260° C
Time within 5° C of actual peak	
• Time (t_P)	20-40 seconds
Time 25° C to peak Temperature	8 minutes max

PACKAGING

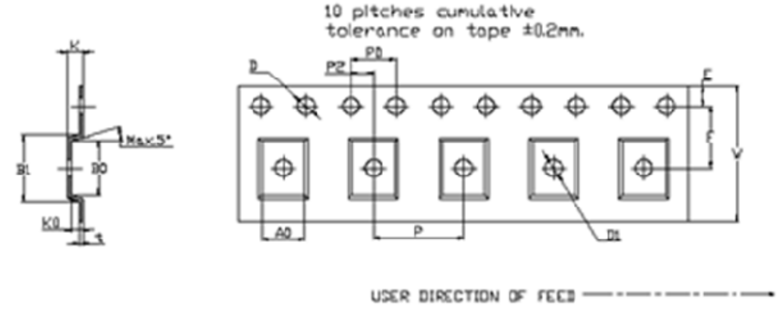
Packaging	Tape & Reel	Standard Box
ZEN056V260A16CE	4,000	20,000

REEL DIMENSION



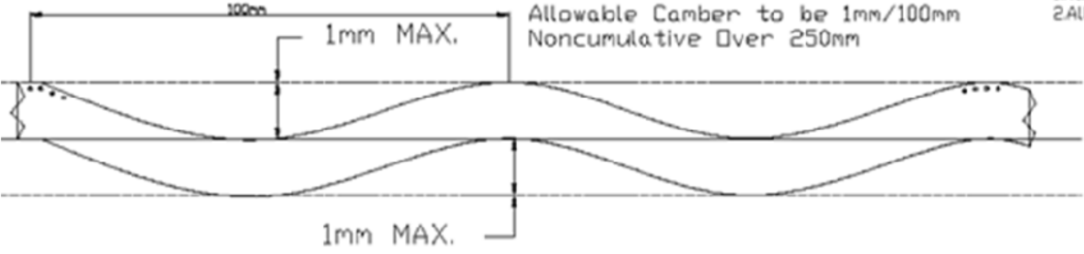
A_{max} = 330
N_{min} = 102
W_1 = 8.4
W_2 = 11.1

TAPE DIMENSIONS

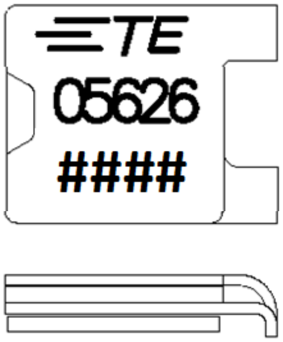


Product Control Number (PCN) Description	OVCE CARRIER TAPE
D0	1.55+0.1−0.0
E1	1.75±0.1
P0	4.0±0.1
T max	0.35
B1 max	6.2
D1 min	1.5
F	5.5±0.05
K1 max	1.7
P2	2.0±0.05
W	12.0±0.3
P1	8.0±0.1
A0	4.3±0.05
B0	5.3±0.05
K0	1.3±0.05

NOTE:
1.Materials: Conductive PS.
2.All dimensions meet EIA-481-D.



DEVICE MARKINGS INFORMATION



Markings	Vz	Hold Current
05626	5.6V	2.6A
####	Last 4 digits of batch number	

MATERIALS INFORMATION

ROHS Compliant
Directive 2002/95/EC Compliant

ELV Compliant
Directive 2000/53/EC Compliant

Halogen Free*
HF

* Halogen Free refers to: Br≤900ppm, Cl≤900ppm, Br+Cl≤1500ppm.